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Modulation Strategy with Minimum Switching Losses for Three-Phase Non-Isolated AC–DC Matrix Converters

Riccardo Testa [1,2], Luca Vancini [1], Gabriele Rizzoli [1], Michele Mengoni [1], Antonio Femia [1], Luca Zarri [1,*] and Angelo Tani [1]

[1] Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi", University of Bologna, 40136 Bologna, Italy; riccardo.testa3@unibo.it (R.T.); luca.vancini4@unibo.it (L.V.); gabriele.rizzoli@unibo.it (G.R.); michele.mengoni@unibo.it (M.M.); antonio.femia3@unibo.it (A.F.); angelo.tani@unibo.it (A.T.)

[2] OCEM Power Electronics, 40056 Valsamoggia, Italy

* Correspondence: luca.zarri2@unibo.it

Abstract: This paper presents an analysis of the operational characteristics of three-phase AC–DC matrix converters, which operate as rectifiers but possess a range of additional capabilities. These include the ability to reverse the power flow, control the input power factor, and generate a multilevel output voltage. The analysis yields a modulation strategy that minimizes switching losses. The proposed modulation strategy is compared with seven well-known space vector modulation strategies in terms of efficiency and distortion of input and output current. The performance is experimentally validated.

Keywords: matrix converter; modulation strategy; switching losses

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1. Introduction

Passive rectifiers are a prevalent choice for interfacing power converters and the grid, mainly due to their simple operation, high efficiency, resilience, and relatively low cost. However, the total harmonic distortion (THD) of the input currents is relatively high. Nevertheless, some improvements can be achieved by incorporating inductive filters. The use of thyristor-based rectifiers results in a reduction in the input power factor as the output voltage decreases. Furthermore, the reversal of power flow cannot be achieved through a mere change in the current direction; instead, more complex bidirectional power conversion structures are necessary.

It can thus be concluded that passive rectifiers are not suitable for emerging applications such as Vehicle-to-Grid (V2G) power exchange or smart grid applications, where the current flow can be in both directions [1,2].

Three-phase pulse-modulated voltage- and current-source rectifiers demonstrate superior performance in terms of input current harmonics and power factor control. Consequently, some authors concur that they will replace the passive and silicon-controlled rectifiers [3,4]. These converters are typically employed as an active front-end to the grid. However, the DC-link voltage of voltage-source rectifiers is greater than the phase-to-phase input voltage, rendering them unsuitable for low-voltage loads, such as batteries, due to the necessity of an additional step-down power stage or a bulky input transformer. In contrast, current source rectifiers have been used in contexts where the output voltage is lower than the input voltage (step-down) and the reversal of the output power is not required, such as in telecommunications and data centers, as well as in off-board DC fast chargers [5]. This configuration is typically favored for high-power applications, whereas in low-power applications, voltage source inverters offer simpler control, a wider range of component options, and lower conduction losses.

For the sake of completeness, several additional possibilities for a rectifying stage could be considered. Among them, the Vienna rectifier is a three-level ac–dc converter,

which is widely used in many applications. The advantages of this converter include low Total Harmonic Distortion (THD), high power density, and high efficiency. It should be noted, however, that the power flow is unidirectional [6,7]. Moreover, multilevel rectifiers may be employed in applications requiring high voltage or high power quality. Some studies were conducted with the objective of reducing the switch count, i.e., namely the removal of some power switches. This simplification reduces the number of gate drivers, cost and complexity of the system [8]. Topologies derived from the conventional multilevel configurations, such as Neutral Point Clamped, Cascaded H-Bridge, Flying Capacitor, Modular Multilevel Converter and T-Type, were investigated. Finally, the possibility of a dual-stage rectifier must be considered, where the input stage is a power factor corrector, and the second stage is a dc–dc converter [9,10].

A topology that may be regarded as an extension of current-source rectifiers and can act as a bidirectional active front end is the three-phase AC–DC matrix converter [11]. The three-phase AC–DC matrix converter is capable of adjusting the input power factor, reversing the power flow, and reducing the harmonic content of input and output currents. In addition, as it is inherently a step-down converter, it is well-suited to applications that necessitate low DC voltages. These considerations collectively motivate a more profound comprehension of the operational characteristics of the AC–DC matrix converter. While the literature on AC–DC matrix converters is not as extensive as that on AC–AC matrix converters, it has nevertheless initiated numerous research projects.

In [12,13], the authors proposed a four-quadrant rectifier based on a matrix converter with high-frequency isolation and soft commutation. This configuration is the so-called isolated matrix rectifier or isolated AC–DC matrix converter. It has received attention for automotive applications and is the subject of some lively lines of research [14–16]. It should be noted, however, that the matrix converter is employed to generate the intermediate high-frequency AC voltage for the isolation stage rather than being used directly to produce the output voltage for the converter. A simpler configuration without isolation but still operated at high frequency and combined with a current-doubler rectifier was proposed to achieve step-down AC–DC conversion at low DC voltages with greater efficiency than the conventional buck converter for aerospace applications [17].

The number of research lines related to non-isolated converters is relatively limited; however, several technological developments were observed. In [18], an ultrasparse AC–DC matrix converter was proposed as a battery charger with low output voltage. The number of switches is notably reduced but the power flow is unidirectional. In [19], an AC–DC matrix converter, derived from a three-phase direct AC–AC matrix converter by the removal of one leg, was presented, along with a suitable space vector modulation. The advantages of a matrix rectifier, including input power factor control, power flow reversal and a reduction in the input filter size, were investigated and clearly motivated. Subsequently, specific control techniques were developed for AC–DC matrix converters. The direct power control method directly controls both the active and reactive power components of the source while achieving sinusoidal input currents and the output DC voltage/current [20–22]. A Space Vector Modulation (SVM) strategy with the optimization of the duty cycle of the zero vector was developed for matrix rectifiers with the objective of reducing the Total Harmonic Distortion (THD) and ripple in the output current [23].

Unbalanced grid voltage occurs frequently due to disturbances. Unbalanced voltage conditions may cause voltage ripples on the DC side and low-order harmonics in the grid current, so specific control strategies have been developed. Two independent control schemes for active and reactive power can be used to control the instantaneous active power and the average reactive power, respectively [24].

Over time, several Model Predictive Control (MPC) algorithms have been used as an alternative approach to the control of AC–DC matrix converters [25,26]. MPC allows the input power factor to be controlled while the output voltage is kept constant. Also, active damping can be included. The input CL filter can cause resonance and lead to distorted input currents. To suppress the resonance, instead of a physical damping resistor, which

brings extra power loss, the active damping mimics the presence of a virtual resistor in parallel to the input filter capacitor, thus damping the current harmonics without affecting the fundamental component.

The present paper makes the following contributions:

(i) it defines a modulation technique for the AC–DC matrix converter as a derivation of the traditional techniques used for AC–AC matrix converters;
(ii) it analyzes the modulation strategy in general terms by representing the switch states as complex numbers;
(iii) it presents a modulation strategy with the theoretical minimum switching losses.

The paper is structured as follows. Section 2 illustrates the modulation theory, Section 3 analyzes the operating range, Section 4 describes an SVM modulation strategy, and Section 5 investigates the reduction in the switching losses and output current ripple. Finally, experimental results substantiate the feasibility and the performance of the proposed modulation strategy, as detailed in Section 6.

2. Modulation Strategy for AC–DC Matrix Converters

The performance of matrix converters is contingent upon the modulation strategy that is employed. A number of modulation strategies based on disparate mathematical methodologies have been proposed in the past for traditional direct three-phase matrix converters (MC) [27]. Each of these strategies exhibits distinct characteristics, including the number of switch commutations per switching period and the degree of input voltage utilization. SVM for MCs has been the subject of extensive research by the academic community, due to its suitability for digital implementation, effective utilization of the input voltage, and the reduction in the root-mean-square value of the load current ripple [28]. A comprehensive solution to the control problem of three-phase direct AC–AC matrix converters is presented in [29]. This solution is based on the representation of the switch states by means of space vectors, which were originally referred to as Duty-Cycle Space Vectors (DCSVs). This method places particular emphasis on all the parameters that affect the performance of the modulation strategy, and these can be freely chosen. In the next section, the same method will be adapted for the analysis of AC–DC matrix converters.

2.1. Input–Output Equations of the AC/DC Matrix Converters

With reference to Figure 1, the expression of the output voltage v_o is as follows:

$$v_o = v_{o1} - v_{o2} = \sum_{k=1}^{3} (m_{1,k} - m_{2,k}) v_{i,k} \tag{1}$$

where $v_{i,1}$, $v_{i,2}$, and $v_{i,3}$ are the input pole voltages, i.e., the potentials of the input terminals, and the signals $m_{h,k}$ (h = 1, 2 and k = 1, 2, 3) are the duty cycles of the switches $S_{h,k}$. Since the converter does not include elements that can store energy, if the converter power losses are neglected, the input power is equal to the output power:

$$\sum_{k=1}^{3} i_{i,k} v_{i,k} = v_o i_o = \sum_{k=1}^{3} (m_{1,k} - m_{2,k}) v_{i,k} i_o \tag{2}$$

where i_o is the output current.

Equation (2) is verified for any value of $v_{i,k}$, so it is possible to conclude that the input currents are:

$$i_{i,k} = (m_{1,k} - m_{2,k}) i_o. \quad k = 1, 2, 3. \tag{3}$$

The duty cycles $m_{1,k}$ and $m_{2,k}$ must satisfy the constraints (4), which prevent short-circuits of the source and over-voltages due to an abrupt interruption of the load current:

$$\sum_{k=1}^{3} m_{h,k} = 1, \quad h = 1,2. \tag{4}$$

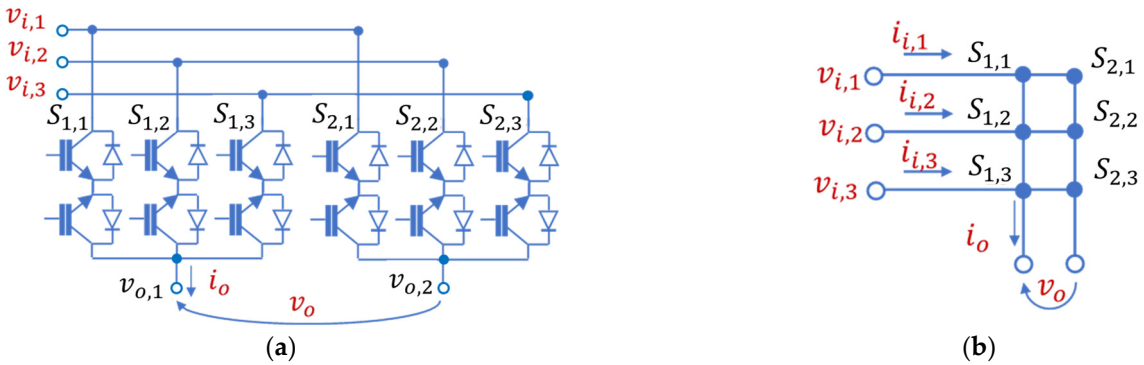


Figure 1. Basic scheme of a three-phase AC–DC matrix converter: (**a**) converter structure; (**b**) simplified matrix representation.

2.2. Input–Output Equations in Terms of Space Vectors

Under the assumption that sums of the input pole voltages and the input currents are zero, it is straightforward to express the input pole voltages and currents in terms of space vectors $\overline{v}_i$ and $\overline{i}_i$. For the kth input phase, the following relationships can be verified:

$$v_{i,k} = \overline{v}_i \cdot \overline{\alpha}_k \tag{5}$$

$$i_{i,k} = \overline{i}_i \cdot \overline{\alpha}_k \tag{6}$$

where "$\cdot$" is the dot product, defined as the real part of the product between the first operand and the complex conjugate of the second operand, and

$$\overline{\alpha}_k = e^{j\frac{2\pi}{3}(k-1)}. \tag{7}$$

The state of the converter legs can be represented by two complex numbers $\overline{m}_1$, $\overline{m}_2$ defined as follows:

$$\overline{m}_h = \frac{2}{3}\sum_{k=1}^{3} m_{h,k}\overline{\alpha}_k, \quad h = 1,2. \tag{8}$$

By replacing (5) and (6) in (1) and (3), and considering (8), the input–output equations of a three-phase AC–DC matrix converter can be written in terms of $\overline{m}_1$ and $\overline{m}_2$ as follows:

$$v_o = \frac{3}{2}\overline{v}_i \cdot (\overline{m}_1 - \overline{m}_2) \tag{9}$$

$$\overline{i}_i = i_o(\overline{m}_1 - \overline{m}_2). \tag{10}$$

Two new variables $\overline{m}_d$ and $\overline{m}_0$ can be introduced to simplify the mathematical formulation of (9) and (10):

$$\overline{m}_d = \overline{m}_1 - \overline{m}_2 \tag{11}$$

$$\overline{m}_0 = \frac{1}{2}(\overline{m}_1 + \overline{m}_2). \tag{12}$$

The complex number $\overline{m}_d$ is here referred to as "direct component", whereas $\overline{m}_0$ is the "zero-sequence component" of $\overline{m}_1$ and $\overline{m}_2$.

As a result, the input and output relationships of the converter become:

$$v_o = \frac{3}{2}\overline{v}_i \cdot \overline{m}_d \tag{13}$$

$$\overline{i}_i = i_o \overline{m}_d. \tag{14}$$

As can be observed, the output voltage and the input current are solely dependent on $\overline{m}_d$ and are not influenced by the values of $\overline{m}_0$. This behavior is analogous to that observed in pulse-width modulated three-phase inverters, wherein the output voltage vector is independent of the zero-sequence of the modulating signals. In AC–DC matrix converters, this role is fulfilled by a complex quantity, $\overline{m}_0$, due to the higher complexity of the converter structure.

If the unit vector $\overline{\psi}_{ref}$ denotes the desired direction of the input current space vector, and $v_{o,ref}$ is the desired output voltage, it can be demonstrated by solving (13) and (14) that $\overline{m}_d$ has the following expression:

$$\overline{m}_{d,ref} = \frac{2}{3}\frac{v_{o,ref}\,\overline{\psi}_{ref}}{\overline{v}_i \cdot \overline{\psi}_{ref}} \tag{15}$$

whereas $\overline{m}_0$ can be freely chosen to improve the performance of the modulation strategy.

Solving (11) and (12) for $\overline{m}_1$ and $\overline{m}_2$, one finds:

$$\overline{m}_h = (-1)^{h-1}\frac{\overline{m}_d}{2} + \overline{m}_0, \;\; h = 1, 2. \tag{16}$$

The quantity $\overline{m}_0$ is equivalent to two degrees of freedom that can be used to define any modulation strategy. The significance of $\overline{m}_1$ and $\overline{m}_2$ lies in the fact that they facilitate the calculation of the switch duty cycles. In practice, the duty cycles $m_{h,k}$ can be found by solving the set of Equations (4) and (8), which yields the following result:

$$m_{h,k} = \frac{1}{3} + \overline{m}_h \cdot \overline{\alpha}_k, \;\; h = 1,\ 2,\ k = 1,\ 2,\ 3. \tag{17}$$

The general solution presented in (15)–(17) encompasses all modulation strategies as specific instances.

3. Control Range of the Output Voltage

The duty cycles are bounded between 0 and 1, i.e.,

$$0 \le m_{h,k} \le 1, \;\; h = 1,\ 2,\ k = 1,\ 2,\ 3. \tag{18}$$

By considering (16) and (17), (18) becomes as follows:

$$0 \le \frac{(-1)^{h-1}}{2}\overline{m}_d \cdot \overline{\alpha}_k + m_{0,k} \le 1, \;\; h = 1,\ 2 \tag{19}$$

where

$$m_{0,k} = \frac{1}{3} + \overline{m}_0 \cdot \overline{\alpha}_k, \;\; k = 1,\ 2,\ 3. \tag{20}$$

Equation (20) demonstrate that the quantities $m_{0,1}$, $m_{0,2}$ and $m_{0,3}$ can be regarded as the components of the vector $\overline{m}_0$, i.e., $\overline{m}_0$ can be expressed as:

$$\overline{m}_0 = \frac{2}{3}\sum_{k=1}^{3} m_{0,k}\overline{\alpha}_k \tag{21}$$

and the sum of $m_{0,k}$ (k = 1, 2, 3) is 1.

Inequalities (19) can be rewritten in a manner that emphasizes the upper and lower bounds of $m_{0,k}$.

$$\frac{(-1)^{h-1}}{2}\overline{m}_d \cdot \overline{\alpha}_k \leq m_{0,k} \leq 1 - \frac{(-1)^{h-1}}{2}\overline{m}_d \cdot \overline{\alpha}_k. \tag{22}$$

It can be demonstrated that the upper and lower bounds in (22), in the worst-case scenario, can be rewritten as follows:

$$m_{0,k}^{min} \leq m_{0,k} \leq m_{0,k}^{max} \tag{23}$$

where

$$m_{0,k}^{min} = \frac{1}{2}|\overline{m}_d \cdot \overline{\alpha}_k|, \quad k = 1, 2, 3 \tag{24}$$

$$m_{0,k}^{max} = 1 - \frac{1}{2}|\overline{m}_d \cdot \overline{\alpha}_k|, \quad k = 1, 2, 3. \tag{25}$$

Given that the upper bound of $m_{0,k}$ must be greater than or equal to the lower bound, it can be inferred from (24)–(25) that the following constraint applies to $\overline{m}_d$:

$$0 \leq |\overline{m}_d \cdot \overline{\alpha}_k| \leq 1. \tag{26}$$

Substituting (15) into (26) yields the following result:

$$\frac{2}{3}\left| v_{o,ref} \frac{\overline{\psi}_{ref} \cdot \overline{\alpha}_k}{\overline{v}_i \cdot \overline{\psi}_{ref}} \right| \leq 1, \quad k = 1, 2, 3. \tag{27}$$

It is possible to verify that the maximum voltage transfer ratio resulting from (27) is when $\overline{\psi}_{ref}$ is aligned with one of the vectors $\overline{\alpha}_k$ (k = 1, 2, 3):

$$\frac{\left| v_{o,ref} \right|}{|\overline{v}_i|} \leq \frac{3}{2}|cos\varphi_i| \tag{28}$$

where φ_i is the input power factor angle, assumed positive when the current lags the input voltage vector.

If the constraint (28) is satisfied, the matrix rectifier operates within the linear modulation range, and the modulation problem has at least one feasible solution. This implies that there exists at least one value of the zero-sequence component $\overline{m}_0$ that allows all duty cycles to remain within the interval [0, 1]. The optimal choice of $\overline{m}_0$ is not a straightforward matter and is discussed in the following section.

4. Space Vector Modulation

A technique that is widely known for the voltage modulation of power converters is SVM, which can also be developed for AC–DC matrix converters. According to this technique, the average value of the desired output voltage over a switching period is approximated with a sequence of different converter configurations.

Table 1 shows the possible states of an AC–DC matrix converter. The first column is the identification number of each configuration, the second column shows the bidirectional switches of Figure 1 that are turned on, and the third and fourth columns show the instantaneous values of $\overline{m}_1$ and $\overline{m}_2$. Finally, the remaining columns are the values of $\overline{m}_d$ and $\overline{m}_0$, calculated by means of (11) and (12). As can be seen, there are six active configurations, which produce a non-zero output voltage, and three zero configurations.

Figure 2 shows that the admissible values of $\overline{m}_d$ divide the plane into six sectors. Since the value of $\overline{m}_{d,ref}$ is known by means of (15), it is possible to identify two vectors, $\overline{m}_d^L$ and $\overline{m}_d^R$, which delimit the sector where $\overline{m}_{d,ref}$ is located. By definition, $\overline{m}_d^L$ lags behind $\overline{m}_d^R$. For example, if $\overline{m}_{d,ref}$ is in sector 1, $\overline{m}_d^L$ is $\frac{2}{3}(\overline{\alpha}_1 - \overline{\alpha}_2)$ and $\overline{m}_d^R$ is $\frac{2}{3}(\overline{\alpha}_1 - \overline{\alpha}_3)$.

Table 1. Configurations of the AC–DC matrix converter.

Conf. #	Switches	$\overline{m}_1$	$\overline{m}_2$	$\overline{m}_d$	$\overline{m}_0$
1	$S_{1,1}ON$ $S_{2,2}ON$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}(\bar{\alpha}_1-\bar{\alpha}_2)$	$\frac{1}{3}(\bar{\alpha}_1+\bar{\alpha}_2)$
2	$S_{1,1}ON$ $S_{2,3}ON$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}(\bar{\alpha}_1-\bar{\alpha}_3)$	$\frac{1}{3}(\bar{\alpha}_1+\bar{\alpha}_3)$
3	$S_{1,2}ON$ $S_{2,3}ON$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}(\bar{\alpha}_2-\bar{\alpha}_3)$	$\frac{1}{3}(\bar{\alpha}_2+\bar{\alpha}_3)$
4	$S_{1,2}ON$ $S_{2,1}ON$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}(\bar{\alpha}_2-\bar{\alpha}_1)$	$\frac{1}{3}(\bar{\alpha}_1+\bar{\alpha}_2)$
5	$S_{1,3}ON$ $S_{2,1}ON$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}(\bar{\alpha}_3-\bar{\alpha}_1)$	$\frac{1}{3}(\bar{\alpha}_1+\bar{\alpha}_3)$
6	$S_{1,3}ON$ $S_{2,2}ON$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}(\bar{\alpha}_3-\bar{\alpha}_2)$	$\frac{1}{3}(\bar{\alpha}_2+\bar{\alpha}_3)$
0_1	$S_{1,1}ON$ $S_{2,1}ON$	$\frac{2}{3}\bar{\alpha}_1$	$\frac{2}{3}\bar{\alpha}_1$	0	$\frac{2}{3}\bar{\alpha}_1$
0_2	$S_{1,2}ON$ $S_{2,2}ON$	$\frac{2}{3}\bar{\alpha}_2$	$\frac{2}{3}\bar{\alpha}_2$	0	$\frac{2}{3}\bar{\alpha}_2$
0_3	$S_{1,3}ON$ $S_{2,3}ON$	$\frac{2}{3}\bar{\alpha}_3$	$\frac{2}{3}\bar{\alpha}_3$	0	$\frac{2}{3}\bar{\alpha}_3$

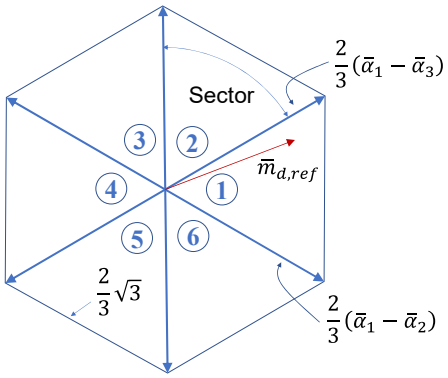


Figure 2. Admissible instantaneous values of $\overline{m}_d$ and repartition of the plane into six sectors.

The mean value of $\overline{m}_d$ over a switching period can be expressed as a linear combination of $\overline{m}_d^L$ and $\overline{m}_d^R$:

$$\overline{m}_{d,\,ref} = \delta^L \overline{m}_d^L + \delta^R \overline{m}_d^R \tag{29}$$

where δ^L and δ^R are numbers in the interval [0, 1], which must be interpreted as duty cycles.

Solving (29) for δ^L and δ^R yields the following expressions:

$$\delta^L = -\frac{\sqrt{3}}{2}\overline{m}_{d,ref} \cdot j\overline{m}_d^R \tag{30}$$

$$\delta^R = \frac{\sqrt{3}}{2}\overline{m}_{d,ref} \cdot j\overline{m}_d^L. \tag{31}$$

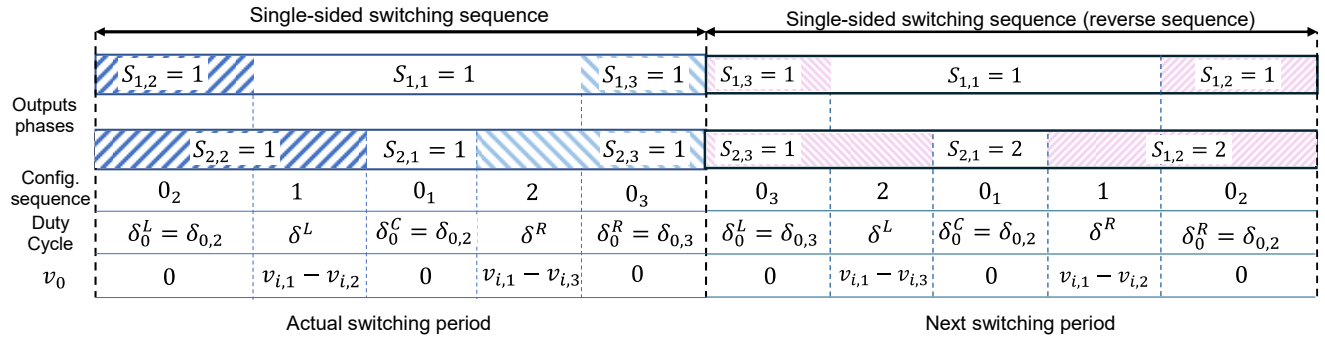
Once the application times of $\overline{m}_d^L$ and $\overline{m}_d^R$ are known, the remaining part of the switching period can be filled with the three zero vectors. In this way, two degrees of freedom are introduced. In fact, the three duty cycles $\delta_{0,1}$, $\delta_{0,2}$ and $\delta_{0,3}$ of the zero configurations 0_1, 0_2 and 0_3 must be chosen under the constraint that the sum of all duty cycles is equal to 1:

$$\delta_{0,1} + \delta_{0,2} + \delta_{0,3} + \delta^L + \delta^R = 1. \tag{32}$$

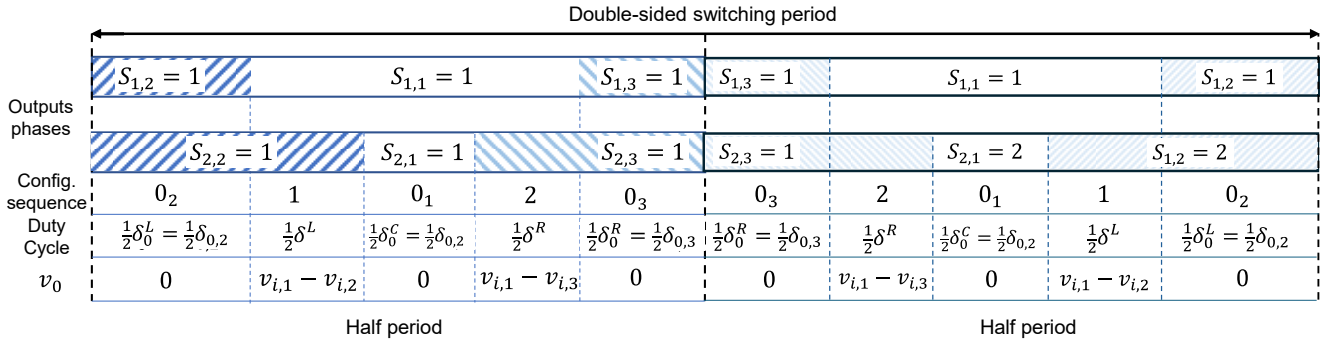
Table 2 illustrates the sequence of vectors utilized in the SVM, organized according to the sector number. It should be noted that there are only two distinct sequences of converter states that minimize the number of switch commutations.

These two sequences are inverse of one another. Table 2 identifies the sequences as c_1-c_2-c_3-c_4-c_5 and c_5-c_4-c_3-c_2-c_1, respectively. Both sequences include three zero configurations interspersed with two active configurations. The configuration c_3 is identical in both patterns and depends on the sector number of $\overline{m}_{d,ref}$. Given that $\overline{m}_{d,ref}$ has the same direction as the input current vector, it can be concluded c_3 can only be a zero vector, 0_1, 0_2 or 0_3, depending on which phase is conducting the maximum absolute value of the current. For example, when the highest current (absolute value) is observed in input phase 1, the current space vector is situated in sector 1, and configuration c_3 is 0_1, as documented in Table 2.

For the sake of completeness, Figure 3 depicts the typical single-sided and double-sided switching patterns of the converter when $\overline{m}_{d,ref}$ is in sector 1. If the switching pattern is double-sided, then the configuration sequence in the second half period is identical to that of the first half period but in reverse order. In this generic example, all three zero configurations are used. When the duty cycles of the zero vectors are equal, the modulation strategy is referred to as SVM 3Z. Similarly, it is possible to define other modulation strategies, such as SVM 2Z and SVM 1Z, that utilize a reduced number of zero configurations (see Table 3). The letters "L", "C" and "R" used in the names of the modulation strategies identify the position of the zero vectors in the switching pattern, namely, "Left", "Center", and "Right".



(**a**)



(**b**)

Figure 3. Switching patterns with three zero-voltage configurations when the vector $\overline{m}_d$ lies in sector 1: single-sided (**a**); or double-sided (**b**).

Table 2. Sequence of vectors for SVM (the reverse order is also possible).

	Vector sequence				
$\overline{m}_d$	0	$\overline{m}_d^L$	0	$\overline{m}_d^R$	0
Duty cycles	δ_0^L	δ^L	δ_0^C	δ^R	δ_0^R
	Configurations $c_1 - c_5$ of the vector sequence				
Sector number	c_1	c_2	c_3	c_4	c_5
1	0_2	1	0_1	2	0_3
2	0_1	2	0_3	3	0_2
3	0_3	3	0_2	4	0_1
4	0_2	4	0_1	5	0_3
5	0_1	5	0_3	6	0_2
6	0_3	6	0_2	1	0_1

Table 3. Space vector modulation strategies.

Modulation Strategy	Constraints	Zero Configurations Used in the Sequence
SVM 3Z	$\delta_0^L = \delta_0^C = \delta_0^R$	c_1, c_3, c_5
SVM 2Zlc	$\delta_0^L = \delta_0^C$, $\delta_0^R = 0$	c_1, c_3
SVM 2Zlr	$\delta_0^L = \delta_0^R$, $\delta_0^C = 0$	c_1, c_5
SVM 2Zrc	$\delta_0^C = \delta_0^R$, $\delta_0^L = 0$	c_3, c_5
SVM 1Zl	$\delta_0^C = \delta_0^R = 0$	c_1
SVM 1Zc	$\delta_0^L = \delta_0^R = 0$	c_3
SVM 1Zr	$\delta_0^L = \delta_0^C = 0$	c_5

5. Improvement in the Switching Losses

5.1. General Expression of the Switching Losses

The values (17) of the duty cycles of the switches are not sufficient to univocally identify a modulation strategy because it is still possible to choose different switching sequences, i.e., different turn-on and turn-off ordering of the switches.

In this paper, it is assumed that the same switching pattern is used for both output phases. Furthermore, it is assumed that during the first half of the switching period, each output phase is connected to the input phases in a predetermined order that depends on the amplitude of the input voltages, i.e., each output phase is firstly connected to the input terminal with the highest voltage, then to the one with the intermediate voltage, and finally to the one with the lowest voltage. In the second half of the switching period, the sequence is repeated in reverse order.

It is established that this switching pattern minimizes the switching losses of the converter, although it may have a slight detrimental impact on the harmonic content of the input and output currents. The following Section presents straightforward proof for the first converter leg, assuming that a four-step commutation is employed. Let us suppose that, in the first half of the switching period, the output pole voltage v_{o1} becomes sequentially equal to $v_{i,a}$, $v_{i,b}$ and $v_{i,c}$. The pattern is reversed in the second half of the switching period (double-sided switching pattern). The switching losses $P_{SW,1}$ of the first leg can be expressed as follows [30]:

$$P_{SW,1} = f_{SW}\tau_{tot}|i_o|\left(\left|v_{i,a} - v_{i,b}\right| + \left|v_{i,b} - v_{i,c}\right|\right) \tag{33}$$

$$\tau_{tot} = \tau_{on} + \tau_{off} + \tau_{rec} \tag{34}$$

where f_{SW} is the switching frequency, and τ_{tot} is a coefficient (with the dimension of time) that represents the energy loss due to switching action per unit of voltage and current. It can be expressed as the sum of three terms. The coefficients τ_{on} and τ_{off} are related to the energy loss process in the IGBTs during turn-on and turn-off, respectively. The coefficient τ_{rec} is related to the energy loss process in the diodes due to the reverse recovery currents during turn-off.

Applying the triangular inequality to (33) gives:

$$P_{SW,1} \geq f_{SW}\tau_{tot}|i_o|(|v_{i,a} - v_{i,c}|). \tag{35}$$

Inequality (35) becomes an equality only if $v_{i,a} \geq v_{i,b} \geq v_{i,c}$, or $v_{i,c} \geq v_{i,b} \geq v_{i,a}$, so P_{SW1} is minimum only if the input voltages of the switching pattern are ordered in descending or ascending order.

As can be seen from (35), the minimum power loss does not depend on the intermediate voltage under the assumption of an ordered pattern, so the switching losses do not change if the intermediate voltage is not included in the switching pattern. If the switching pattern does not contain the maximum or minimum voltages, the switching losses are further reduced because the voltage gap $|v_{i,a} - v_{i,c}|$ in (35) is replaced by $|v_{i,b} - v_{i,c}|$ or $|v_{i,a} - v_{i,b}|$, respectively.

In general terms, if the indices of the input voltages in descending order (top, medium and bottom) are given by the triplet (t, m, b), so that:

$$v_{i,t} \geq v_{i,m} \geq v_{i,b} \tag{36}$$

the switching losses of the whole converter can be expressed in the general case as follows:

$$\begin{aligned} &P_{SW,tot} = P_{SW,1} + P_{SW,2} = \\ &f_{sw}\tau_{tot}\ |i_o| \sum_{h=1}^{2} \left(|v_{i,t} - v_{i,m}|\varepsilon_{top,h} + |v_{i,m} - v_{i,b}|\varepsilon_{bot,h} \right) \end{aligned} \tag{37}$$

where the coefficient $\varepsilon_{top,h}$ is equal to 1 if the hth output pole voltage commutes from the maximum input voltage to another (lower) voltage level in the switching period. Conversely, if this transition does not exist, the coefficient is equal to 0. Similarly, the coefficient $\varepsilon_{bot,h}$ is 1 if the hth output pole voltage commutes to the minimum input voltage from another (higher) voltage level in the switching period. The four coefficients $\varepsilon_{top,h}$ and $\varepsilon_{bot,h}$ (h = 1, 2) are normally equal to 1, but suitable choices of $\overline{m}_0$ may result in up to two of them being set to zero. If all coefficients $\varepsilon_{top,h}$ and $\varepsilon_{bot,h}$ are 1, (37) becomes:

$$P_{SW,tot} = 2f_{sw}\tau_{tot}|i_o|(v_{i,t} - v_{i,b}). \tag{38}$$

If the output pole voltages are synthesized without using all input voltages, the switching losses decrease in comparison to (37), provided that the unused voltage is not the intermediate one, whose absence is ineffective.

5.2. Optimal Zero Sequence Component for a Reduction in the Switching Losses

A reduction in the switching losses is possible only when an output pole voltage is synthesized without using the maximum or the minimum input voltages $v_{i,t}$ and $v_{i,b}$. This occurs only when $m_{0,t}$ and $m_{0,b}$ are equal to the lower and upper bounds of the admissible ranges (23). Table 4 summarizes the four possible combinations, which will be examined subsequently.

In Case 1, $m_{0,t}$ is equal to $m_{0,t}^{min}$ and $m_{0,b}$ is equal to $m_{0,b}^{min}$. When this happens, two duty cycles, $m_{h^I,t}$ and $m_{h^{II},b}$, become zero (consequently, ε_{top,h^I} and $\varepsilon_{bot,h^{II}}$ are zero too). The indexes h^I and h^{II} can be found from (23) with $k = t$ and $k = b$, as shown in Table 5.

In Case 2-A, $m_{0,t}$ is equal to $m_{0,t}^{max}$ and a duty cycle, $m_{h^{III},t}$, becomes equal to 1.

Table 4. Values of the zero-sequence components.

	$m_{0,t}$	$m_{0,b}$
Case 1	$m_{0,t}^{min} = 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_t\rvert$	$m_{0,b}^{min} = 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_b\rvert$
Case 2-A	$m_{0,t}^{max} = 1 - 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_t\rvert$	$m_{0,b}^{min} = 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_b\rvert$
Case 2-B	$m_{0,t}^{min} = 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_t\rvert$	$m_{0,b}^{max} = 1 - 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_b\rvert$
Not applicable	$m_{0,t}^{max} = 1 - 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_t\rvert$	$m_{0,b}^{max} = 1 - 0.5\lvert\overline{m}_d \cdot \overline{\alpha}_b\rvert$

Table 5. Coefficients for Case 1, 2-A and 2-B.

Case 1	
$h^I = \begin{cases} 2 \; if \; sgn(\overline{m}_d \cdot \overline{\alpha}_t) \geq 0 \\ 1 \; otherwise \end{cases}$	$h^{II} = \begin{cases} 2 \; if \; sgn(\overline{m}_d \cdot \overline{\alpha}_b) \geq 0 \\ 1 \; otherwise \end{cases}$
Case 2-A	Case 2-B
$h^{III} = \begin{cases} 1 \; if \; sgn(\overline{m}_d \cdot \overline{\alpha}_t) \geq 0 \\ 2 \; otherwise \end{cases}$	$h^{IV} = \begin{cases} 1 \; if \; sgn(\overline{m}_d \cdot \overline{\alpha}_b) \geq 0 \\ 2 \; otherwise \end{cases}$

The index h^{III} can be found from (23) with $k = t$ (Table 5). Since $m_{h^{III},t}$ is 1, necessarily, the other duty cycles of the same output leg are forced to be zero, so the remaining condition $m_{0,b} = m_{0,b}^{min}$ in Table 5 is automatically satisfied for Case 2-A. This case corresponds to the conditions $\varepsilon_{top,h^{III}} = \varepsilon_{bot,h^{III}} = 0$.

Similarly, in Case 2-B, $m_{0,b}$ is equal to $m_{0,b}^{max}$, and a duty cycle $m_{h^{IV},b}$ becomes equal to 1. This case corresponds to the condition $\varepsilon_{top,h^{IV}} = \varepsilon_{bot,h^{IV}} = 0$.

Finally, the case where $m_{0,t}$ and $m_{0,b}$ are both one is not considered because these two constraints are usually incompatible with each other.

Once the values of $m_{0,t}$ and $m_{0,b}$ are known, the component $m_{0,m}$ can be calculated as a difference.

$$m_{0,m} = 1 - m_{0,t} - m_{0,b}. \tag{39}$$

The value of $m_{0,m}$ resulting from (39) has to comply with (23). By using (21), the zero sequence component $\overline{m}_0$ becomes

$$\overline{m}_0 = \frac{2}{3}(m_{0,t}\overline{\alpha}_t + m_{0,m}\overline{\alpha}_m + m_{0,b}\overline{\alpha}_b). \tag{40}$$

It is simple to show that that Case 2-A and Case 2-B are mutually exclusive. The explicit expression of $m_{0,m}$ deduced in Case 2-A is

$$m_{0,m} = \frac{1}{2}(|\overline{m}_d \cdot \overline{\alpha}_t| - |\overline{m}_d \cdot \overline{\alpha}_b|) \tag{41}$$

while in Case 2-B it is

$$m_{0,m} = \frac{1}{2}(|\overline{m}_d \cdot \overline{\alpha}_b| - |\overline{m}_d \cdot \overline{\alpha}_t|). \tag{42}$$

Since (41) and (42) are opposite to each other, one of them is definitely negative and does not comply with the lower bounds given by (23), which are positive.

In addition, it is possible to verify that the solutions of Case 2 exist for any input voltage only if the input current angle φ_i is in the range $[-\frac{\pi}{6}, \frac{\pi}{6}]$. A qualitative analysis is presented in Section 5.3.

In conclusion, only two modulation strategies in Table 4 reduce the switching losses. The first one corresponds to the choice of $\overline{m}_0$ resulting from Case 1 and exists for any value of the input power factor; the second one corresponds to the choice of $\overline{m}_0$ resulting from either Case 2-A or Case 2-B, but it exists only if $|\varphi_i| \leq \frac{\pi}{6}$.

5.3. Graphical Representation of the Switch State

If $\overline{m}_1$ (or $\overline{m}_2$) is plotted on the complex plane, it lies inside the triangular region depicted in Figure 4, which can be identified by considering all the admissible values of $\overline{m}_1$.

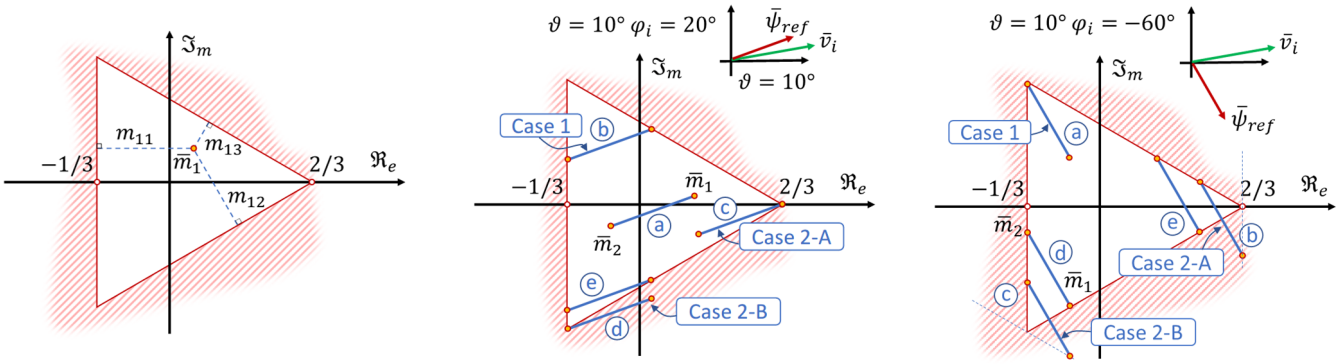


Figure 4. Geometrical representation of $\overline{m}_1$ and $\overline{m}_2$: (**a**) graphical meaning of $\overline{m}_1$; (**b**) typical positions of the segment connecting $\overline{m}_1$ and $\overline{m}_2$ with an input power factor greater than 0.866; (**c**) typical positions of the segment connecting $\overline{m}_1$ and $\overline{m}_2$ with an input power factor lower than 0.866.

Equation (17) demonstrates that the distances of $\overline{m}_1$ from the triangle sides are numerically equal to the duty cycles $m_{1,1}$, $m_{1,2}$ and $m_{1,3}$. Figure 4a gives a visual representation of this concept. Similarly, the distances of $\overline{m}_2$ from the triangle sides are the duty cycles $m_{2,1}$, $m_{2,2}$ and $m_{2,3}$. Consequently, when $\overline{m}_1$ (or $\overline{m}_2$) is situated on the triangle sides, at least one duty cycle is equal to zero, thereby reducing the number of switch commutations per period. Moreover, when $\overline{m}_1$ (or $\overline{m}_2$) is situated at a triangle vertex, one duty cycle is equal to 1, and the remaining duty cycles are zero.

According to (16), $\overline{m}_1$ and $\overline{m}_2$ turn out to be the endpoints of a segment that can be rigidly translated by changing $\overline{m}_0$, which is its midpoint. Figure 4b illustrates five different positions of the aforementioned segment, designated by the letters (a), (b), (c), (d) and (e). To draw Figure 4b, it is assumed that the phase angle of the input current φ_i and voltage vectors ϑ are, respectively, 20° and 10°. The maximum, intermediate and minimum voltages are, respectively, $v_{i,1}$, $v_{i,2}$ and $v_{i,3}$, i.e., (t, m, b) = (1, 2, 3).

In position (a), the segment does not come into contact with the triangle sides, and thus no commutation is avoided. Position (b) corresponds to Case 1 in Table 4, as both $m_{1,3}$ and $m_{2,1}$ are equal to zero.

In position (c), $\overline{m}_1$ coincides with a triangle vertex. The duty cycle $m_{1,1}$ is equal to 1, whereas $m_{1,2}$ and $m_{1,3}$ are both zero. This position is classified as Case 2-A in Table 4.

Similarly, position (d) corresponds to Case 2-B, since $m_{2,1} = 0$ $m_{2,2} = 0$ and $m_{2,3} = 1$. As anticipated, this operating condition is not feasible because $\overline{m}_1$ is not contained within the triangle.

Ultimately, position (e) leads to a feasible solution to the modulation problem, characterized by the fact that $m_{2,1}$ and $m_{1,2}$ are both zero. Nevertheless, this condition is not considered in Table 4 because it is suboptimal since zeroing $m_{1,2}$ means that the input intermediate voltage is not used to synthesize the pole voltage of the first output phase, and this does not lead to any reduction in the switching losses.

Figure 4c analyses the possible positions of segment $\overline{m}_1 - \overline{m}_2$ when the input power factor angle φ_i is −60°. While Case 1 still leads to a feasible configuration in position (a), Case 2-A and Case 2-B, corresponding to positions (b) and (c), produce two configurations that are not admissible. The other positions, (d) and (e), reduce the switching losses but as much as in Case 1.

5.4. Optimal Expression of the Switching Losses

If the zero-sequence component is chosen in every switching period according to Cases 1 or 2 of Table 4, the expression of the total power losses (37) can be simplified because some coefficients among $\varepsilon_{top,h}$ and $\varepsilon_{bot,h}$ (h = 1, 2) are zero. Specifically, ε_{top,h^I} and $\varepsilon_{bot,h^{II}}$ are both zero in Case 1, $\varepsilon_{top,h^{III}}$ and $\varepsilon_{bot,h^{III}}$ are zero In Case 2-A, and $\varepsilon_{top,h^{IV}}$ and $\varepsilon_{bot,h^{IV}}$ are zero in Case 2-B. It turns out that Case 1, 2-A or 2-B provide the same value of the switching losses, which can be calculated by means of (37):

$$\begin{aligned} P_{sw,tot} &= f_{sw}\tau_{tot}|i_o|\left(|v_{i,t} - v_{i,m}| + |v_{i,m} - v_{i,b}|\right) = \\ &= f_{sw}\tau_{tot}|i_o|(v_{i,t} - v_{i,b}) \end{aligned} \tag{43}$$

Therefore, all cases theoretically produce the same amount of switching losses. The average switching losses of the converter, calculated over a fundamental period of the input voltage, are as follows:

$$P_{sw,avg} = \frac{3\sqrt{3}}{\pi}\tau_{tot}f_{sw}|\overline{v}_i||i_o|. \tag{44}$$

Consequently, it is not possible to identify an optimal modulation strategy among Cases 1–2 in terms of switching losses. However, the solution corresponding to Case 1 is viable for any value of the input power factor. In contrast, Case 2 does not produce feasible solutions when the input power factor is lower than 0.866. For these reasons, Case 1 is considered the optimal solution in experimental validation.

6. Experimental Results

Experimental tests were carried out to verify the performance of the proposed modulation strategy. The basic scheme of the experimental setup is described in Figure 5.

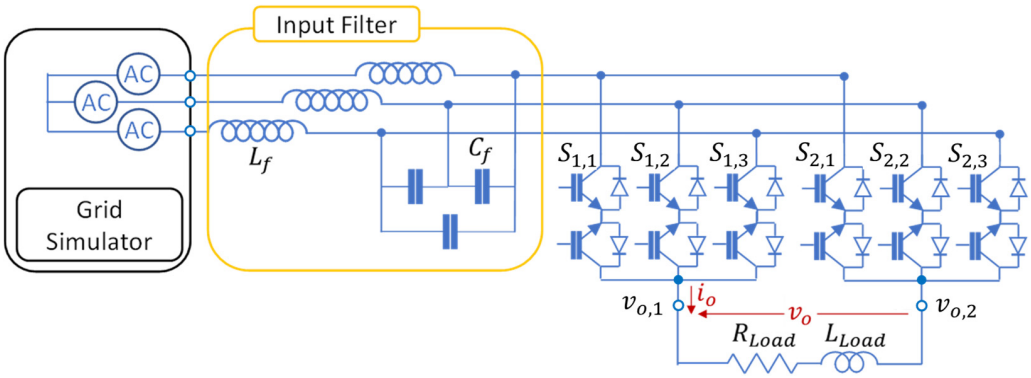


Figure 5. Basic scheme of AC–DC conversion system.

The converter is based on the IGBT module FM35E12KR3. The control algorithm was implemented on a fixed-point digital signal processor produced by Texas Instruments, Dallas, TX, USA (model TMS320F2812). The system parameters are shown in Table 6, and the four-step commutation strategy is used. Also, Figure 6 illustrates the curve of switching losses of IGBTs and diodes as a function of the direct current given a blocking voltage of 600 V and a junction temperature of 25 °C. The rated power of the prototype is about 12 kW. However, since the power module has never reached the commercialization stage, the converter is currently being used at about 20% of its rated power (2.5 kW). The effect of the commutations inevitably produces switching noise on the output voltage, and an output LC filter is commonly required in order to reduce the output current ripple (Appendix A). However, in this paper, the converter load is an ohmic inductive impedance because using a first-order low-pass filter allows one to accurately evaluate the effect of the modulation strategies on the distortion of the output current without the influence of complex filters.

Figure 7a shows the path in the complex plane of $\overline{m}_0$ and $\overline{m}_1$ for Case 1 when the voltage transfer ratio varies from 1.5 to 0.25. For a comparison, Figure 7b shows the path

of $\overline{m}_0$ and $\overline{m}_1$ in the complex plane for the conventional modulation strategies when the voltage transfer ratio is 1.5 and 0.75.

Table 6. Parameters of the experimental setup.

Supply	Input Filter	Converter	Load
v_i = 150 V ω_G = 2π 60 rad/s,	L_f = 0.2 mH C_f = 25 μF (Δ)	f_{SW} = 10 kHz, T_{dead} = 2 μs	R_{Load} = 22.6 Ω L_{Load} = 2.36 mH
DC collector current Repetitive peak collector current		$I_{C,nom}$ = 35 A @ T_{CASE} = 80 °C I_{CRM} = 70 A @ T_{CASE} = 80 °C, t_{PULSE} = 1 ms	
Collector emitter saturation voltage		V_{CEsat} = 1.70 V @ T_{VJ} = 25 °C $I_C = I_{C,nom}$, V_{GE} = 15 V	
Diode forward voltage		V_F = 1.65 V @ T_{VJ} = 25 °C, $I_C = I_{C,nom}$, V_{GE} = 15 V	
Collector-emitter voltages		V_{CES} = 1200 V	
Thermal resistance junction-to-case		$R_{th,JC,trans}$ = 0.60 K/W $R_{th,JC,diode}$ = 0.95 K/W	

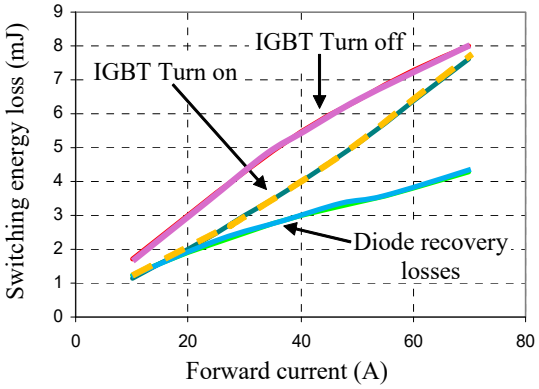


Figure 6. Switching losses of the converter IGBTs and diodes when the test voltage is 600 V, and the junction temperature is 25 °C.

At the maximum voltage transfer ratio (i.e., 1.5), the boundaries of linear modulation are clearly visible. The vector $\overline{m}_1$ follows a path that coincides with the sides of an equilateral triangle. In this situation, $\overline{m}_d$ reaches the maximum amplitude permitted for linear modulation. As the voltage transfer ratio decreases, $\overline{m}_1$ partially continues to follow the sides of the triangle. The position of $\overline{m}_1$ depends on the sequence of the switching states and the input voltages whereas $\overline{m}_0$ follows a path based on the rules of Table 5.

Figure 8 shows the behavior of the converter when eight distinct modulation strategies are employed with a voltage transfer ratio of 0.9 and a power factor of 1. The proposed modulation strategy is compared with seven space vector modulation strategies with a reduced number of commutations (Table 3). Figure 8 shows the waveforms of the input current i_{i1}, input voltage v_{i1}, output current i_o, output voltage v_o, and the waveforms of modulating signals of the first output leg $m_{1,1}$, $m_{1,2}$, $m_{1,3}$. As can be seen, the input voltage is in close phase alignment with the input current. The presence of the input filter capacitor results in a minimal phase lead in the line current, which is dependent on the voltage transfer ratio. In fact, the line current is the sum of the current through the capacitor C_f (Figure 5), which is $j\omega_G C_f \overline{v}_i$ at steady state, and the converter input current, $\overline{i}_i$. As the voltage transfer ratio decreases, the input converter current decreases while the capacitor current remains constant. Consequently, the phase lead of the line current tends to increase, reaching a theoretical value of 90 degrees when the input current $\overline{i}_i$ is zero (Appendix B). According to Figure 8, the power supplied to the load is approximately 2400 W, in contrast to a power consumption of roughly 2500 W. The phase voltage at the input filter is approximately 150 V_{peak}, with an electrical current of around 11 A_{peak}. The

capacitive current measures 4.5 A_{peak}, whereas the inductive current is approximately 12 A_{peak}. The reactive power consumed by the filter is approximately −1000 VAr. This causes the current to lead the voltage, yielding a power factor of around 0.9 for the source. The phase displacement of the input line current could be corrected by adjusting the phase angle of $\overline{\psi}_{ref}$ directly or through a specific control loop for the input power factor, as proposed by some authors [21,22]. However, this approach has not been adopted in this paper in order to avoid introducing further complexity to the assessment of the modulation strategy.

Figure 7. Paths in the complex plane of $\overline{m}_1$ and $\overline{m}_0$ for Case 1 (**a**) and for the conventional SVM strategies (**b**).

As illustrated in Figure 8, the modulation strategy corresponding to Case 1 consistently sets two modulating signals to zero. For high power factors, the zeroed modulating signals belong to two different output phases (Figure 4b). In contrast to the other modulation strategies, the symmetrical space vector modulation (SVM3Z) does not avoid any commutations. All other techniques reduce the number of commutations by alternatively clamping some duty cycles to either 0 or 1.

The efficiency of the AC–DC matrix converter controlled by using the eight different modulation strategies was experimentally measured by using a power meter Yokogawa WT2030. Figure 9 illustrates the efficiency and the converter losses as a function of the voltage transfer ratio under identical load conditions as those specified in Figure 8.

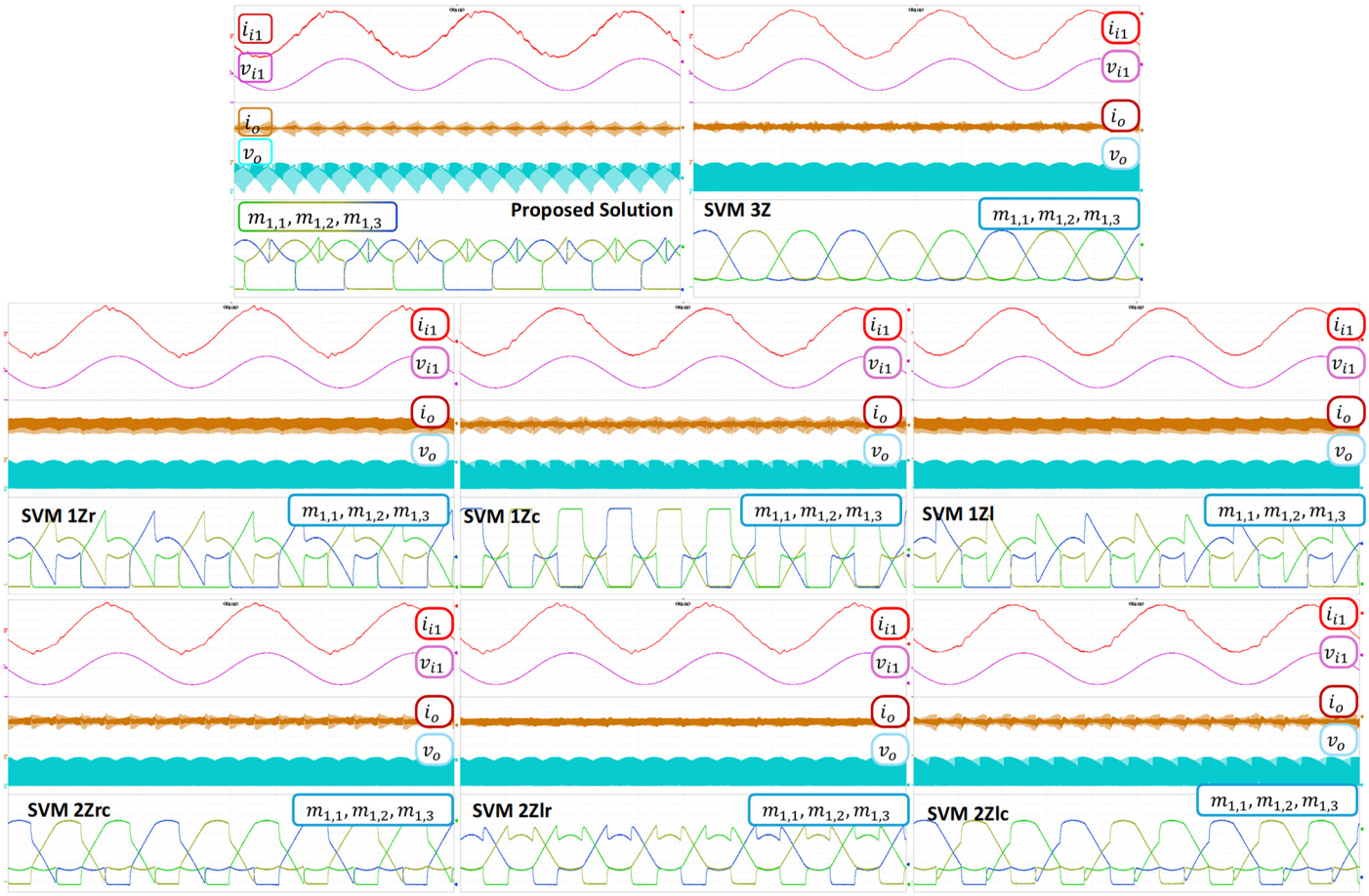


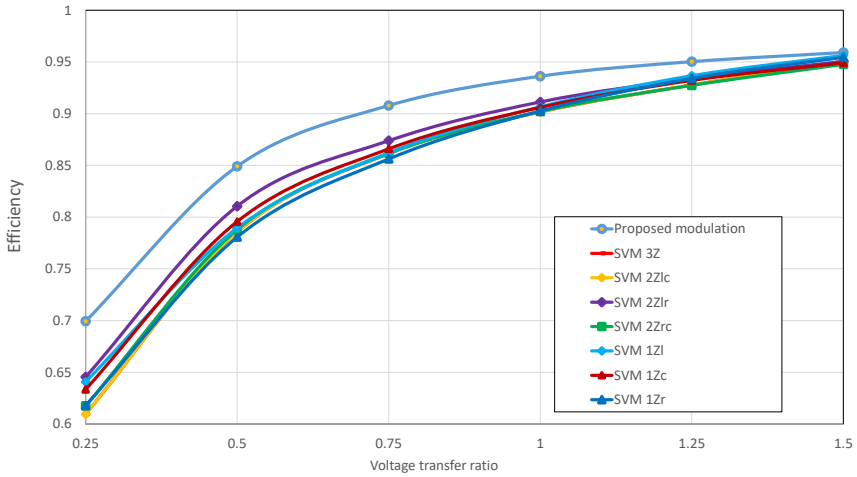
Figure 8. Experimental behaviors of the AC–DC matrix converter for different modulation strategies when the input power factor is 1 and the voltage transfer ratio is 0.9. Input current i_{i1} (5 A/div). Input voltage v_{i1} (100 V/div). Load current i_o (3 A/div). Output voltage v_o (50 V/div). Signals $m_{1,1}$, $m_{1,2}$, $m_{1,3}$ (0.125/div). Time scale (5 ms/div).

As can be observed, the efficiency of the modulation strategy derived from Case 1 is markedly superior to that of the other SVM strategies, particularly in the context of a low voltage transfer ratio. This finding is substantiated by the theoretical analysis. The efficiencies of the SVM 1Zr and SVM 1Zl techniques are largely comparable due to the symmetry inherent in these modulation techniques. Although the commutation losses are not identical instantaneously, the average value of the losses evaluated over the input voltage period is nearly identical. Similarly, the losses of SVM 2Zlc and SVM 2Zrc are nearly identical. The minor discrepancies can be attributed to the input filter losses and the disparate effects of dead times in the two scenarios.

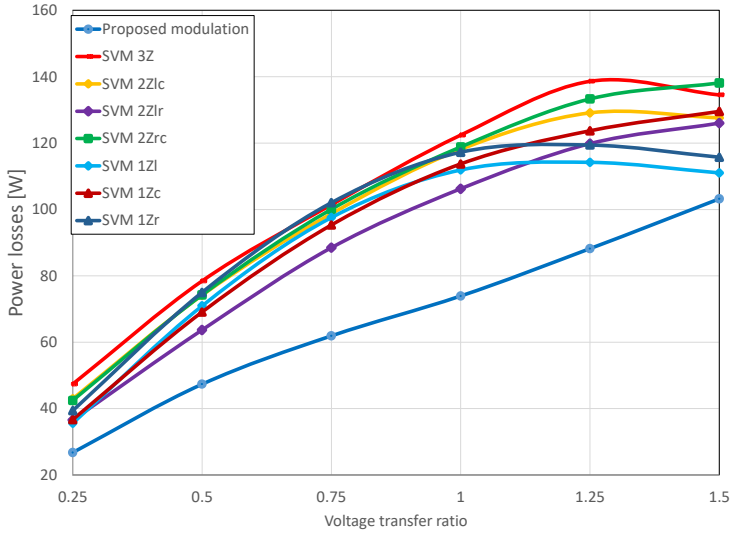
An approximate estimation of the converter losses can be obtained by comparing the input power and the efficiencies. If the proposed modulation strategy is compared with the SVM3Z, there is a loss reduction by nearly 24% when the voltage transfer ratio is maximum and by almost 44% when the voltage transfer ratio is 0.25. These losses include the switching and conduction losses of the converter, the input filter losses, and the losses related to the clamp circuit.

The efficiency of the converter depends on the switching and conduction losses of its components. In order to minimize the switching losses, a modulation technique must ensure that each output terminal is connected to the input terminals arranged in ascending or descending order of input voltages. Conventional methodologies do not adhere to this criterion, resulting in increased switching losses. In addition, the proposed theoretical analysis entails the computation of duty cycles for the bidirectional switches. The developed

modulation technique identifies the available degrees of freedom. For each output terminal, either the switch connected to the highest input voltage or the one associated with the lowest voltage does not commutate. This results in a further reduction in the switching losses.



(**a**)



(**b**)

Figure 9. Behavior of the AC–DC matrix converter for eight different modulation strategies when the input power factor is 1: efficiency (**a**); power losses (**b**).

Figure 10 shows the converter efficiencies with the modulation strategies of Table 4 for different values of the input power factor. All these results are obtained with the maximum possible voltage transfer ratio as defined by (28). The efficiency improvement of the proposed modulation strategy is consistent across all values of the input power factor.

Figures 11 and 12 illustrate the total harmonic distortion (THD) of the load current and the input current as a function of the voltage transfer ratio when the input power factor is unitary. The THD of the output current is defined as follows:

$$THD(i_o) = \sqrt{\frac{I_{o,RMS}}{I_{o,AVR}} - 1} \tag{45}$$

where $I_{o,RMS}$ and $I_{o,AVR}$ are the RMS and average values of the output current.

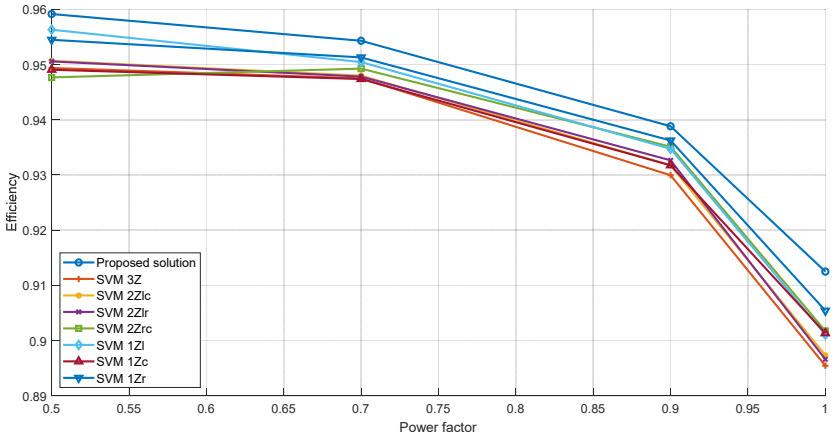


Figure 10. Efficiency of the AC–DC matrix converter for eight different modulation strategies when the voltage transfer ratio is maximum (1.5).

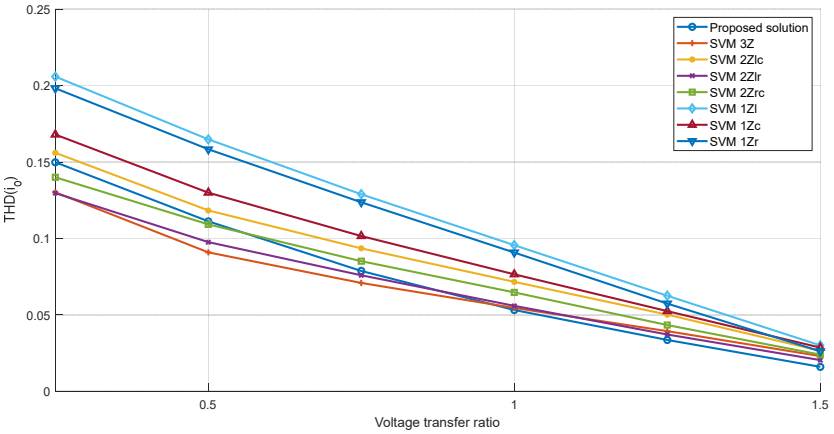


Figure 11. Measured THD of the output current as a function of the voltage transfer ratio when the input power factor is 1.

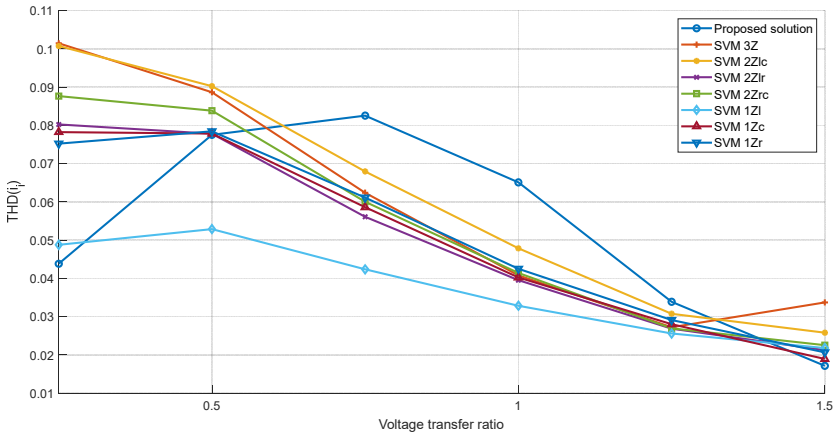


Figure 12. Measured THD of the input current as a function of the voltage transfer ratio when the input power factor is 1.

The proposed modulation strategy demonstrates the lowest distortion of the output and input current for high values of the voltage transfer ratio. Conversely, for values of the voltage transfer ratio between 0.5 and 1.25, the distortion of the input current is markedly elevated because of the reordering of the switching pattern. The trend of the output current THD in Figure 11 was experimentally determined and lacks a definitive theoretical rationale. The THD provides an integral representation of the current quality

over a fundamental period, which makes it challenging to ascertain the factors contributing to its reduction. However, it is worth noting that the proposed technique tends to reduce the variations in the potentials of the output terminals. This action may have a generally positive impact on the ripple of the load current.

Finally, the converter was tested in transient conditions. In Figure 13, the waveform of the input and output voltages and currents is depicted following three-step changes in the reference voltage transfer ratio, ranging from 0.75 to 1.5 in increments of 0.25. The figure also presents details of two transients of the output voltage and current. After each step, the current stabilizes within 1 ms. The output current is not regulated due to the deliberate absence of a control loop in the converter, which could adjust the voltage transfer ratio to account for noise and nonlinearity, potentially impacting the evaluation of modulation techniques.

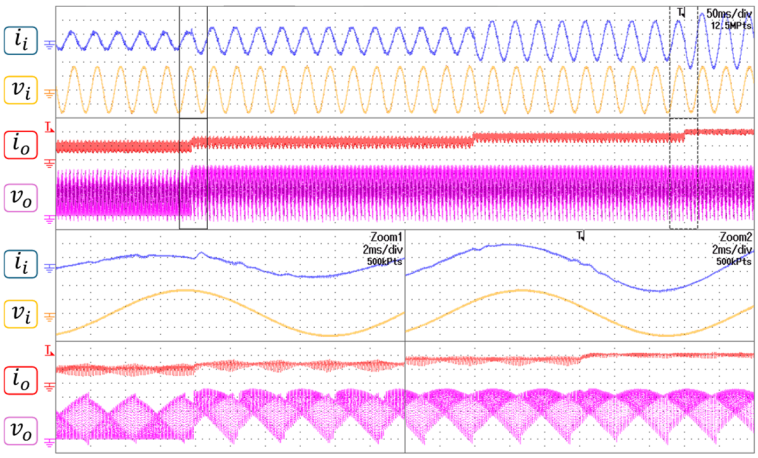


Figure 13. Transient behavior of the converter during three-step changes of the voltage transfer ratio (0.75, 1. 1.25, 1.5). From top to bottom: input current (5 A/div), input voltage (100 V/div), output current (5 A/div), output voltage (80 V/div).

7. Conclusions

This paper presents a comprehensive methodology for evaluating the performance of three-phase AC–DC matrix converters. A modulation strategy that minimizes switching losses was identified. This strategy reduces switching losses to approximately 24% in comparison to the space vector modulation that employs three equally spaced zero vectors at the maximum voltage transfer ratio. A substantial body of experimental evidence substantiates the viability and efficacy of the proposed approach.

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Conflicts of Interest: Author Riccardo Testa was employed by the company OCEM Power Electronics. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Appendix A Design of the Output Filter

In practical applications, an LC filter is often used to improve the quality of the output voltage. The inclusion of the capacitor significantly reduces the load current ripple, but also introduces an additional variable in the problem.

To size an LC filter, it is essential to estimate the ripple of the output current and voltage. For a preliminary calculation, it can be assumed that the filter requirements are expressed in terms of the voltage distortion across the capacitor (load voltage) and the peak-to-peak current ripple at the switching frequency through the filter inductance.

The transfer function $H(f)$ of the LC filter between the load voltage and the converter output voltage is a second-order filter. Referring to Figure A1, assuming that the switching frequency significantly exceeds the resonance frequency f_R, the expression for $H(f)$ can be estimated as follows:

$$H(f) = \frac{1}{\sqrt{\left[1 - \left(\frac{f}{f_R}\right)^2\right]^2 + \left(\frac{2\pi f L_o}{R_{load}}\right)^2}} \cong \left(\frac{f_R}{f}\right)^2 \tag{A1}$$

where R_{load} is the load resistance, L_o is the filter inductance, C_o is the filter capacitance and the resonant frequency f_R is defined as follows:

$$f_R = \frac{1}{2\pi\sqrt{L_o C_o}}. \tag{A2}$$

The output voltage distortion squared can be written as a function of the voltage harmonics $V_{load,k}$ of v_{load} $(k \geq 1)$, and the voltage harmonics $V_{o,k}$ of v_o $(k \geq 1)$:

$$D^2 = \frac{\sum_{k=1}^{\infty} V_{load,k}^2}{V_{load,0}^2} = \frac{\sum_{k=1}^{\infty} H_k^2 V_{o,k}^2}{V_{load,0}^2} \tag{A3}$$

where

$$H_k = H(2\pi k f_{SW}). \tag{A4}$$

An upper limit for the distortion can be determined with the following chain of inequalities:

$$D^2 = \frac{\sum_{k=1}^{\infty} H_k^2 V_{o,k}^2}{V_{load,0}^2} \leq \frac{H_1^2 \sum_{k=1}^{\infty} V_{o,k}^2}{V_{load,0}^2} = H_1^2 \frac{V_{o,rms}^2 - V_{load,0}^2}{V_{load,0}^2} \leq H_1^2 \left(\frac{3V_i^2}{V_{load,0}^2} - 1\right) \tag{A5}$$

The last inequality is justified by the fact that the output voltage v_o is either equal to one of the input line-to-line voltages $\left(\sqrt{3}V_i\right)$ or zero. Therefore, given a maximum value for D, it is possible to estimate a lower bound for the product $L_o C_o$.

$$L_o C_o \geq \frac{1}{4\pi^2 f_{SW}^2 D_{max}^2} \left(\frac{3V_i^2}{V_{load,0}^2} - 1\right) \tag{A6}$$

To estimate the current ripple, it can be presumed that the voltage across the capacitor remains nearly constant, so the inductor current is given by the following equation:

$$L_o \frac{di_o}{dt} = v_o - V_{load,0} \tag{A7}$$

An upper limit for the current fluctuation may be established under the assumption that the voltage v_o is constantly equal to the maximum input line-to-line voltage, $\sqrt{3}V_i$, for the whole switching period T_{SW} (worst case scenario):

$$\Delta i_{o,max} = \frac{\left(\sqrt{3}V_i - V_{load,0}\right) T_{SW}}{L_o}. \tag{A8}$$

In order to prevent the current fluctuation from exceeding the limit, it is typically necessary for $\Delta i_{0,max}$ to be a given fraction ϵ of the permissible direct current through the static switches.

$$L_o \geq \frac{\left(\sqrt{3}V_i - V_{load,0}\right) T_{SW}}{\epsilon I_{F,max}} \tag{A9}$$

The values of L_o and C_o can be determined from commercial specifications by fulfilling constraints (A6) and (A9).

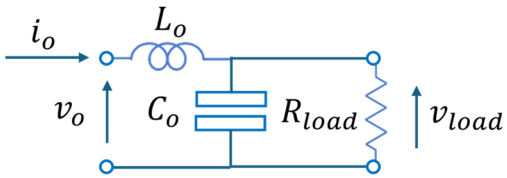

Figure A1. Output LC filter.

Appendix B Design of the Input Filter

The matrix rectifier requires an LC input filter to smooth the input current. A simplified design procedure is reported hereafter with reference to Figure A2.

Given the desired output power P_o and the converter efficiency η, the input power P_i is as follows:

$$P_i = \frac{P_o}{\eta}. \tag{A10}$$

The inductor current $\bar{I}_g$ is a function of the lag angle φ_i of the input current and the peak value of the input phase voltage V_i:

$$\bar{I}_g = j\omega_G C_f V_i + \frac{2}{3}\frac{P_i}{V_i \cos\varphi_i} e^{-j\varphi}. \tag{A11}$$

The filter inductance must be chosen so that its voltage drop is a fraction ϵ' of the input voltage. This poses an upper limit to the filter inductance.

$$\omega_G L_f I_g \leq \epsilon' V_i \tag{A12}$$

The filter capacitor is chosen so that the resonance frequency is much smaller than the switching frequency. This poses an upper limit to the filter capacitance.

$$\frac{1}{2\pi\sqrt{L_f C_f}} \ll \frac{1}{T_{SW}} \tag{A13}$$

Finally, it is necessary to ensure that the reactive power of the LC filter does not reduce the power factor significantly:

$$Q_g = \frac{3}{2}\omega_G L_f I_g^2 + \frac{3}{2}\omega_G C_f V_i^2 < \tan\varphi_{max} P_i \tag{A14}$$

where φ_{max} is the maximum displacement angle.

For the design of the prototype, whose parameters are reported in Table 6, the values of ϵ' is 1% and $\cos\varphi_{max}$ is 0.9.

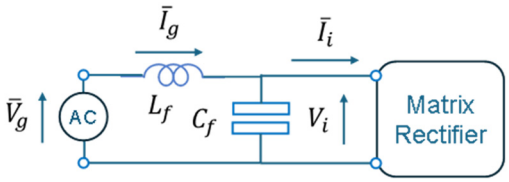

Figure A2. Input LC filter.

References

1. Mao, H.; Lee, C.; Boroyevich, D.; Hiti, S. Review of high performance three-phase power-factor correction circuits. *IEEE Trans. Ind. Electron.* **1997**, *44*, 437–446.
2. Kolar, J.W.; Friedli, T. The essence of three-phase PFC rectifier systems. In Proceedings of the 33rd International Telecommunications Energy Conference (INTELEC), Amsterdam, The Netherlands, 9–13 October 2011; pp. 1–27.
3. Hartmann, M.; Ertl, H.; Kolar, J.W. Current control of three-phase rectifier systems using three independent current controllers. *IEEE Trans. Power Electron.* **2013**, *28*, 3988–4000. [CrossRef]
4. Singh, B.; Singh, B.N.; Chandra, A.; Al-Haddad, K.; Pandey, A.; Kothari, D.P. A review of three-phase improved power quality AC–DC converters. *IEEE Trans. Ind. Electron.* **2004**, *51*, 641–660. [CrossRef]
5. Guo, B.; Wang, F.; Aeloiza, E. A novel three-phase current source rectifier with delta-type input connection to reduce the device conduction loss. *IEEE Trans. Power Electron.* **2016**, *31*, 1074–1084. [CrossRef]
6. Rajendran, G.; Vaithilingam, C.A.; Misron, N.; Naidu, K.; Ahmed, R. Voltage Oriented Controller Based Vienna Rectifier for Electric Vehicle Charging Stations. *IEEE Access* **2021**, *9*, 50798–50809. [CrossRef]
7. Zhang, Q.; Jiang, W.; Hu, Y.; Wang, J. An Easy-Implemented Pulsewidth Modulation Method for Vienna Rectifier with Minimized Current Distortion Including Overmodulation Operation. *IEEE J. Emerg. Sel. Top. Power Electron.* **2024**, *12*, 2639–2650. [CrossRef]
8. Dutra, A.D.E.; Vitorino, M.A.; Corrêa, M.B.D.R. A Survey on Multilevel Rectifiers With Reduced Switch Count. *IEEE Access* **2023**, *11*, 56098–56141. [CrossRef]
9. Kolar, J.W.; Friedli, T. The Essence of Three-Phase PFC Rectifier Systems—Part I. *IEEE Trans. Power Electron.* **2013**, *28*, 176–198. [CrossRef]
10. Friedli, T.; Hartmann, M.; Kolar, J.W. The Essence of Three-Phase PFC Rectifier Systems—Part II. *IEEE Trans. Power Electron.* **2014**, *29*, 543–560. [CrossRef]
11. Holmes, D.G.; Lipo, T.A. Implementation of a controlled rectifier using AC-AC matrix converter theory. *IEEE Trans. Power Electron.* **1992**, *7*, 240–250. [CrossRef]
12. García-Gil, R.; Espí, J.M.; Dede, E.J.; Sanchis-Kilders, E. A bidirectional and isolated three-phase rectifier with soft-switching operation. *IEEE Trans. Ind. Electron.* **2005**, *52*, 765–773. [CrossRef]
13. Yan, Z.; Zhang, K.; Li, J.; Wu, W. A novel absolute value logic SPWM control strategy based on de-re-coupling idea for high frequency link matrix rectifier. *IEEE Trans. Ind. Inform.* **2013**, *9*, 1188–1198. [CrossRef]
14. Carvalho, E.L.; Blinov, A.; Emiliani, P.; Chub, A.; Vinnikov, D. Three-phase bidirectional isolated AC–DC matrix-converter with full soft-switching range. *IEEE Access* **2023**, *11*, 119270–119283. [CrossRef]
15. Mahmud, T.; Gao, H. A comprehensive review on matrix-integrated single-stage isolated MF/HF converters. *Electronics* **2024**, *13*, 237. [CrossRef]
16. Korkh, O.; Blinov, A.; Vinnikov, D.; Chub, A. Review of isolated matrix inverters: Topologies, modulation methods and applications. *Energies* **2020**, *13*, 2394. [CrossRef]
17. Singh, A.K.; Jeyasankar, E.; Das, P.; Panda, S.K. A matrix-based nonisolated three-phase AC–DC rectifier with large step-down voltage gain. *IEEE Trans. Power Electron.* **2017**, *32*, 4796–4811. [CrossRef]
18. Metidji, R.; Metidji, B.; Mendil, B. Design and implementation of a unity power factor fuzzy battery charger using an ultrasparse matrix rectifier. *IEEE Trans. Power Electron.* **2013**, *28*, 2269–2276. [CrossRef]
19. You, K.; Xiao, D.; Rahman, M.F.; Uddin, M.N. Applying reduced general direct space vector modulation approach of AC-AC matrix converter theory to achieve direct power factor controlled three-phase AC-DC matrix rectifier. *IEEE Trans. Ind. Appl.* **2014**, *50*, 2243–2257. [CrossRef]
20. Kim, J.-C.; Kwak, S.; Kim, T. Power factor control method based on virtual capacitors for three-phase matrix rectifiers. *IEEE Access* **2019**, *7*, 12484–124949. [CrossRef]
21. Kim, J.-C.; Kwak, S. Direct power control method with minimum reactive power reference for three-phase AC-to-DC matrix rectifiers using space vector modulation. *IEEE Access* **2019**, *7*, 67515–67525. [CrossRef]
22. Kim, J.-C.; Kim, D.; Kwak, S.-S. Direct power-based three-phase matrix rectifier control with input power factor adjustment. *Electronics* **2019**, *8*, 1427. [CrossRef]
23. Fang, F.; Li, Y. An Improved SVM strategy to reduce DC current ripple for AC–DC matrix converter. *IEEE Trans. Ind. Appl.* **2021**, *57*, 570–579. [CrossRef]
24. Nguyen, T.L.; Lee, H.H. An enhanced control strategy for AC–DC Matrix converters under unbalanced grid voltage. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1718–1727. [CrossRef]

25. Nguyen, T.L.; Lee, H.H. Simplified model predictive control for AC/DC matrix converters with active damping function under unbalanced grid voltage. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 2907–2917. [CrossRef]
26. Fang, F.; Tian, H.; Li, Y. Finite control set model predictive control for AC–DC matrix converter with virtual space vectors. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 616–628. [CrossRef]
27. Rodriguez, J.; Rivera, M.; Kolar, J.W.; Wheeler, P.W. A review of control and modulation methods for matrix converters. *IEEE Trans. Ind. Electron.* **2012**, *59*, 58–70. [CrossRef]
28. Casadei, D.; Serra, G.; Tani, A. Reduction of the input current harmonic content in matrix converters under input/output unbalance. *IEEE Trans. Ind. Electron.* **1998**, *45*, 401–411. [CrossRef]
29. Casadei, D.; Serra, G.; Tani, A.; Zarri, L. Matrix converter modulation strategies: A new general approach based on space-vector representation of the switch state. *IEEE Trans. Ind. Electron.* **2002**, *49*, 370–381. [CrossRef]
30. Helle, L.; Larsen, K.; Jorgensen, A.; Munk-Nielsen, S.; Blaabjerg, F. Evaluation of modulation schemes for three-phase to three-phase matrix converters. *IEEE Trans. Ind. Electron.* **2004**, *51*, 158–171. [CrossRef]