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Breakdown-Voltage Degradation Under AC Stress of Thick SiO2 Capacitors for Galvanic Insulation

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Breakdown-voltage degradation under AC stress of thick SiO_2 capacitors for galvanic insulation

Federico Giuliano, Susanna Reggiani, Elena Gnani, Antonio Gnudi, Mattia Rossetti, Riccardo Depetro

***Abstract*— High-voltage dielectric breakdown of thick amorphous silicon-dioxide capacitors for galvanic insulation have been recently investigated showing a significant difference under DC and AC stresses. The impact-ionization generation is expected to be the dominant mechanism for thicknesses larger than 1 μm. A significant degradation of the breakdown voltage is observed for AC stress, which requires a focused TCAD-based investigation to fully understand the involved physical mechanisms. Accurate TCAD predictions of the measured leakage current allow to validate the proposed model gaining the detailed understanding of the device breakdown regime.**

***Index Terms*— Silicon oxide; Insulators; Reliability; TEOS;**

I. Introduction

Silicon oxide metal-insulator-metal (MIM) capacitors, embedded in the back-end inter-level dielectric layers, have been recently used for analog and RF applications in integrated circuits [1], [2]. Thetraethyl-orthosilicate (TEOS) oxide is usually adopted as back-end dielectric, but the material intrinsic defectivity and the large applied biases give rise to leakage currents which are responsible for degradation and failure [3]. The complexity of the transport features in such kind of material led to the need of a TCAD-based comprehensive model, which was recently developed to predict the current characteristics up to the avalanche onset [4]. The main physical mechanisms, such as charge injection at the contacts and trapping mechanisms from defects in the bulk, were taken into account and properly modeled in the TCAD setup. The model was extended in order to account for the impact-ionization generation over different stress conditions in [5]. The characterization and numerical analysis of the breakdown under DC-stress conditions in MIM capacitors with different thicknesses was carried out in [6], clearly showing that the explanation of the DC-stress measured data requires also the realistic description of the 3-D structure of the device. In particular, the breakdown field is substantially modulated by the electric-field and trapped-charge distribution in the proximity of the top-electrode corner.

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It is thus relevant to extend the proposed analysis to the AC stress condition, as it is a required validation of the modeling methodology, but also represents a realistic operating bias showing unexpected phenomena. In this work the TCAD model recently developed for thick amorphous TEOS SiO_2 is applied to predict the anomalous degradation of the breakdown under AC stress conditions. To this purpose, TCAD simulations have been carried out and compared to the experimental results under both DC and AC stress conditions in order to fully understand the observed behavior.

II. AC analyses at different oxide thicknesses

Following [4]–[6], the same simulation setup for the TEOS oxide is adopted here. The full vertical stack of the MIM structure is accounted for by assuming the fully extended bottom electrode and a circular electrode on top. An ideal insulator is placed on top of the structure to emulate the passivation layers. Simulations are carried out by using a 2-D domain for the radial cross-section of the device and cylindrical coordinated to fully represent the 3-D structure. The voltage is intended applied to the top electrode with the bottom electrode grounded. As a preliminary analysis, the TCAD approach has been validated against experiments performed under a square-wave (AC stress) for a MIM capacitor with $t_{OX} = 0.9\,\mu$m.

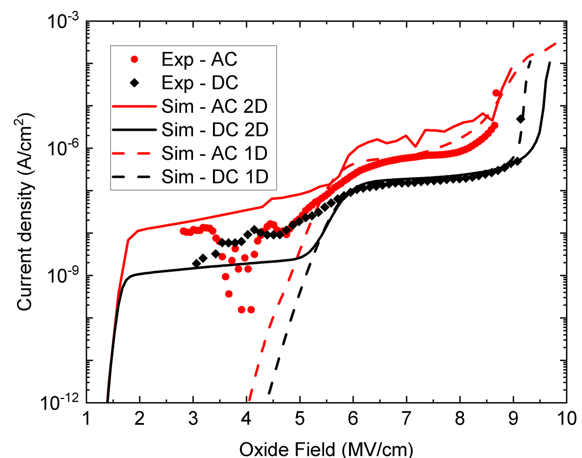

Fig. 1. Current density as a function of the oxide field up to the breakdown for different stress conditions. Experiments are compared with simulations at $t_{OX} = 0.9\,\mu$m for AC and DC stresses. Symbols: experiments. Continuous lines: Simulations carried out on the 2-D structure. Dashed lines: Simulations carried out on a 1-D test structure.

In Fig. 1, the TCAD simulations of the current density versus the oxide field, calculated as the ratio between the applied peak voltage and the oxide thickness, are compared against measured data at $T = 25\,^{\circ}\mathrm{C}$ under AC and DC stresses. Concerning the AC stress, the results have been extracted taking the current at the voltage peak of each positive half-wave of the signal, thus including only the injection current and not the displacement current. The limited increase of the current in the intermediate-field portion of the characteristics between 2 and 5 MV/cm is due to the peripheral current contribution at the corner of the structure. The comparison with 1-D simulations carried out on a simple parallel-plate capacitor with equivalent geometry shows current levels in the high-field portion of the characteristics in nice agreement with 2-D simulations for both stress conditions, whereas no 1-D current contribution is observed in the intermediate-field portion. In the overall, the AC and DC characteristics show a very similar behavior: the limited increase of the current in the high-field regime can be ascribed to charge trapping effects. Moreover, the breakdown field for both the DC and the AC stresses, extracted when a large current gradient is observed in the simulated curves, correctly captures the experiments in Fig. 3.

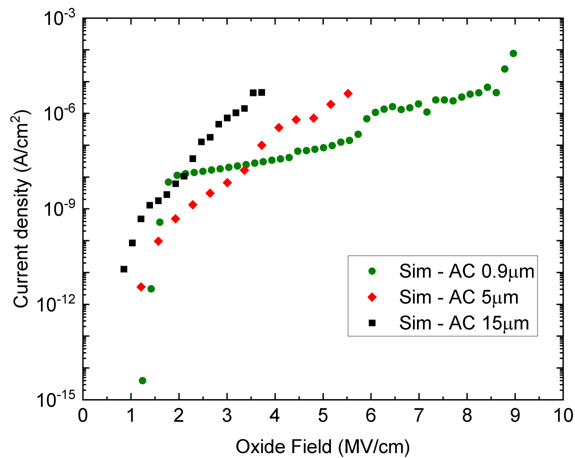

Fig. 2. TCAD results of the current density as a function of the oxide field up to the breakdown for the oxides with thickness $0.9\,\mu$m, $5\,\mu$m and $15\,\mu$m under an AC stress.

In addition, the simulations of the current density as a function of the oxide field for devices with different thickness during AC stress are reported in Fig. 2. It can be noted that the thicker oxide cases show a completely different behavior with respect to the thinner one ($t_{\mathrm{OX}} = 0.9\,\mu$m). An anticipated breakdown is clearly observed, the charge trapping effects show a current increase scaled to lower oxide fields, and the corner effect takes place for a much more limited field range. The oxide with thickness $5\,\mu$m shows an intermediate behavior between the thick and the thin one. The much more abrupt onset of the avalanche breakdown of the thicker oxide with respect to the thinner one might be ascribed to very different spatial distributions of the trapped charges within the bulk of the oxide, in particular in the proximity of the top metal corner. It is expected that a larger amount of trapped charges,

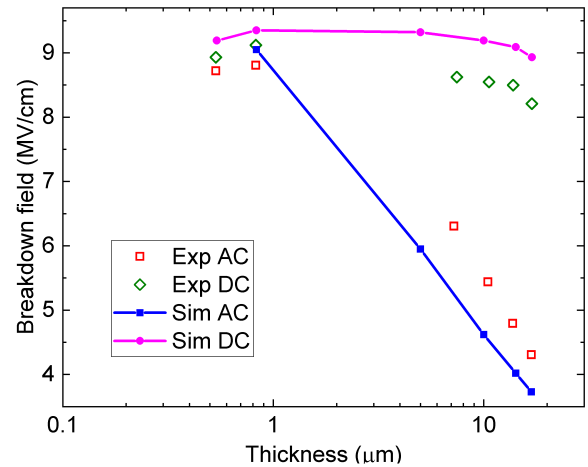

Fig. 3. Breakdown field as a function of the oxide thickness for samples with thicknesses up to $17\,\mu$m under AC and DC stresses. Dots: experiments. Lines and dots: Simulations.

caused by electron injection during the negative half-wave, leads to a greater electric field in the corner region during the positive half-wave and thus to a less smooth behavior of the avalanche onset. The predicted breakdown fields as a function

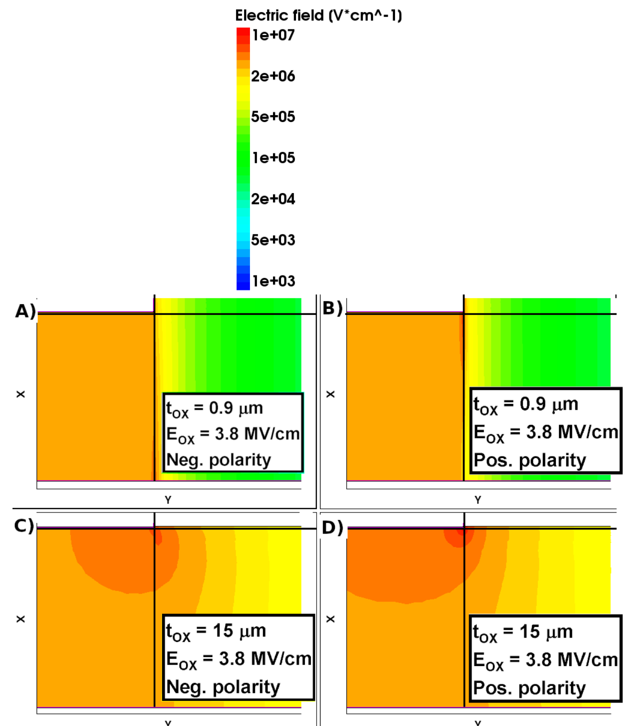

Fig. 4. Electric field within the oxide layer for the oxides with thicknesses: $t_{\mathrm{OX}} = 0.9\,\mu$m (top) and $t_{\mathrm{OX}} = 15\,\mu$m (bottom) at positive and negative polarity during the AC stress. X and Y axes have arbitrary units. The same scale is used on every Y axis, while different scales have been used for the X axes due to the different thicknesses.

of the oxide thickness for the AC stresses are reported in Fig. 3 compared with experiments along with the DC stress cases. Even if slight differences are found with respect to the experimental data, the overall dependence on the oxide thickness is fairly captured by simulations in a wide range

of thicknesses and for both stress conditions. This is a clear indication that the most relevant physical mechanisms have been taken into account.

An analysis of the physical quantities such as the electric field and the trapped charge across the devices has been carried out through the TCAD results using the devices with thicknesses $0.9\,\mu$m and $15\,\mu$m. To this purpose, the electric field during the AC stress at different polarities and for different thicknesses is shown in Fig. 4. The same scale is used on the Y axis of the different devices, while different scales have been used for the X axes due to the different thicknesses. In order to fairly compare the two thicknesses, the same electric field has been used, choosing the value of $E_{\rm OX} = 3.8$ MV/cm which is in the proximity of the breakdown of the thick oxide (see Fig. 1). The electric field profile of the thinner oxide resembles that of a 1D parallel-plate capacitor for both the negative and positive polarity (Fig. 4, plots A and B). The high field region around the corner sharply decreases along the Y axis. Differently, in the thicker oxide, a geometry-related effect can be noted: the high-field region around the corner extends in a wider region for both polarities (Fig. 4, plots C and D). The electric field is still in the order of 1 MV/cm at several microns of distance from the corner along the Y axis. In addition, it can be noted that the electric field in the proximity of the corner is larger during the positive half-wave than during the negative half-wave due to a significant negative trapped charge in the proximity of the top metal corner.

In order to further investigate this aspect, in Fig. 5, the electric field profile along the X-axis cut line indicated in Fig. 4 is reported in the case of the thick oxide ($t_{\rm OX} = 15\,\mu$m). During the positive stress, the electric field peak at the top metal corner is wider than during the negative stress, exceeding the intrinsic breakdown strength of SiO_2. It is a hint that the breakdown is driven by the positive half-wave stress: the top metal, and thus the region in the proximity of the corner acts as the anode during the positive half-wave, thus featuring an increase of the electric field. During the negative half-wave, on the contrary, the high electric field region is in the proximity of the bottom metal, and it is reduced near the top metal which now acts as a cathode. However, being the bottom metal a simple plane contact, the increase of the electric field is limited and not enhanced by the presence of a corner, thus the electric field cannot be high enough to trigger the onset of the breakdown.

In Fig. 6, the charge trapped during the AC stress at different polarities and for thicknesses $0.9\,\mu$m and $15\,\mu$m is shown. In the thin-oxide case (Fig. 6, plots A and B), trap distributions are almost uniformly charged through the entire thickness of the insulator in a region of limited extension around the top metal corner. On the contrary, in the thick-oxide case (Fig. 6, plots C and D), the traps are substantially empty over a great portion of the oxide thickness, and there is a significant trapped charge density only in the proximity of the top metal corner.

The distribution of the charged traps is further highlighted in Fig. 7, where the trapped charge density is plotted against the normalized position in the X axis along the vertical black lines of Fig. 4, where position 1 corresponds to the top metal position for both $t_{\rm OX} = 0.9\,\mu$m and $t_{\rm OX} = 15\,\mu$m. We have to point out that during each half-wave the charge is trapped in a region of limited thickness around the cathode. This trapping length is in the order of $\approx 0.4\,\mu$m, a significant fraction the total thickness of the thin oxide. This means that the charged defects in thin oxide are distributed approximately in a uniform way along the entire thickness of the oxide, as shown with the dashed lines in Fig. 7, leading to a limited increase of the electric field. As far as the thicker oxide is concerned, this trapping length represents only a small fraction of the total thickness of the device, implying that defects are almost empty throughout the oxide except in a small region around

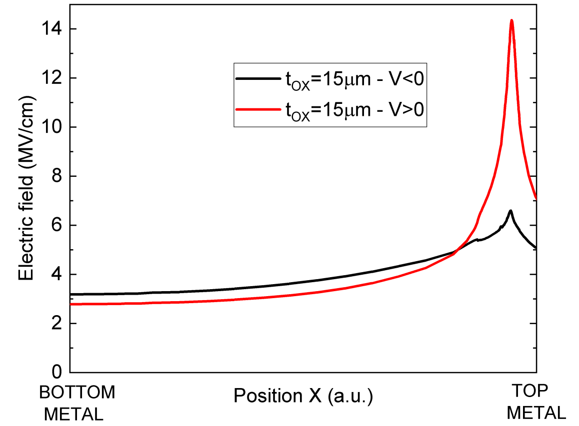

Fig. 5. Electric field along the X axis for the oxide with $t_{\rm OX} = 15\mu$m during the AC stress at negative and positive polarity.

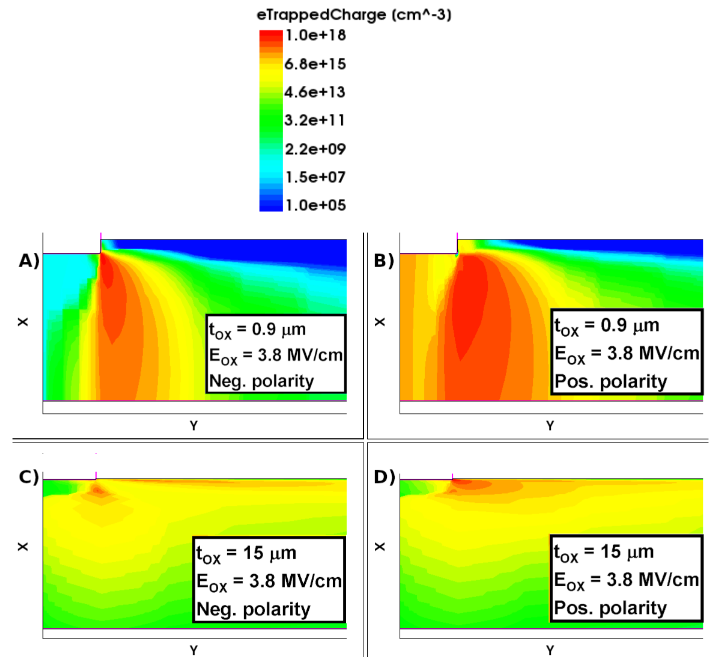

Fig. 6. Trapped charge within the oxide layer for the oxides with thicknesses: $t_{\rm OX} = 0.9\,\mu$m (plots A and B) and $t_{\rm OX} = 15\,\mu$m (plots C and D) at positive and negative polarity during the AC stress. X and Y axes have arbitrary units. The same scale is used on every Y axis, while different scales have been used for the X axes due to the different thicknesses.

the top metal and in particular around the corner, as it can clearly be seen by the solid lines of Fig. 7. Hence, the electric field in this region is much increased if compared to the field built up in the same region of the thinner oxide.

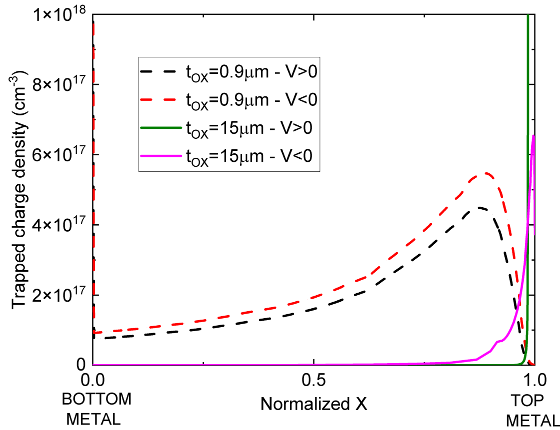

Fig. 7. Trapped charge density along the normalized X axis during the AC stress at negative and positive polarity with $\boldsymbol{E_{OX}} = \mathbf{3.8}$ MV/cm. Dashed lines: $\boldsymbol{t_{OX}} = \mathbf{0.9}\,\boldsymbol{\mu}$m. Solid lines: $\boldsymbol{t_{OX}} = \mathbf{15}\,\boldsymbol{\mu}$m. The position $\mathbf{0}$ corresponds to the bottom metal, the position $\mathbf{1}$ corresponds to the top metal.

As the most significant DC-vs-AC variation of breakdown is observed at large thicknesses, the thickest oxide has been taken as a reference for a further analysis. In Fig. 8, the impact-ionization generation during DC (plots A and B) and AC (plots C and D) stresses is compared for different biases. Two biases have been used for the DC stress condition: $E_{\rm OX} = 3.8$ MV/cm, at the onset of AC breakdown but far from the DC breakdown, and $E_{\rm OX} = 8.8$ MV/cm which is at the onset of the avalanche condition during the DC stress. For the AC stress, only $E_{\rm OX} = 3.8$ MV/cm has been used, at positive and negative polarity.

At small values of $E_{\rm OX}$, the impact-ionization profile in the DC case is very similar to the AC profile during the negative half-wave, with a relatively high hot spot extending around the top metal corner. The electric field reaches a maximum value of about 6 MV/cm, not enough to trigger on the breakdown. Differently, at the same bias, the electric field around the corner during the positive half-wave of the AC stress is very high, with a maximum value of about 14MV/cm, explaining why the impact-ionization generation can reach values as high as 10^{20} cm^{-3}s^{-1}, thus leading to the breakdown of the device. The DC profile at high stresses (top right) is indeed different from all the other situations: the impact-ionization generation is high over a very wide region of the device. The peak generation is still lower than the peak of the AC stress, however, the large extension of the involved region leads to avalanche breakdown.

III. Conclusions

For the first time, TCAD results have been reported that explain the thickness dependence of the breakdown field under different stress conditions in high-voltage TEOS capacitors. The TCAD framework has been proven to be a useful tool to

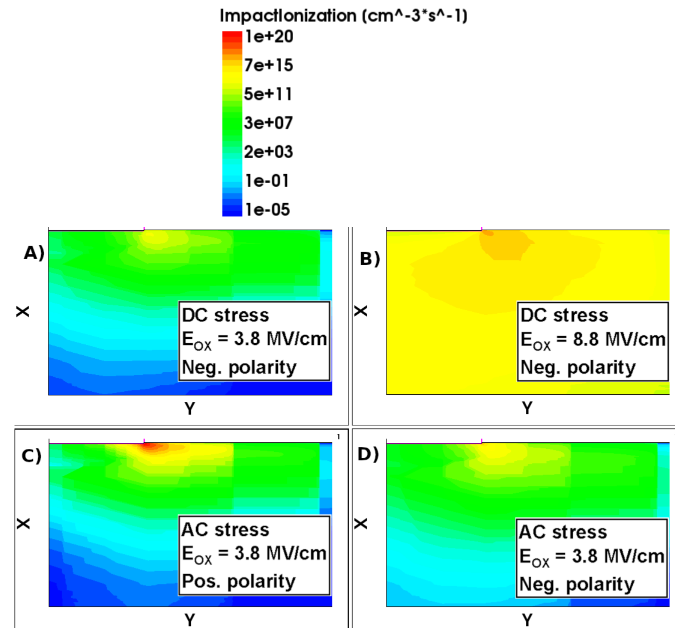

Fig. 8. Impact ionization generation rate within the thick oxide ($\boldsymbol{t_{OX}} = \mathbf{15}\,\boldsymbol{\mu}$m) during AC and DC stresses.
A) DC stress at $\boldsymbol{E_{OX}} = \mathbf{3.8}$ MV/cm (far from breakdown) with negative polarity.
B) DC stress at $\boldsymbol{E_{OX}} = \mathbf{8.8}$ MV/cm (onset of avalanche breakdown) with negative polarity.
C) AC stress at $\boldsymbol{E_{OX}} = \mathbf{3.8}$ MV/cm with positive polarity.
D) AC stress at $\boldsymbol{E_{OX}} = \mathbf{3.8}$ MV/cm with negative polarity.

study the breakdown onset under different stress conditions in realistic 2-D structures. The breakdown of devices with thicknesses in the range 1 - $15\,\mu$m is strongly affected by corner effects: charge build-up in such limited region of the device is responsible for the large increase of the electric field which triggers impact ionization causing the anticipated failure under AC-stress condition for thicker devices.

References

[1] R. Higgins, and J. McPherson, *TDDB Evaluations and Modeling of Very High-Voltage (10 KV) Capacitors*, IEEE 47th Annual International Reliability Physics Symposium, Montreal, QC, Canada, pp. 432-436, April 26-30, 2009. DOI: 10.1109/IRPS.2009.5173292.

[2] W. Wu, S. Rojas, S. Manzini, A. Modelli, D. Re, *Characterization Of SiO_2 Films Deposited By Pyrolysis Of Tetraehylorthosilicate (TEOS)* , Journal de Physique Colloques, Vol. 49 (C4), pp.C4-397-C4-400, 1988. DOI: 10.1051/jphyscol:1988483.

[3] S. Shin, Y.P. Chen, W. Ahn, H. Guo, B. Williams, J. West, T. Bonifield, D. Varghese, S. Krishnan, and M. A. Alam *High Voltage Time-Dependent Dielectric Breakdown in Stacked Intermetal Dielectric*, IEEE 56th Annual International Reliability Physics Symposium, Burlingame, CA, USA, pp. P-GD.9-1-P-GD.9-5, March 11-15, 2018. DOI: 10.1109/IRPS.2018.8353669.

[4] F. Giuliano, S. Reggiani, E. Gnani, A. Gnudi, M. Rossetti, R. Depetro, G. Croce, *Novel TCAD Approach for the Investigation of Charge Transport in Thick Amorphous SiO_2 Insulators*, IEEE Transactions on Electron Devices, Vol. 68, No. 11, pp. 5438-5447, 2021. DOI: 10.1109/TED.2021.3100309.

[5] F. Giuliano, S. Reggiani, E. Gnani, A. Gnudi, M. Rossetti, R. Depetro, G. Croce, *Characterization and numerical analysis of breakdown in thick amorphous SiO_2 capacitors*, Solid-State Electronics, Vol. 192, 2022. DOI: 10.1016/j.sse.2022.108256.

[6] F. Giuliano, S. Reggiani, E. Gnani, A. Gnudi, M. Rossetti, R. Depetro, *Thickness-dependent dielectric breakdown in thick amorphous SiO2 capacitors*, Solid-State Electronics, Vol. 194, 2022. DOI: 10.1016/j.sse.2022.108363.