In-Circuit Assessment of the Long-Term Reliability of E-Mode GaN HEMTs

Giuseppe Capasso, Mauro Zanuccoli, Andrea Natale Tallarico, *Senior Member, IEEE*, and Claudio Fiegna

***Abstract*—This article presents an in-circuit approach to assess the long-term reliability of enhancement-mode GaN HEMTs. A synchronous buck converter conceived for the on-board transistors' characterization is proposed. Here, high-side and low-side power transistors operate under realistic stress conditions, whereas their degradation is assessed by measuring, in-circuit, the full *I–V* characteristics at prefixed stress times. Moreover, a long-term reliability analysis of commercial 80-V GaN HEMTs is reported. Threshold voltage and ON-state resistance degradation induced by the buck converter operation is investigated, as well as their dependencies on the input voltage, duty cycle, ambient temperature, and output current. Results highlight a clear difference compared to standard dc-stress and reveal a strong correlation between the degradation of the high-side transistor and the input voltage. On the contrary, the low-side transistor degradation is almost insensitive to the different operating regimes of the power converter.**

***Index Terms*—DC–DC converter, GaN HEMT, in-circuit characterization, ON-state resistance drift, reliability, threshold voltage shift.**

I. Introduction

THE GaN-based high electron mobility transistor (HEMT) represents an excellent candidate as switching device for power electronics applications, due to its promising electronic properties in comparison to silicon (Si) and silicon carbide (SiC) counterparts. Low power losses, high switching frequency, and high breakdown voltage allow GaN HEMTs to be one of the best candidates for ultracompact and high-power density dc–dc converters for computing applications [1]. In the automotive industry, with the introduction of 48-V batteries, GaN HEMTs could be adopted for low-voltage dc–dc converters, especially for 48-/12-V conversion [2], [3].

Power semiconductor devices are the most prone-to-failure components in power converters [4]. The stress conditions are primarily induced by OFF-state voltage, hard-switching, and self-heating effects over a long-time operation. Furthermore, increasing the switching frequency and reducing the transistors' turn-on and turn-off times in the nanoseconds range, the device must sustain possible additional stress induced by voltage overshoots and current spikes.

It is well known that GaN HEMTs can be affected by several degradation mechanisms that lead to a drift of On-state drain–source resistance (R_{ON}) and threshold voltage (V_{TH}), limiting their performance and reliability [5], [6], [7], [8], [9]. To assess the GaN device reliability, two main different experimental approaches can be distinguished, i.e., single transistor stress (on-wafer or in package) and in-circuit degradation analysis.

The first approach—the mostly adopted one—consists in the study of stress-induced degradation by monitoring the I–V characteristics of the individual transistor. Such method is useful to obtain relevant physical information about failure and aging mechanisms. For instance, in [5], the negative V_{TH} shift in metal–insulator–semiconductor (MIS) HEMTs has been ascribed to the depletion of trap states located at the SiN/AlGaN interface and/or gate insulator. In [6], the role of the aluminum content in the AlGaN barrier layer on the V_{TH} degradation of GaN HEMTs with p-type Schottky gate has been analyzed. The drain current collapse caused by self-heating effects and transient charge trapping phenomena has been investigated in [7] and [8], respectively. However, these experimental results are limited to the application of standard dc or pulsed stress and recovery methods. Modolo et al. [9] have proposed an on-wafer hard-switching setup to study the GaN HEMT degradation. However, the analysis was carried out at the switching frequency of 100 kHz, probably limited by the involved parasitics.

The second approach consists in the development of test beds able to reproduce realistic stress conditions and monitor the health status of the GaN HEMTs [10], [11], [12], [13], [14], [15]. In [10], a chopper buck circuit, operating at 20-kHz switching frequency, is used to stress GaN HEMTs. However, the power devices were physically removed from the circuit to characterize their degradation in terms of R_{ON}

Manuscript received 9 June 2023; revised 25 August 2023; accepted 20 September 2023. Date of publication 3 October 2023; date of current version 24 October 2023. This work was supported in part by Intelligent Reliability 4.0 (iRel40), iRel40 is a European co-funded innovation project that has been granted by the Electronics Components and Systems for European Leadership (ECSEL) Joint Undertaking (JU) under Grant 876659. The founding of the project comes from the Horizon 2020 Research Programme and participating countries. National Funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, The Netherlands, Slovakia, Spain, Sweden, and Turkey. The review of this article was arranged by Editor B. J. O'Sullivan. *(Corresponding author: Giuseppe Capasso.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3318865.

Digital Object Identifier 10.1109/TED.2023.3318865

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and V_{TH} shifts. Threshold voltage is not straightforward to monitor; therefore, in-circuit analyses mainly focus on the degradation of the R_{ON} drift evaluated during the deviceON-state as the ratio between V_{DS} and I_D, measured through clamp circuits and current sensors, respectively. In [11], a setup aimed at detecting the degradation of dynamic R_{ON}, in the milliseconds range, under different OFF-state voltages and temperatures, has been proposed. In [12], a test circuit in half-bridge configuration is adopted to evaluate the R_{ON} variation under several hard- and soft-switching conditions for switching frequency up to 1 MHz. The test beds proposed in [13] and [14] allow the estimation of the R_{ON} degradation considering high switching frequency operation (up 1 MHz), analyzing the effects of high temperature and current intensity. Finally, in [15], an integrated dc–dc converter is proposed to monitor R_{ON} degradation up to few hundreds kilohertz switching frequency. However, the analysis based on on-the-fly measurement suffers some limitations. As reported in [16], the measured R_{ON} is sensitive to V_{TH} shift caused by charge trapping and detrapping mechanisms. A positive V_{TH} shift reduces the gate overdrive voltage, hence I_D, misinterpreting it as a drift of R_{ON}. Therefore, the analysis of the full I–V characteristics is of paramount importance for an accurate assessment of the power transistor reliability.

This article proposes an automatic characterization system, based on a power dc–dc synchronous buck converter, aimed at stressing the GaN HEMTs and assessing their degradation through a full I–V characterization. Due to this approach, the power devices operate under a combination of typical power converter stress regimes, including hard-switching, pulsed OFF- and ON-state. However, since the I–V characterization is performed offline, requiring a relatively short interruption of the power circuit operation, the effects of nonpermanent fast trapping and detrapping phenomena (<1 s) cannot be explored, focusing the analysis to the long-term reliability.

This article is structured as follows: Section II provides an overview of the principle of operation and the adopted circuital solutions of the proposed technique. Section III presents a long-term degradation analysis of commercial GaN HEMTs under several power converter operating conditions, discussing the role of input voltage, duty cycle, output current, and ambient temperature. Finally, Section IV draws conclusions based on the experimental results.

II. Experimental Setup

Fig. 1 depicts the proposed setup, which mainly includes a synchronous buck converter to apply realistic stress conditions and a set of source measurement unit (SMUs) for transistors I–V characterization. During the stress mode, the switches S_{1-5} are closed and the devices under test (DUTs) operate into the synchronous buck converter. During the characterization phase, the DUTs are isolated from the power network by opening S_{1-5} and connected, one at a time, to the SMUs by means of S_D, S_G, and S_S relays. The DUTs isolation avoids possible perturbations induced by the converter circuit during the I–V characterization. The latter is carried out through a four-wires approach, and its accuracy was validated by comparison with the measurements performed directly on the standalone transistors. Finally, an external board composed by a matrix of relays handles the switches' connections. It allows to automatically switch between converter (stress) and characterization (measure) phase during the test.

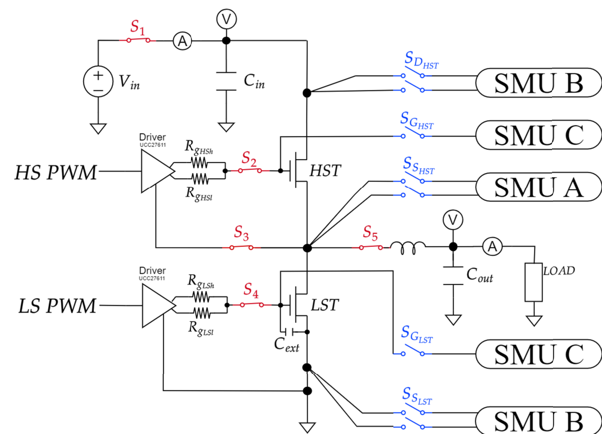

Fig. 1. Simplified electric diagram of the proposed setup. The red relays enable the stress mode induced by synchronous buck converter, whereas the blue ones alternatively allow the characterization of the DUTs.

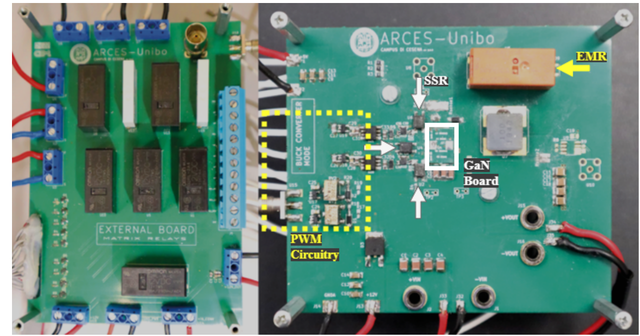

Fig. 2. Relay board (left) and main board (right) prototype. In the latter, it is possible to note: PWM circuit (yellow box), solid-state relays (white arrows), electromechanical relay (yellow arrow), and GaN board (white box).

As reported in [17], characterization and stress phases are alternatively repeated in accordance with a standard measure–stress–measure technique. After each degradation step, the setup takes approximately 1 s to safety shut-down the converter and to begin transistors I–V characterizations with the SMUs. The measured characteristics reflect the overall actual transistors degradation occurring during their operation within the dc–dc converter.

Fig. 2 reports the relay-matrix board (left) and the main board (right). The latter includes the synchronous buck converter, in particular: 1) an analog circuitry (yellow dashed box) able to generate highly flexible PWM signals with adjustable dead time; 2) solid-state relays (SSRs) placed in the gate loops ($S_{2,3,4}$), highlighted by white arrows; and 3) electromechanical relay (EMR) placed before the inductor (S_5), indicated with yellow arrow. Currently, the specifications of the adopted PWM circuitry and EMR limit the maximum allowed ambient temperature to 85 °C.

The power GaN HEMTs used for this study is a commercial 80-V enhancement-mode GaN HEMT with a typical R_{ON} of

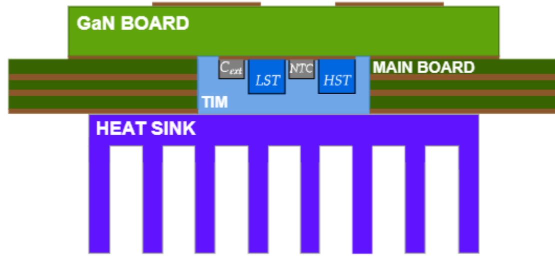

Fig. 3. Cross section sketch of the GaN board mounting. LST and HST denote the low-side and high-side transistors, respectively. TIM is used to fill the gap between GaN HEMTs and heatsink. NTC and C_{ext} represent the NTC thermistor and the external gate-to-source capacitor mounted on the GaN board.

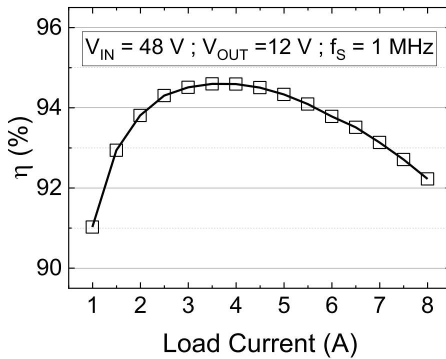

Fig. 4. Efficiency curve of the proposed synchronous buck converter. A peak of ∼94.5% occurs between 3 and 4.5 A.

20 mΩ. The maximum continuous drain current (I_D) is 6.8 A. They are assembled on a dedicated PCB (denoted as GaN board), which is necessary to easily replace the stressed DUTs after tests completion. To mitigate unavoidable parasitic effects affecting the critical loops of the converter layout, due to the introduction of additional components and GaN HEMTs assembly, series gate resistors have been adopted [18] and an extra gate–source capacitor, C_{ext}, has been added to boost the Miller ratio [19].

Fig. 3 illustrates the cross section view of the GaN board, soldered on the main PCB; the DUTs, high-side transistor (HST) and low-side transistor (LST) of the half bridge, are placed on its bottom surface. Thermal dissipation of GaN HEMTs is allowed by means of a heatsink. The residual gap of 0.185 mm between heatsink and transistors is filled by thermal interface material (TIM), exhibiting high thermal conductivity. A negative temperature coefficient (NTC) thermistor is placed between the two transistors (Fig. 3) to monitor the temperature over the stress time. As a result, by knowing ambient temperature, thermal resistances (devices, TIM, and heatsink) and transistor's power dissipation (from simulation) the junction temperature of the devices can be estimated.

The isolation relays located in the critical paths of the circuit and the assembly of GaN HEMTs on a dedicated board make the PCB layout more complex and prone to parasitics compared to a conventional circuit topology. However, due to an accurate layout design assisted by electromagnetic simulation [20], the converter is able to operate at switching frequencies up to 1 MHz with an efficiency over 94%, as reported in Fig. 4. The measured voltage waveforms at the switching node and on the gate of the HST and LST are shown in Fig. 5, in the case of a switching frequency of 1 MHz, 48-/12-V input–output voltage, and 4-A output current. It is worth noting that waveforms are measured on test points, which are relatively far from transistors' terminals; therefore, they are affected by perturbations [21] during high-frequency operation (1 MHz). However, as observed in Fig. 5, electrical simulations accounting for circuit parasitics, estimated by electromagnetic simulation, accurately reproduce the experiments, allowing us to evaluate the signals waveform directly at the terminals of the transistors.

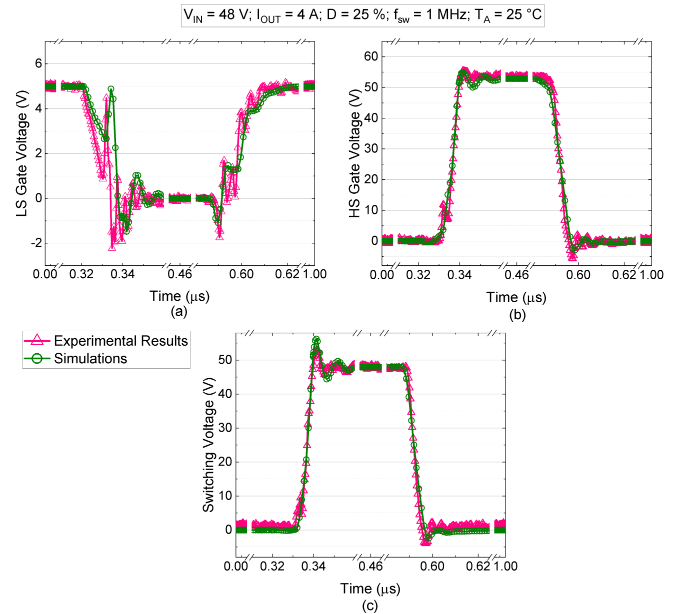

Fig. 5. Measured and simulated voltage waveforms of the synchronous buck converter at $V_{\text{IN}} = 48$ V, $I_{\text{OUT}} = 4$ A, $D = 25\%$, $f_{\text{sw}} = 1$ MHz, and $T_a = 25\ ^\circ$C.

III. Experimental Results

A. Preliminary DC Reliability Analysis

A preliminary aging analysis under OFF- and ON-state dc stress has been carried out to analyze the device's behavior from the reliability standpoint and to provide a reference for the in-circuit reliability analysis. Devices do not show degradation under ON-state dc stress ($V_{\text{GS}} = 5$ V, $I_D = 6.8$ A, and stress time $8 \cdot 10^4$ s) except for a slight V_{TH} drift induced by the gate bias (∼0.2 V after 10^5 s), as shown in Fig. 6.

On the contrary, a drift has been observed for both R_{ON} and V_{TH} in the case of OFF-state dc stress. In particular, devices have been stressed at 64 V drain-to-source voltage (V_{DS}) for $8 \cdot 10^4$ s and ambient temperature (T_a) ranging from 40 °C to 150 °C. Fig. 7 shows the R_{ON} (a) and V_{TH} (b) drift during the stress for different T_a values. A nonmonotonic temperature dependency is observed for both ΔR_{ON} and ΔV_{TH}. In particular, their drift increases for increasing T_a up to 100 °C, while they decrease for $T_a > 100$ °C, suggesting the presence of two competing trapping mechanisms. Such behavior is correlated to the distribution of the drain leakage current during the

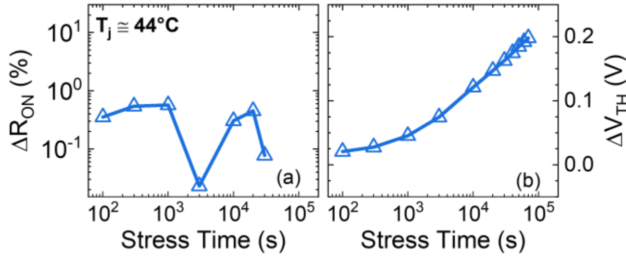

Fig. 6. (a) R_{ON} and (b) V_{TH} drift under ON-state stress condition ($I_D = 6.8$ A; $V_{GS} = 5$ V).

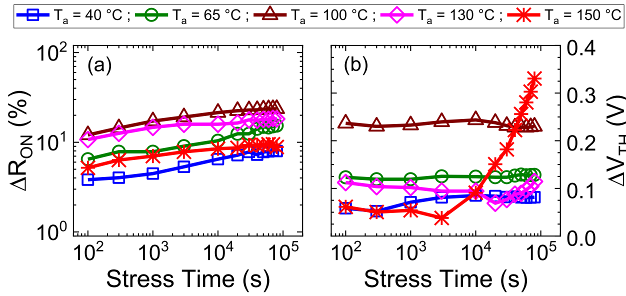

Fig. 7. (a) R_{ON} and (b) V_{TH} drift under OFF-state stress condition ($V_{DS} = 64$ V; $V_{GS} = 0$ V) as a function of different ambient temperatures T_a.

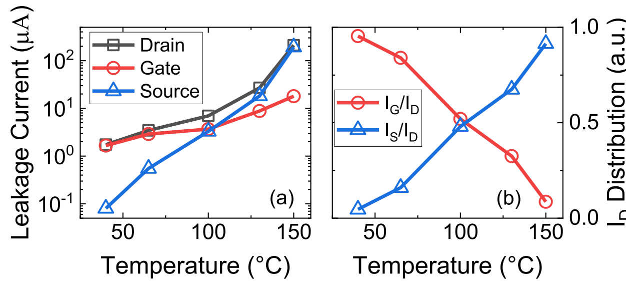

Fig. 8. (a) Leakage currents under OFF-state stress condition ($V_{DS} = 64$ V; $V_{GS} = 0$ V) at various ambient temperatures T_a. (b) Gate (I_G) and source (I_S) leakage currents normalized with respect to drain one (I_D) at various ambient temperatures.

stress, as reported in Fig. 8. It flows mainly through the gate electrode for temperatures below 100 °C, while it provides larger contribution to the source current at larger T_a values. Unfortunately, further physical insights cannot be provided due to a lack of information on the device architecture and fabrication process.

Finally, by focusing on ΔV_{TH} [Fig. 7(b)], a significant drift can be observed after $3 \cdot 10^3$ s for $T_a = 150$ °C. A similar behavior seems to occur, at longer stress times, for $T_a = 130$ °C. In [22], a ΔV_{TH} up to 40% has been ascribed to the ionization of out-diffused Mg-related acceptor traps in the AlGaN region, caused by the high electric field induced by large V_{DS}. In our case, the observed temperature dependence is consistent with the presence of the same mechanism.

B. In-Circuit Reliability Analysis

When power transistors operate in a synchronous dc–dc buck converter, multiple stress factors may contribute to their aging. In particular, the single device switches from

TABLE I
ACCELERATED STRESS FACTORS FOR SYNCHRONOUS BUCK CONVERTER

STRESS FACTOR	STRESS CONDITIONS
Voltage (V_{IN})	OFF-state; semi ON-state
Duty cycle (D)	OFF-state; ON-state
Temperature (T_a)	All
Current (I_{OUT})	ON-state; semi ON-state
Switching frequency (f_{sw})	semi ON-state

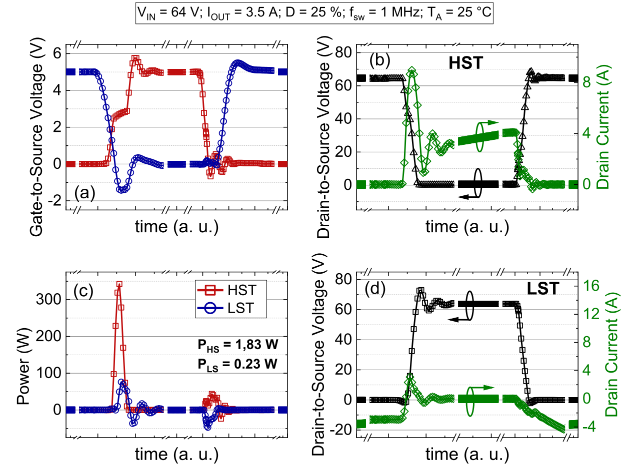

Fig. 9. Simulated waveforms at the transistors' terminals in the case of $V_{IN} = 64$ V, $I_{OUT} = 3.5$ A, $D = 25\%$, $f_{sw} = 1$ MHz, and $T_a = 25$ °C. HST and LST (a) V_{GS} and (c) power dissipation; V_{DS} and I_D in the case of (b) HST and (d) LST.

OFF- to ON-state and vice versa, sustaining a high drain voltage V_{IN} and current I_{OUT} during the semi periods t_{OFF} and t_{ON}, respectively; the durations of such semi-periods depend on the switching frequency (f_{sw}) and duty cycle (D). In addition, the so-called "hard-switching" transition from OFF- to ON-state and vice versa includes a third stress phase, i.e., semi ON-state, in which the device is simultaneously subjected to relatively high V_{DS} and I_D for a few nanoseconds. In such a condition, it has been demonstrated that hot-electron effects play a crucial role in the device degradation [23].

Table I summarizes the possible acceleration factors and the corresponding stress phases, within each cycle of buck-converter operation.

In order to characterize the device degradation, V_{TH} is measured by means of constant-current method, in our case $V_{TH} = V_{GS}$ at $I_D = 3$ mA with $V_{DS} = 5$ mV, whereas R_{ON} is evaluated in the linear region at a given gate overdrive voltage, in order to exclude a possible contribution deriving from the drift of V_{TH}. Furthermore, the parameters drift is evaluated with respect to their respective values measured after 100 s of converter operation in order to: 1) focus mainly on the long-term/permanent degradation, since, as reported in [17], the drift occurring during the initial stage of test is fully recoverable; and 2) reach a thermal steady-state condition.

1) HST Versus LST Degradation: A synchronous buck converter induces asymmetrical stress to the DUTs in terms of applied voltage, current, and temperature.

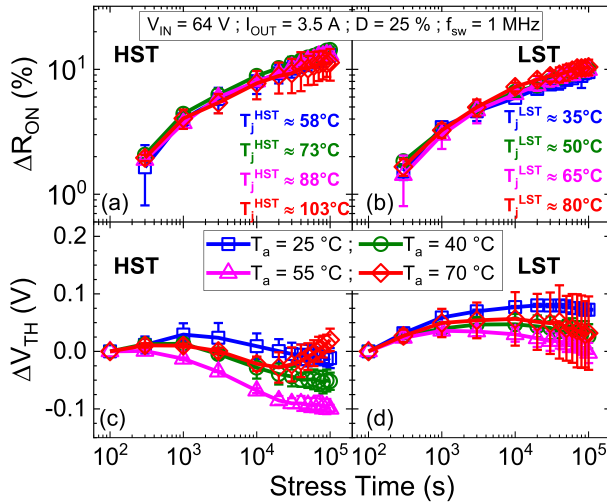

Fig. 10. R_{ON} and V_{TH} drift in the case of (a) and (c) HST and (b) and (d) LST during the stress time while the devices operate in the buck converter under different ambient temperatures (T_a). T_j denotes the estimated junction temperature.

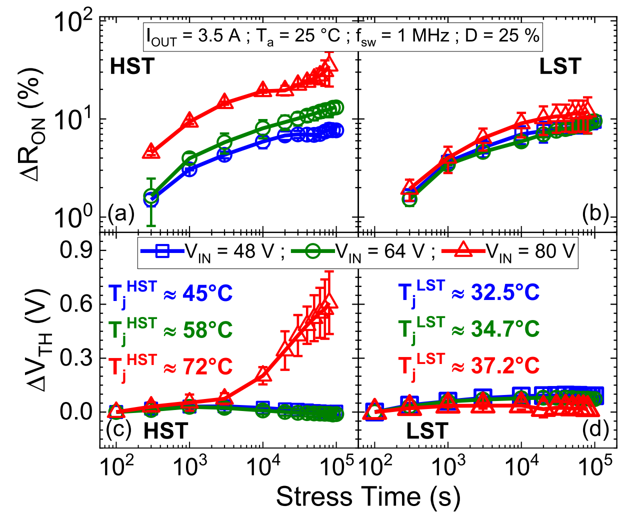

Fig. 11. R_{ON} and V_{TH} drift in the case of (a) and (c) HST and (b) and (d) LST during the stress time while the devices operate in the buck converter under several input voltage conditions. T_j denotes the estimated junction temperature.

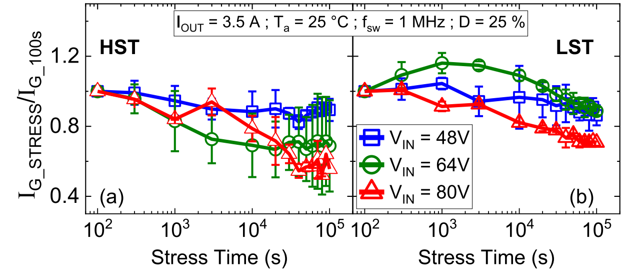

Fig. 12. I_G variation of (a) HST and (b) LST during the stress time while the devices operate in the buck converter under several input voltage conditions. I_G has been monitored at $V_G = 5$ V.

Fig. 9 depicts the simulated V_{GS}, V_{DS}, I_D, and power dissipation of the HST and the LST operating with $V_{IN} = 64$ V, $I_{OUT} = 3.5$ A, $D = 25\%$, $f_{sw} = 1$ MHz, and $T_a = 25$ °C. It is worth noticing that deadtime external gate series resistors and gate-to-source capacitor have been set and adopted to prevent shoot-through phenomenon, maximize converter efficiency, and improve the signal integrity. However, it can be observed how the HST is subjected to a large switching power loss during its turn-on, making switching losses dominant. On the contrary, they are negligible in the LST, where the conduction losses are the dominant ones. HST switching losses and LST conduction losses account for ~65% and ~8% of the whole system losses, respectively. As a consequence, the HST is more subjected to hard-switching stress compared to LST, showing up, as reported from here on, a larger ΔR_{ON}.

2) Role of Ambient Temperature: A temperature-dependent in-circuit analysis has been carried out to make a first rough comparison with the results of OFF-state dc stress (Fig. 7). It is worth noticing that, although the same OFF-state voltage level ($V_{IN} = 64$ V) has been adopted, 10^5 s of converter stress time corresponds to $75 \cdot 10^3$ s and $25 \cdot 10^3$ s of cumulative t_{OFF} for HST and LST, respectively. Moreover, the DUTs can be subjected to additional simultaneous stress factors, e.g., hard-switching.

T_a has been varied from 25 °C to 70 °C by means of a laboratory oven, which corresponds to an estimated HST junction temperature (T_j) between 58 °C and 103 °C, respectively.

Finally, I_{OUT}, f_{sw}, and D were fixed at 3.5 A, 1 MHz, and 25%, respectively, ensuring the operation of the power transistors within their safe operating area (SOA).

Fig. 10 reports the related R_{ON} (top) and V_{TH} (bottom) drift, as a function of T_a, in the case of HST (left) and LST (right). It is possible to note that ΔR_{ON} does not show T-dependency neither on HST (a) nor on LST (b), highlighting a significant difference with respect to dc-stress case. As already anticipated, the power transistor operating in a switching circuit is subjected to different stress factors. By focusing on the R_{ON} drift, the role of the ON-state stress (high I_D) can be excluded as no aging has been observed in the case of dc stress, although a higher I_D has been adopted. As a result, it is possible to conclude that ΔR_{ON} reported in Fig. 10(a) and (b) is due to the combined effect of OFF- and semi ON-state-related degradation mechanisms. The latter, as reported in [23], is dominated by hot-electron effects, which, having a negative T-dependence, can compensate the positive one observed in the case of OFF-state dc stress [Fig. 7(a), up to 100 °C].

Concerning ΔV_{TH}, both HST [Fig. 10(c)] and LST [Fig. 10(d)] show a similar T-dependency, which is different from the one observed in the case of OFF-state dc stress under a wider T_a range. As a matter of fact, it decreases up to $T_a = 55$ °C; then, it starts to increase for higher T_a. Moreover, V_{TH} seems to show the start of a significant positive drift in the case of HST stressed with $T_a = 70$ °C, probably triggered by the relatively high junction temperature, i.e., ~103 °C. Unlike the OFF-state dc stress, here the gate-stack can be site of competing trapping mechanisms induced by positive gate bias (ON-state), high drain voltage (OFF-state), and combination of both including relatively high I_D (semi ON-state). Overall, by considering dc-stress analysis and the in-circuit one, it is

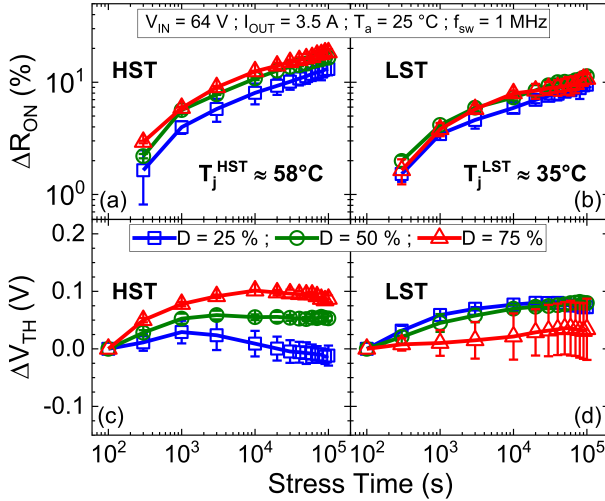

Fig. 13. R_{ON} and V_{TH} drift in the case of (a) and (c) HST and (b) and (d) LST during the stress time while the devices operate in the buck converter under several duty cycle conditions. T_j denotes the estimated junction temperature.

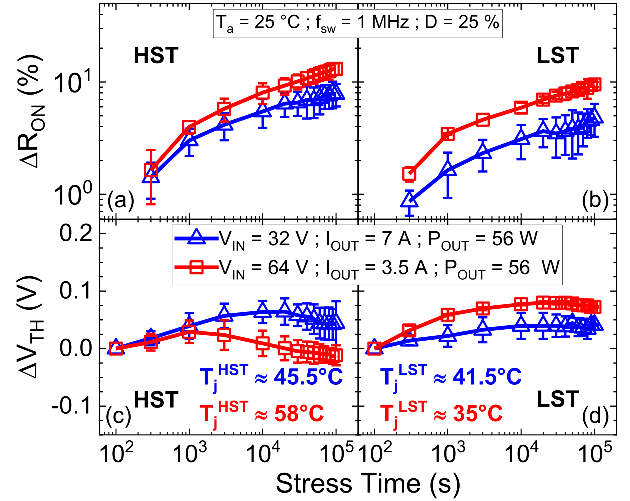

Fig. 14. R_{ON} and V_{TH} drift in the case of (a) and (c) HST and (b) and (d) LST during the stress time while the devices operate in the buck converter at the same output power but with different input voltages and output currents. T_j denotes the estimated junction temperature.

clear that the temperature is an accelerating factor for the V_{TH} degradation, while ΔR_{ON} is almost T-independent in the case of in-circuit stress.

3) Role of Input Voltage and Duty Cycle: To investigate the role of the converter input voltage, three different biases have been adopted, i.e., 48, 64, and 80 V, while keeping fixed $f_{sw} = 1$ MHz, $I_{OUT} = 3.5$ A, $D = 25\%$, and $T_a = 25$ °C. By observing Fig. 11, it is possible to note that ΔR_{ON} increases with V_{IN} only in the HST case [Fig. 11(a)], although both transistors are subjected to the same OFF-state voltage (V_{IN}). This behavior may be correlated to two factors: 1) longer t_{OFF} values, since HST sustains an OFF-state voltage for the 75% of the switching period, against 25% in the LST case; 2) hard switching (semi ON-state), which primarily impacts the HST, as shown in Fig. 9, and confirmed by the higher T_j caused by self-heating effects (Fig. 11).

The role of t_{OFF} can be excluded by observing Fig. 13(a) and (b), reporting ΔR_{ON} in the case of in-circuit tests performed with different duty cycles, i.e., 25%, 50%, and 75%, for the HST and LST. Both transistors do not show the expected t_{OFF}-dependency; on the contrary, ΔR_{ON} of the HST [Fig. 13(a)] is slightly reduced in the case of longer t_{OFF} (smaller D). As a result, the relationship between ΔR_{ON} and V_{IN} observed in the case of HST [Fig. 11(a)] can be mainly ascribed to the hard-switching stress, which is enhanced by increasing V_{IN}. The latter induces an increase of the longitudinal electric field in the drain-to-gate access region, amplifying the hot-electron-related degradation mechanisms, causing a larger ΔR_{ON}.

By focusing on ΔV_{TH}, on the one hand, it is possible to note that the sole increase of drain voltage (V_{IN}) does not lead to relevant V_{TH} drift, as reported in Fig. 11(d). On the other hand, the combination of relatively high V_{DS} and T produces a relevant V_{TH} degradation [Fig. 11(c)]. The latter has not a clear impact on the gate leakage, as shown in Fig. 12, suggesting that: 1) ΔV_{TH} is not caused by a possible degradation of the metal/p-GaN Schottky junction, i.e., the reverse-biased junction determining I_G at $V_G = 5$ V; and 2) ΔV_{TH} is ascribed, as in the case of dc stress (Section III-A), to the ionization of out-diffused Mg-related acceptor traps in the AlGaN region, caused by the combination of high temperature and electric field induced by large V_{DS} (V_{IN}).

Overall, by considering the results reported so far, the higher V_{DS}, the lower T (and vice versa) needed to induce an uncontrolled positive V_{TH} drift. By limiting both V_{DS} and T as in the case of Fig. 13, ΔV_{TH} is relatively small. In such a case, this small drift seems to be associated with ON-state degradation, i.e., gate-bias stress, since ΔV_{TH} increases with D, hence with t_{ON}, the time interval during which the gate is positively biased.

4) Role of Output Current: In order to analyze the role of the converter's output current on the GaN HEMTs reliability, a further test has been carried out by setting $I_{OUT} = 7$ A and $V_{IN} = 32$ V. The input voltage has been reduced to maintain the same duty cycle and output power of the reference case ($V_{IN} = 64$ V, $D = 25\%$, $I_{OUT} = 3.5$ A, and $P_{OUT} = 56$ W). The experimental results are plotted in Fig. 14.

It is clear that the increase of I_{OUT} while reducing V_{IN} results in a greater robustness for both HST and LST. In particular, both transistors show a higher ΔR_{ON} in the case of higher V_{IN}, in spite of the lower I_{OUT} (i.e., I_D in ON-state), confirming: 1) the negligible role played by the ON-state current and 2) the significant impact of the OFF-state voltage on the transistor degradation. Finally, V_{TH} does not exhibit a significant shift, as T is relatively low.

IV. Conclusion

In this article, a novel approach aimed at assessing the long-term reliability of GaN HEMTs operating under realistic stress conditions has been proposed. The experimental setup consists in a custom synchronous buck converter operating at a high switching frequency (1 MHz) and enabling in-circuit full I–V characterization of the power transistors, overcoming several

limitations affecting the currently available methodologies for degradation analysis.

Moreover, a long-term reliability analysis of commercial e-mode GaN-HEMTs has been performed under several operating conditions of the dc–dc converter, investigating the role of input voltage, ambient temperature, duty cycle, and output current.

In contrast to a preliminary dc-stress analysis, the in-circuit-related results have shown that ambient temperature does not affect the degradation of R_{ON}, whereas it plays an appreciable role in the V_{TH} shift. A significant correlation has been found between the input voltage of the converter and device reliability. In particular, a larger R_{ON} shift and a significant positive V_{TH} drift of the high-side transistor are observed by increasing the input voltage, likely due to the combination of high electric field and high junction temperature. The role of V_{IN} has been mainly related to hard-switching stress rather than the OFF-state one.

Finally, the duty cycle has shown a role only on V_{TH} shift, i.e., larger by increasing D (longer t_{ON}), whereas the output current does not have a significant impact on the device degradation, except for the indirect one related to self-heating.

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Open Access funding provided by 'Alma Mater Studiorum - Università di Bologna' within the CRUI CARE Agreement