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Architecture and First Characterization of the Microstrip Silicon Detector Data Acquisition of the FOOT experiment

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Abstract—Oncological hadrontherapy is a novel technique for cancer treatment that improves over conventional radiotherapy by having higher effectiveness and spatial selectivity. The FOOT (FragmentatiOn Of Target) experiment studies the nuclear fragmentation caused by the interactions of charged particle beams with patient tissues in Charged Particle Therapy. Among the several FOOT detectors, the silicon Microstrip Detector is part of the charged-ions-tracking magnetic spectrometer. The detector consists of three x-y planes of two silicon microstrip detectors arranged orthogonally between each other to enable tracking capabilities. Ten analog buffer chips and five ADCs read out each detector. A Field-Programmable Gate Array collects the output of the ADCs of an x-y plane, possibly processes the data, and forms a packet to be sent to the experiment central data acquisition. This data acquisition system shall withstand the trigger rate and detector's throughput at any time. In this work, we discuss the architecture of the data acquisition system-in particular of the silicon microstrip detector one-and the first results obtained from the x-y plane's prototype.

I. INTRODUCTION

T HE Fragmentation Of Target (FOOT) experiment aims at collecting experimental data in the area of Charged Particle Therapy (CPT) [1], which treats deep-seated tumors with higher effectiveness and spatial selectivity with respect to conventional radiotherapy. These data will deepen the knowledge on the interaction of particle beams with patients' tissues by studying the nuclear fragments [2], [3] production in terms of cross section, energy spectra, and particles identification.

Measuring the characteristics like yield, charge, energy, and angle of nuclear fragments is vital to know the effects of particles' interaction with the human body, that can be applied both to CPT or radioprotection in space [4]. FOOT will use the inverse kinematics [5] approach to overcome the problem of low-energy and short-range fragments production. It will use beams of ions of which human tissues are rich, like C, O, or Ca, that impinge on hydrogen-rich targets.

FOOT will use ion beams of energies of 50–250 MeV for protons and 50–400 MeV/u for Carbon ions. These beams will be distributed in several facilities and experimental rooms, each with its space limitations and technical requirements.

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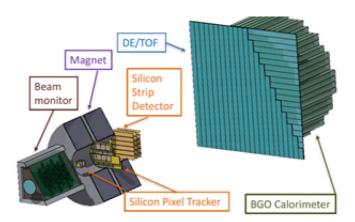


Fig. 1. CAD model of FOOT, showing all the experiment's detectors. The beam goes from the bottom-left corner to the top-right one.

Portability among facilities and small dimensions are therefore of paramount importance for FOOT.

Fig. 1 shows the experiment architecture. It consists of multiple detectors capable of different measurements of charged fragments' kinematic quantities over a 10° cone around the beam axis. The detectors are divided into three main regions:

- the *pre-target* has monitor tasks, with a beam monitor and a start counter detectors.
- the magnetic spectrometer tracks and identifies crossing fragments to measure their kinetic energy and momentum. It consists of magnets, two silicon pixel trackers, and one Silicon Micro-Strip Detector.
- the *fragment identification*—the farthest region from the target—uses scintillators and calorimeters to measure the time of flight (TOF) and kinetic energy of fragments.

II. THE SILICON MICRO-STRIP DETECTOR

The magnetic spectrometer region hosts the silicon Micro-Strip Detector (MSD) to measure the position of fragments on three planes in space. Being the MSD placed after the magnetic volume, these points are used to reconstruct the paths of crossing fragments and hence to evaluate their kinetic energy and momentum. Fig. 2 shows a block diagram of the MSD, which consists of three x-y planes of two silicon microstrip detector.

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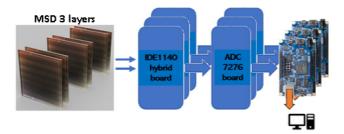


Fig. 2. Block diagram of the MSD showing three replicas of detector x-y planes. For each x-y plane we see, from left to right, the 2-layer detector, the IDE1140 readout, the ADC board, and a DE10-Nano. The arrows show the direction of the data flow.

Each microstrip detector measures an x or y coordinate via a 150-µm-thick sensor¹ with an active area of $96 \times 96 \text{ mm}^2$. 1920 strips with a 50 µm pitch populate the area, but only one out of three strips is read out externally. The number of read out strips is 640, for an overall pitch of 150 µm.

A hybrid board hosts one sensor and ten 64-channels, lownoise, and low-power IDE1140s readout chips². Each IDE1140 input channel embeds a charge-sensitive preamplifier, a slow shaper, and a sample-and-hold circuitry. Being capable of multiplexing in time the analog output of the strips into a single line, two IDE1140 chips are connected in a daisy-chain fashion. A 40-pin connector, line drivers, and line buffers complete the hybrid board.

III. MSD DATA ACQUISITION SYSTEM

The rationale behind the MSD data acquisition (DAQ) system was the same as for the whole FOOT experiment: scalability and adaptability to multiple conditions. Fig. 3(a) shows the concept behind an MSD x-y plane, while Fig. 3(b) a picture of the actual system. The DAQ consists of two main components: the ADC board and the DAQ board. The former hosts the ADCs to digitize the IDE1140 outputs, whereas the latter embeds the controller of all of the other subsystems and the interface toward the central system.

Each ADC board serves one x-y plane, *i.e.* two microstrip detectors, connected via two 40-pin connectors. The board embeds ten 12-bit 3-Msps AD7276A³ ADCs and each of them digitizes two IDE1140 outputs. We chose the number of IDE1140s per ADC, and thus the total number of ADCs, to guarantee a maximum dead time below 500 μ s. The board also includes one device to generate the bias voltage for the x-y plane and the buffers/drivers for the DAQ board.

The ADC board directly plugs to the DAQ board, *i.e.* a Terasic DE10-Nano board. This commercial board is the core unit of the x-y plane readout with an Intel Cyclone V System-On-Chip device that embeds an FPGA and a Microcontroller, referred to as Hard Processor System (HPS). The Cyclone V commands the IDE1140s and ADCs, collects their digital output, and communicates with the central DAQ system.

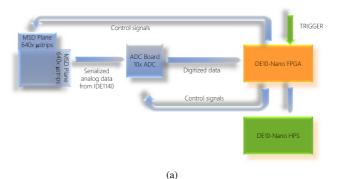




Fig. 3. Concept (a) and actual picture (b) of an MSD x-y plane and its readout. From bottom to top, there are the ADC board, DE10-Nano, and one hybrid board with ten IDE1140s and one sensor. The picture misses one hybrid board to form a complete x-y plane.

The FPGA side of the Cyclone V takes care of the first two tasks. Once the central DAQ system issues a trigger signal, the FPGA starts the following readout procedure:

- 1) wait for the IDE1140 shaper to reach its peak;
- start the IDE1140s readout process with a pulse of their shift in line;
- 3) enable the *hold* of the sample-&-hold circuitry;
- 4) activate the ADCs by deasserting their chip select;
- 5) feed the ADCs' serial clock to synchronize their output;
- 6) sample the incoming *serial data* from the ADCs and parallelize them in 16-bit shift registers;
- feed the IDE1140s *clock* to multiplex in output all of the microstrip values.

Steps 4)-7) are repeated 128 times, or the total number of strips multiplexed to each ADC.

The ten streams of parallel output from the ADCs are interleaved to form a 32-bit wide packet, that is encapsulated with a header and a trailer. The header contains the packet length, a progressive number of triggers occurred, and a timestamp computed from an external 1-MHz clock. Because each ADC generates 128 2-byte words, the length of a packet

¹The sensors are produced by Hamamatsu Photonics

²The commercial readout devices are produced by IDEAS, https://ideas.no/ products/ide1140

³The ADCs are produced by Analog Devices, https://www.analog.com/en/ products/ad7276.html

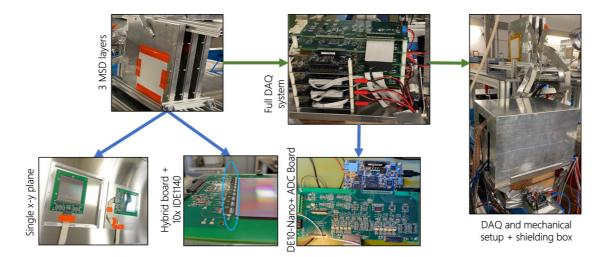


Fig. 4. Real view of the MSD system.

is fixed to 1280 bytes for a single detector, 2560 bytes for one x-y plane, and ~8 kB for three x-y planes. No further processing is performed on the packet yet. In the future we could implement a dedicated compression to decrease the bandwidth and memory occupation of the data stream. Some ancillary electronics implement an array of registers for slow control and monitoring.

The DE10-Nano HPS communicates with the FPGA via an AXI interface, with a maximum throughput of 100 Gbps. The FPGA writes the events directly into the HPS memory via Direct Memory Access (DMA), to guarantee the maximum use of the AXI interface bandwidth. The HPS is based on the embedded Linux distribution developed by Terasic, which runs custom software for all of the FOOT-related tasks. All the communications—including slow control, monitoring, and physics data—rely on a TCP channel over the 1 Gbps Ethernet interface of the board.

A patch-panel completes the DAQ system with the electrical interface toward the central trigger control unit. For the received signals of trigger, clock, and reset it provides conversion from LVDS to single-ended 3.3-LVTTL and fan-out for all of the DE10-Nano boards. It also converts the single-ended busy lines from the DE10-Nano to LVDS signals to be sent to the central trigger control unit. All of the electronic boards are placed in an aluminum box that acts as a Faraday cage to reduce interference and noise from the environment. Fig. 4 shows the detailed schematic of the actual system.

IV. FIRST MEASUREMENTS RESULTS

With the system described in the previous chapters, we performed the first measurements of the MSD detector. A key aspect we analyzed is the one of the pedestals: the base-level of each microstrip when there are no particles crossing the detectors. We will use such pedestals in further acquisitions with actual radiation sources to have a close-to-zero output of the system when there is no particle generated signal.

Fig. 5 shows an analysis of the pedestals of one microstrip detector computed on 5000 events. Fig. 5(a) shows their mean

value, while Fig. 5(b) their standard deviation. The pedestal values for the whole detector spans between 150 and 350 ADC counts, but for each channel is distributed around the mean value with a standard deviation of ~ 1.8 ADC Counts. There is one outlier with a standard deviation of ~ 2.7 ADC Counts that can be masked in case of interference with the measurements; however, we still consider this value reasonable. Both the mean and the standard deviation values are within the expectation.

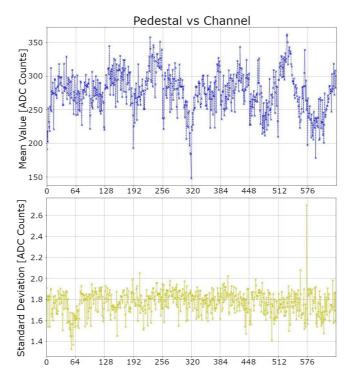


Fig. 5. Mean value (a) and standard deviation (b) for the pedestal of a single 640-channel detector.

V. CONCLUSIONS

We successfully designed the Micro-Strip Detector data acquisition system which sustains a maximum trigger rate of 2 kHz, above the foreseen one for the entire FOOT. With this DAQ system we read out three MSD x-y planes and analyzed their pedestals output, showing no issues. We also acquired data in several dedicated tests in particle beams, that will be discussed in future publications.

We will further develop the system by designing a data compression custom algorithm to optimize the data transfer rate and to improve the maximum sustainable trigger rate. We also plan to extend the system's characterization with tests and analyses in more complex set-ups.

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