On the breakdown voltage temperature dependence of high-voltage power diodes passivated with diamond-like carbon

On the Breakdown Voltage Temperature Dependence of High-Voltage Power Diodes Passivated with Diamond-Like Carbon

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***Abstract*—Diamond-Like Carbon (DLC) is well established material for the passivation of high voltage negative bevelled power diode. In our previous works, the conduction mechanism of the DLC has been carefully described through the characterization and the physical modelling of Metal-Insulator-Semiconductor (MIS) structures. In addition, the effects on the breakdown voltage and leakage current have been clarified comparing the available experiments with numerical simulations. However, the role played by the DLC on the breakdown voltage temperature dependence is still lacking. In this work, we addressed the latter issue and found out an anomalous reduction of the temperature dependence which is clearly ascribed to the DLC behaviour. The temperature dependencies of carrier transport in the DLC have been further investigated in order to explain the experimental results. The observed effect might be related to the release of the trapped charges with increasing temperatures or to a different temperature dependence of the DLC mobility which is function of the distance from the Si/DLC interface. TCAD simulations are used to corroborate such assumptions.**

***Index Terms*—Diamond-Like Carbon, Power diode, Junction Termination, Breakdown Voltage**

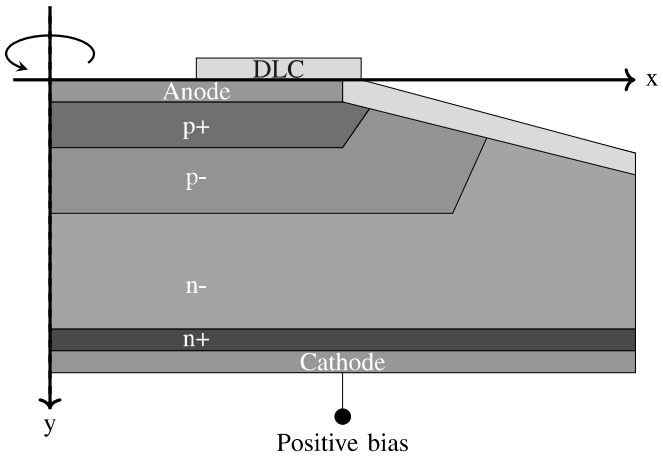

Fig. 1. Schematic representation of a power diode with negative bevel termination and DLC as passivation layer. Structure not in scale

I. Introduction

The ability to predict the breakdown voltage (BV) of negative bevelled large-area power diodes up to the maximum allowed junction temperature is fundamental to guarantee the most accurate design for high blocking capability in any operating regime. The most critical region is the bevel junction termination which is realized by cutting the device with a diamond blade. The large number of defects coming from the wafer sawing results in a significant and unpredictable amount of fixed charge on the bevel surface. The latter negatively affects the stability of the breakdown voltage and the long-term reliability of the device. This is confirmed by comparing one dimensional simulations of the ideal pn junction with 2D simulations of the bevelled diode with an ideal SiO_2 passivation. In the former case, the avalanche condition at room temperature is reached at 6800V (ideal 1D-BV)) while in the latter it occurs at 5650V. Diode manufactured without passivation exhibits an even lower BV, as low as approximately 5300V, together with a very high leakage current due to the large number of defects on the bevel surface [1]. For this reason, the role played by the material deposited on the bevel termination is fundamental to obtain a stable and high BV [2]. From a physical standpoint, the passivation material not only helps to reduce the damage along the bevel surface but also provides a uniform and tunable amount of fixed charge improving the blocking capability by lowering the undesired electric-field peaks. Recently, DLC has been demonstrated to be a very promising passivation material since it allows to obtain BV very close to the theoretical limit of the 1D-BV with a high reproducibility. From previous measurements, an increased blocking capability, up to 6400V, has been found at room temperature together with a much lower leakage current [1]. However, new experimental data show that when DLC is used as passivation material the BV exhibits a weaker temperature dependence when compared to the theoretical silicon bulk material where a strong increase of the breakdown

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voltage with temperature is expected from the reduction of the impact ionization generation coefficients [3] [4]. ~~The latter results partially limits the advantage of the DLC at large temperatures.~~ A TCAD model which describes the DLC electrical features accounting for both its electrostatic properties and its main charge transport mechanism has been already developed [5] [6]. Starting from it, the blocking capability at high temperatures has been investigated here for the first time. In this work, two different approaches are proposed to extend the validity of the existing model to predict the anomalous BV temperature dependence: (i) by accounting for the charge de-trapping at high temperatures using a temperature-dependent doping concentration; (ii) by assuming that different Poole-Frenkel activation energies must be used into the DLC layer depending on the distance from the Si/DLC interface.

II. Role of the DLC passivation and TCAD model

The device under test is a 4.5kV negatively-beveled high voltage diode with a diameter of 90mm as schematically represented in Fig.1. The DLC has been used as passivation layer directly in contact with the junction termination. The 2D radial cross-section has been simulated with the TCAD tool assuming cylindrical coordinates [7]. The SRH lifetimes have been fitted against the reverse leakage current curves measured at different temperatures when an undoped DLC was used as passivation layer. Finally, the silicon impact ionization generation has been accounted for by using the Van Overstraeten model with default parameters.

The charge transport in DLC, due to its amorphous nature, is dominated by the trap-to-trap hopping as confirmed by the Poole-Frenkel-like conductivity observed in MIS and MIM structures [5] [6] [8] [9]. It can be expressed as [10]:

$$\sigma \propto \exp\left\{-\frac{q}{k_B T}\left[\Phi - \sqrt{\left(\frac{qE}{\pi\varepsilon_r\varepsilon_0}\right)}\right]\right\} \tag{1}$$

With Φ the barrier height, k_B the Boltzmann constant, T the absolute temperature, q the elementary charge, E the electric field, ε_0 and ε_r the vacuum and the relative dielectric constant respectively. In the framework of the TCAD simulator, the DLC is modelled by using the drift-diffusion (DD) transport equation with two symmetric Gaussian density of states (G-DOS), one for each charge carrier. Electron G-DOS is thus given by [11] [12] [13]:

$$\Gamma(E) = \frac{N_t}{\sqrt{2\pi}\sigma}\exp\left[-\frac{(E-E_0)^2}{2\sigma^2}\right], \tag{2}$$

where N_t is the concentration of hopping states, σ the standard deviation and E_0 the energy shift with respect to the conduction band. The electron concentration is calculated by performing the Gauss-Fermi integrals:

$$n = \int \Gamma(E) f(E) dE \tag{3}$$

where $f(E)$ is the Fermi-Dirac distribution. Similar expressions and considerations with respect to the valence band can be made for the hole concentration p. As shown by [11], the temperature dependence of n and p is strongly affected by σ. In particular, larger values of the standard deviation lead to a weaker increase of n and p with T. The trap-to-trap hopping is emulated by using the Pool-Frenkel-like mobility model, as available in the simulator. It can be expressed as:

$$\mu = \mu_0 exp\left(-\frac{E_a}{k_B T}\right) exp\left(\frac{\beta\sqrt{E}}{T}\right) \tag{4}$$

where μ_0 is the low-field mobility, E_a is the activation energy of the hopping carriers and β is a fitting parameter.

The polarization effect has been accounted for by using the first-order Debye equation of the ferroelectric model. In addition, a two-layer DLC stack has been assumed with a first interface layer of about 70nm identified using TEM images. All the parameters of the models described so far have been chosen according to experimental evidence or theoretical considerations as detailed discussed in [6]. The I-V curves of DLC passivated power diodes under reverse-bias condition are reported in Figs. 2, 3 and 4. The values of the corresponding breakdown voltage are collected in Fig. 5 and have been used as reference for TCAD simulations. At room temperature, error bars have been extracted using a set of 40 devices: 20 of them have been passivated with the undoped DLC, 10 with the N-DLC and 10 with the B-DLC. However, at higher temperature, experiments are available only for the reference diodes corresponding to Figs. 2, 3 and 4. It can be assumed that the error bars on the BV are constant in the whole temperatures range. In our previous works [6], it has been demonstrated that BV is affected almost exclusively by the amount of fixed charge available in the DLC layer originating from the depletion condition experienced by the doped DLC. As observed also in other amorphous materials

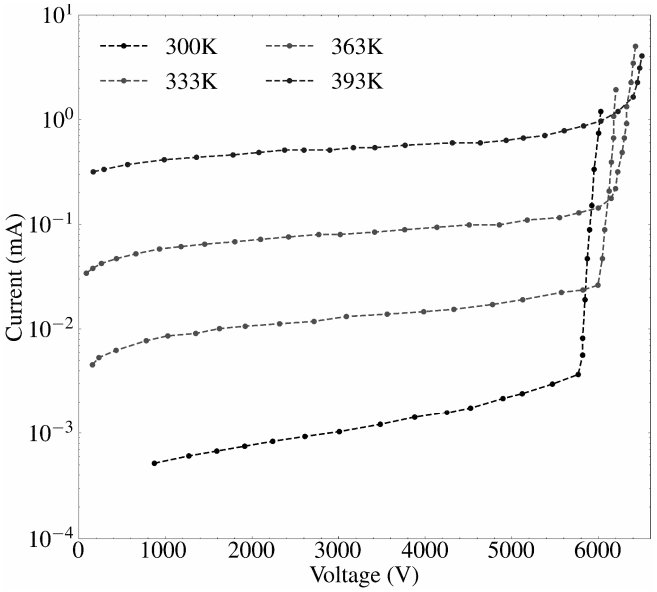

Fig. 2. IV curves corresponding to measurements on a single power diode passivated with undoped DLC under reverse-bias condition for different ambient temperature.

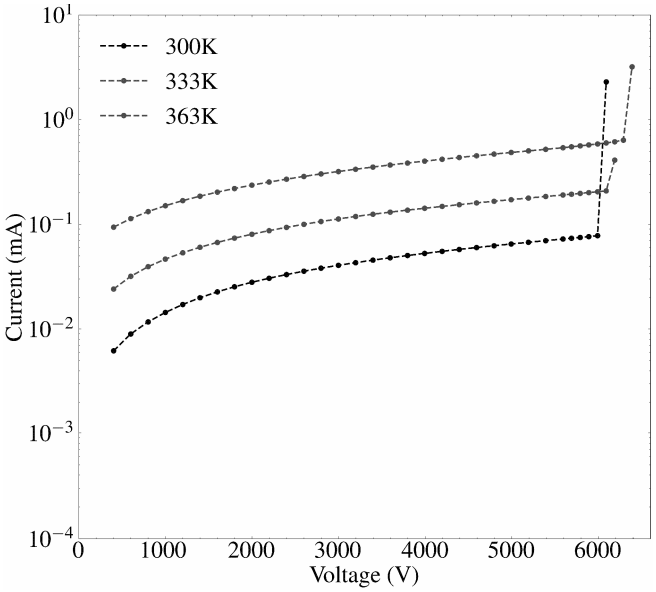

Fig. 3. IV curves corresponding to measurements on a single power diode passivated with N-DLC under reverse-bias condition for different ambient temperature.

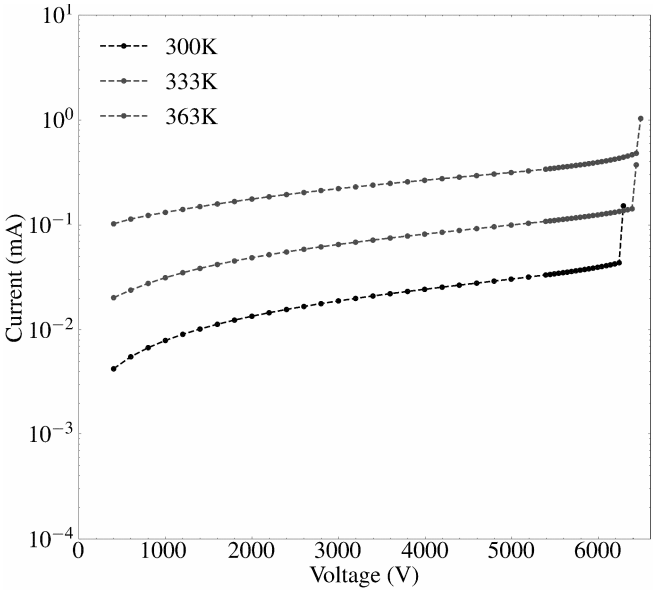

Fig. 4. IV curves corresponding to measurements on a single power diode passivated with B-DLC under reverse-bias condition for different ambient temperature.

[14] [15], at high temperature trapped charges can acquire enough energy to overcome the barrier and, as a consequence, the amount of fixed charge available to modify the depletion region width along the bevel is drastically reduced. This leads to a limited increase of the BV with temperature. The temperature dependence of the leakage current shows similar features as discussed in [6]. Once all the traps are free the charge carrier concentration can not further increases

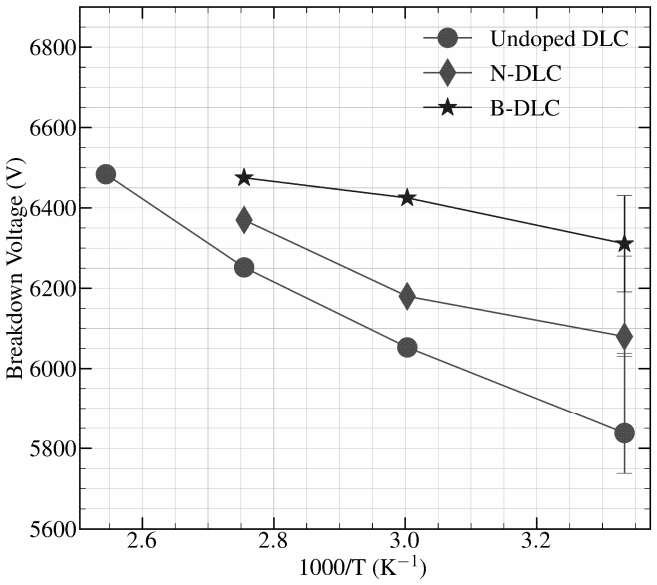

Fig. 5. Breakdown voltage of DLC passivated power diodes extracted from Figs. 2, 3 and 4. Error bars show the upper and the lower value of the breakdown voltage observed by measuring several samples.

leading to a saturation of the DLC conductivity. As shown in the next section, assuming a temperature dependent doping concentration, it is possible to emulate the charge de-trapping inside the DLC passivation layer. In addition to this, another assumption can be made, which comes from the different resistivity observed in vertical and lateral DLC conductivities. If the DLC2 layer exhibits a lower activation energy when compared with the DLC1, the interlayer effect vanishes at higher temperatures thus limiting the increase of BV.

III. Simulations results and comparison with experiments

Metal-Insulator-Semiconductor (MIS) test structures have been used to identify the main charge transport features in the DLC layers and the properties of the Si/DLC interface. The DLC is deposited on a lightly doped n-type or p-type silicon substrate following the same process steps used for the passivation of the negative bevel junction termination. In this way, it is possible to correlate the vertical features of the reverse-bias condition of the MIS diode to the corresponding region along the bevelled interface of the real power diode. Top and bottom metal contacts have been realized with Aluminium. Different recipes of the passivation layer have been tested, namely, undoped DLC, Nitrogen-doped DLC (N-DLC) and the Boron-doped DLC (B-DLC) [5] [6]. The schematic view of the test structures is reported in Fig. 6. The top layer (DLC2) was modelled by simply assuming a 100 times larger carrier mobility at low filed with respect to the interfacial layer DLC1 [6]. The JV curves have been obtained by measuring the current as a function of the top electrode bias for different ambient temperatures [6]. As an example, the JV curves for the MIS structure with n-type and p-type silicon bulk and B-DLC

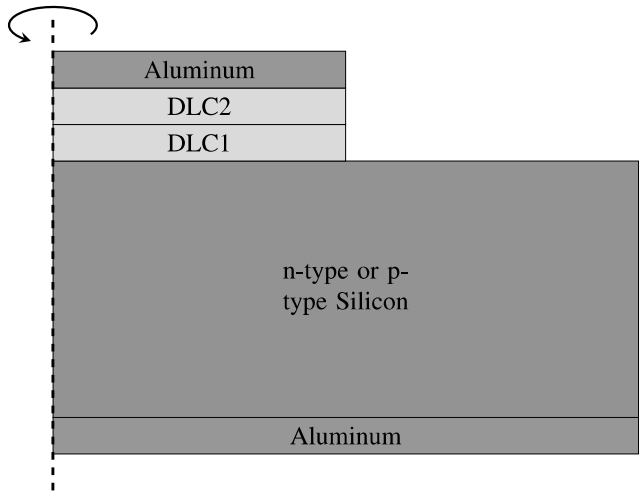

Fig. 6. Schematic view of the cross-section of a Metal-DLC-Si device. The structure is not in scale. TCAD simulations were carried out with a cylindrical symmetry in order to predict the current spreading in the Si substrate.

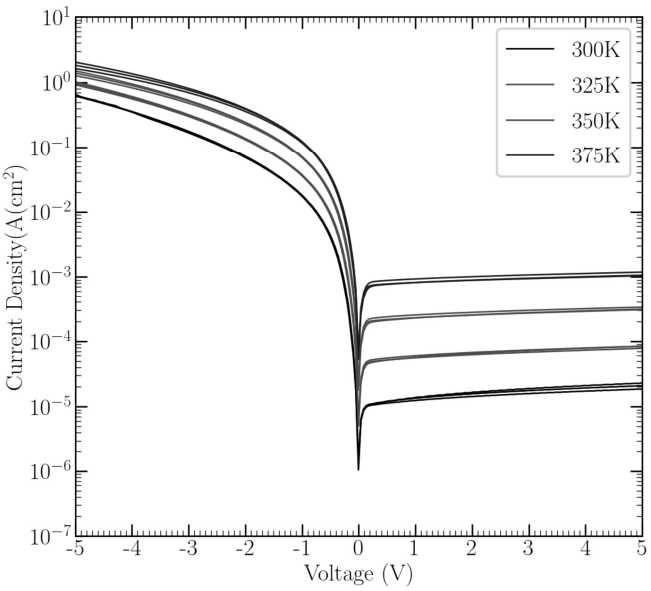

Fig. 7. J-V curves of MIS structures with p-type silicon substrate and B-DLC at different temperatures.Measurements on three different samples have been reported to show the negligible experimental error.

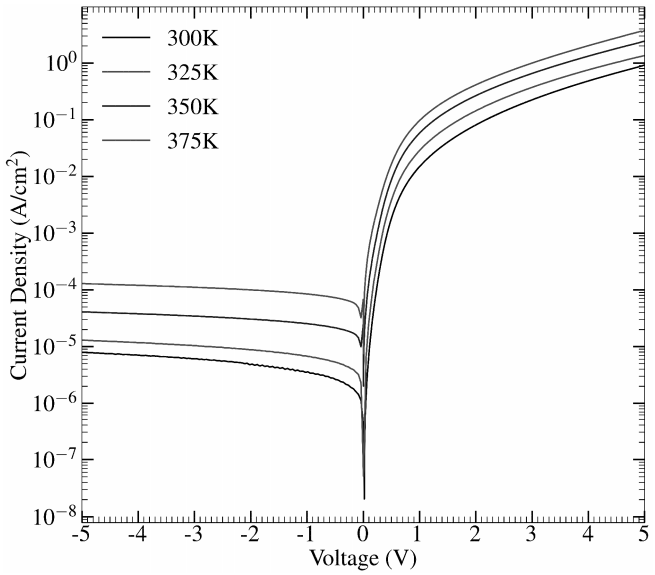

Fig. 8. Averaged J-V curves of MIS structures with n-type silicon substrate and B-DLC at different temperatures. The average has been calculated by using measurements performed on three different samples (not shown).

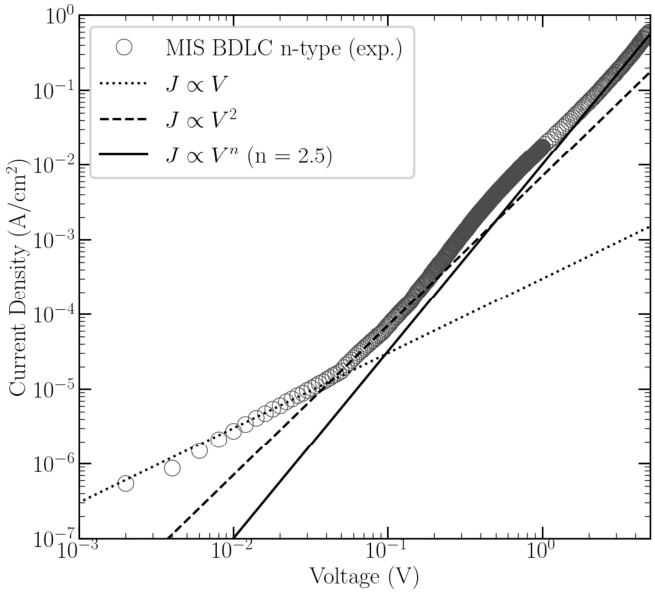

Fig. 9. Forward bias J-V curve corresponding to Fig. 8 at T = 300K. Black lines show the different transport regimes.

are shown in Figs. 8 and 7. When a positive voltage is applied on the top electrode electrons move from silicon toward the DLC layer. In the forward bias condition, which is experienced by the n-type Si structure, the DLC resistance is higher than the silicon one and dominates on the device conductivity. Vice-versa, in the p-type Si structure, the depleted region in silicon shows a higher resistance and limits the current density. The same considerations apply symmetrically for the negative voltage case. Three different regions can be observed from the J-V curves in forward bias [5]: an Ohmic region where $J \sim V$, a space charge limited current (SCLC) region where $J \sim V^2$ and a space charge limited current region enhanced by the Poole-Frenkel field emission with a slope grater than 2 ($J \sim V^n$, with $n > 2$). As an example, the forward bias J-V curveat room temperature shown in Fig. 8 at 300K is reported in Fig. 9 in a log-log plot. Fitting curves correspond to the three different transport regimes showing the validity ranges of each of them confirming the expected roles. Under reverse

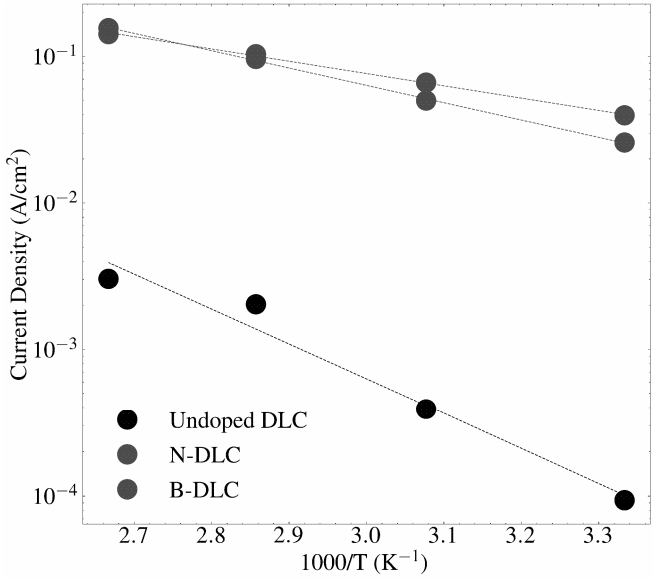

Fig. 10. Current density of MIS structure with n-type Si substrate under forward bias condition extracted at +1.25V for different temperatures and different DLC recipes. Symbols: experiments. Dashed lines: exponential fitting

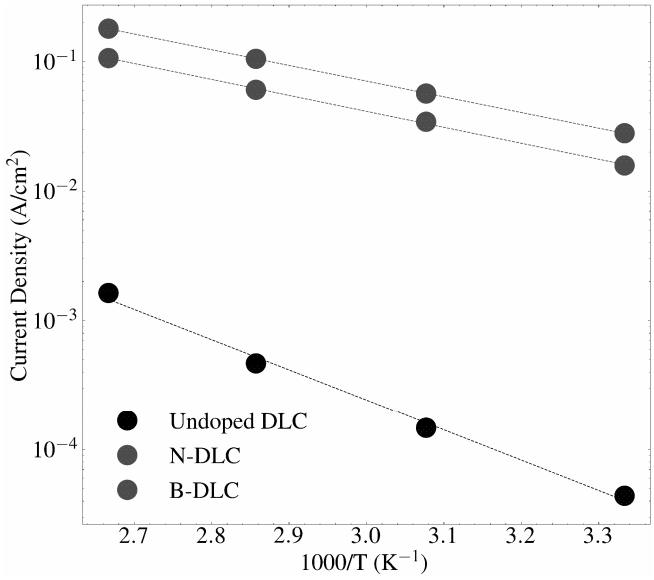

Fig. 11. Current density of MIS structure with p-type Si substrate under forward bias condition extracted at -1.25V for different temperatures and different DLC recipes. Symbols: experiments. Dashed lines: exponential fitting

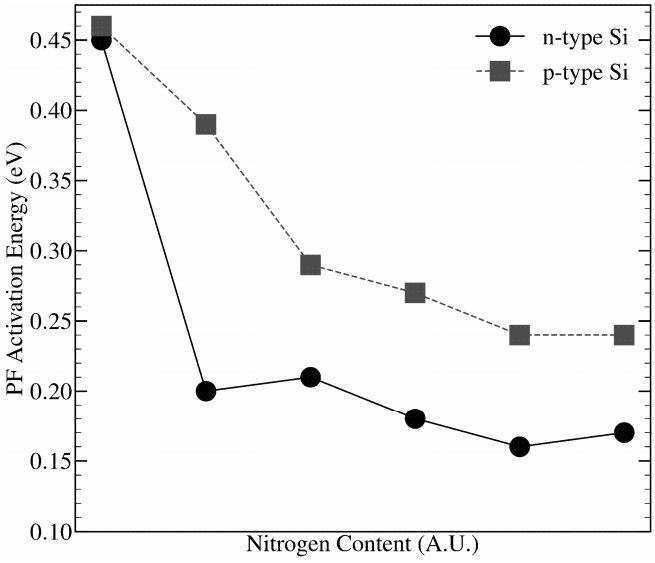

Fig. 12. Poole-Frenkel activation energy extracted from the forward bias JV curves of MIS structure with N-DLC on top for different Nitrogen concentration and different substrate doping type.

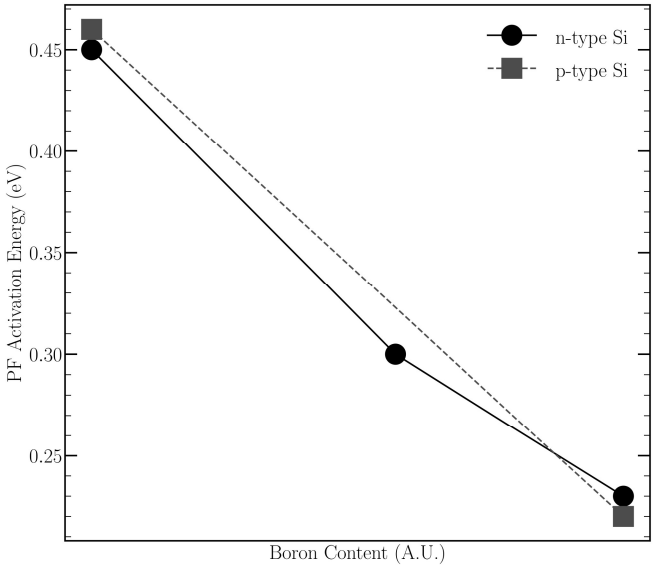

Fig. 13. Poole-Frenkel activation energy extracted from the forward bias JV curves of MIS structure with B-DLC on top for different Nitrogen concentration and different substrate doping type.

bias condition, the MIS structure shows a current saturation: the Si depletion region is formed in the silicon substrate and widens with the increase of the reverse bias. Its resistivity becomes larger than the DLC-layer one, so that the whole potential drops across the substrate and the resulting current is quite constant. Different doping types of the silicon substrate have been considered in order to understand the role played by both types of carriers on the DLC conductivity. In [6], it has been observed that the current contribution due to the electrons or holes injected from the top metal is almost equivalent, independently of the differently doped silicon substrates at the bottom. Morover, the role of the metal on top was investigated by means of measurements carried out on MIS with different metallization on top. It has been assumed that the large number of states inside the energy gap of the DLC pin the Fermi level at the metal/DLC interface independently of the metal workfunction [6] [16].

The forward-bias current densities extracted at $\pm$1.25V for the n-type and p-type silicon substrates are reported in Figs.

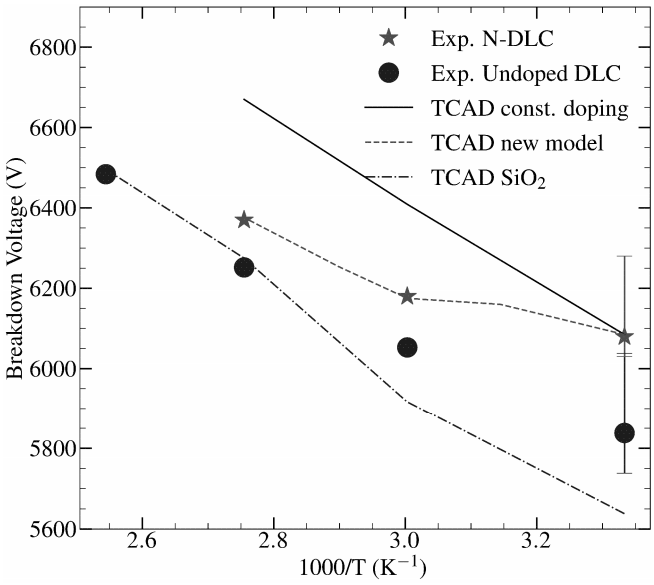

Fig. 14. Breakdown voltage of negative bevelled power diode with N-DLC as passivation. Error bars refer to room temperature measurements shown in Fig. 5. Symbols: experiments. lines: TCAD simulations

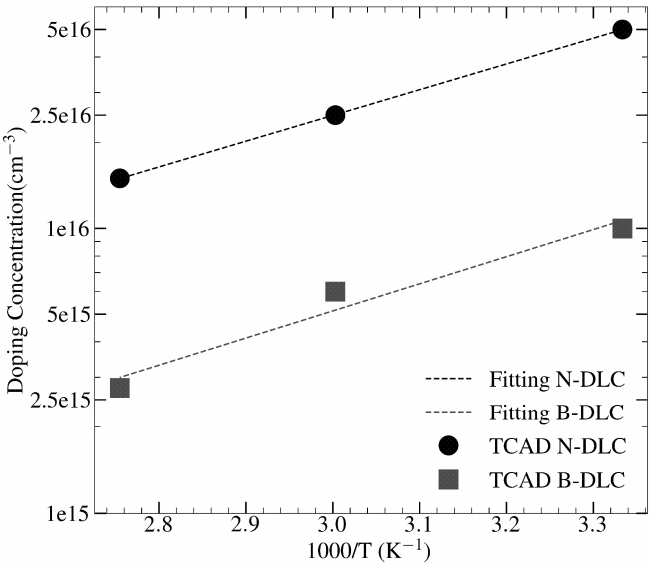

Fig. 16. DLC Doping concentration as function of temperature. Symbols: doping concentration at different temperatures. Dashed lines: exponential fitting.

10 and 11, respectively. All the different DLC recipes show an Arrhenius-like temperature dependence. The value of the applied voltage is well above the onset of the space-charge limited current, but it is low enough to neglect the energy barrier lowering due to the local electric field in the Poole-Frenkel conductivity equation.

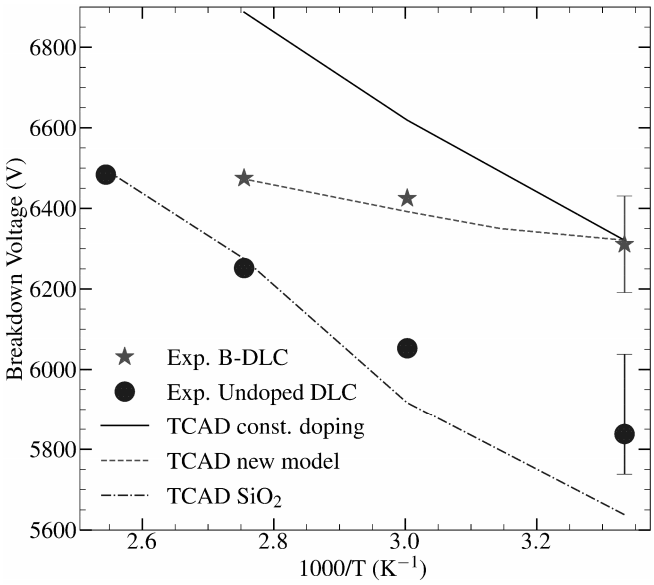

Fig. 15. Breakdown voltage of negative bevelled power diode with B-DLC as passivation. Error bars refer to room temperature measurements shown in Fig. 5. Symbols: experiments. Lines: TCAD simulations

The extracted activation energies of the forward-bias curves of MIS structures with different DLC recipes and substrate doping type are reported in Figs. 12 and 13 and are in perfect agreement with those used in the simulator setup [6]. It can be clearly observed that the undoped DLC shows a higher activation energy when compared with the doped cases (N-DLC, B-DLC) [17]. According with Eq. 1, a lower value of the effective energy barrier Φ results in a higher trap emission probability. The amount of trapped charges then might rapidly decrease with temperature. This effect can play a role in the control of the electrostatics for the diode at large reverse bias conditions. It is expected that, due to a decrease of trapped charge, the depletion region width would reduce to that of the undoped case. This explain a lower temperature dependence of the breakdown voltage.

In Figs. 14 and 15, the measured BV as function of the ambient temperature are compared with TCAD simulations. The undoped DLC behaves as a lightly doped p-type semiconductor [18] [19] and provides a small amount of negative trapped charge which results in a slightly increase of the BV at low temperatures when compared with simulations with ideal SiO_2. At higher temperatures, for doped DLCs, the TCAD predictions show an overestimation of BV. The experimental reduction can be explained assuming that traps tend to empty above 300K [20]. In order to reproduce this feature through TCAD simulations, that the doping concentration is a decreasing function of temperature following an exponential curve as shown in Fig. 16. In Figs. 17 and 18, the 2D contour plots of the electrostatic potential close to the junction termination are reported for a constant doping concentration and the new reported temperature dependent one, respectively. The width of the depletion region along the bevel is lowered in the second case due to the reduced doping concentration. Up to now, we assumed that the ratio between the low-field mobilities of the

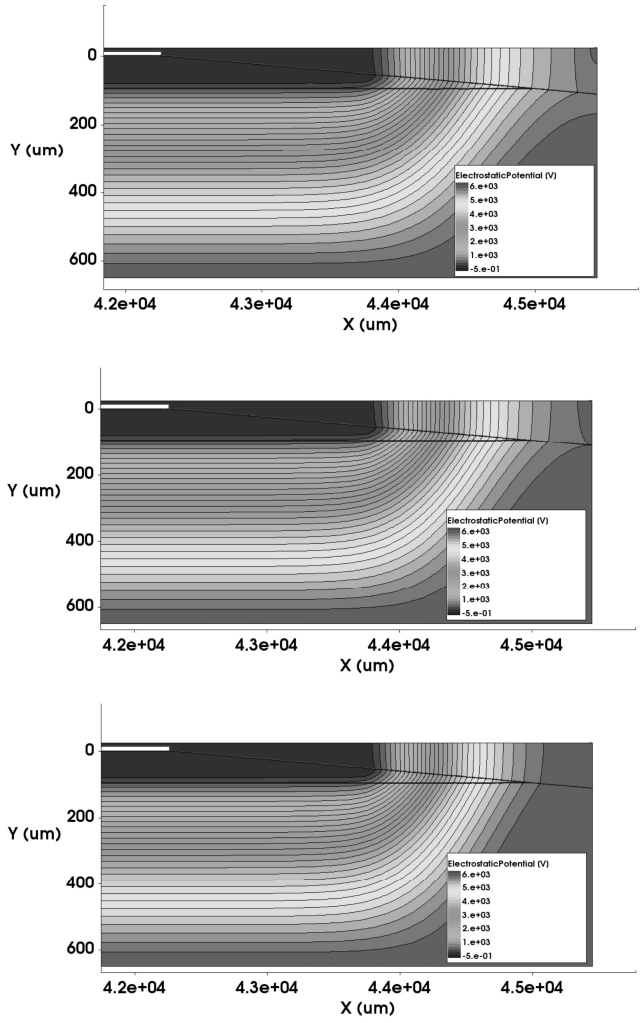

Fig. 17. 2D Contour plot of the electrostatic potential of the diode with B-DLC for three different temperatures using a constant doping concentration. Top: 300K, Middle: 333K, Bottom: 363K

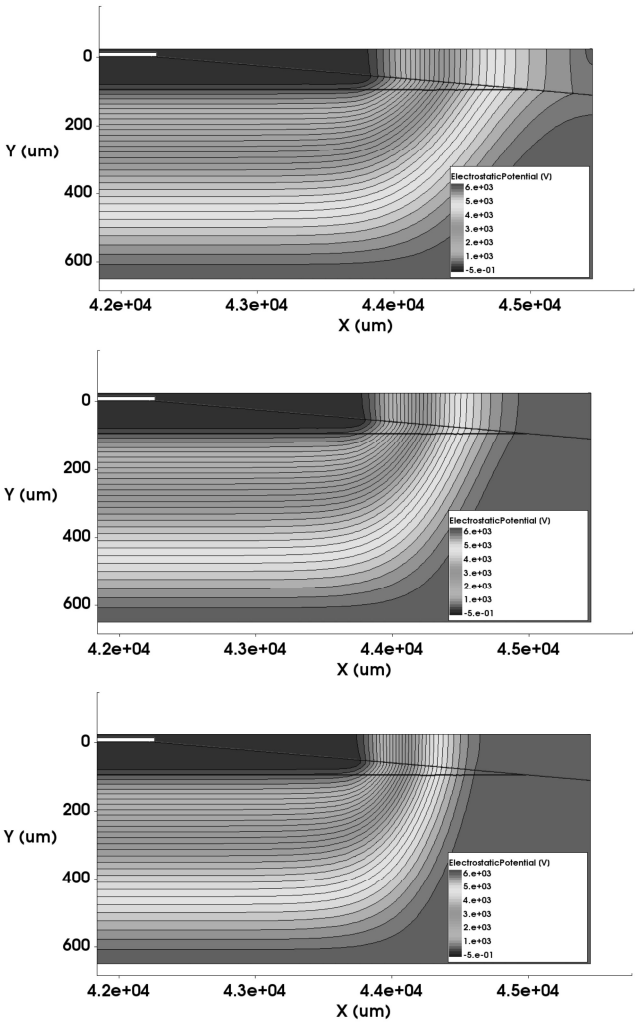

Fig. 18. 2D Contour plot of the electrostatic potential of the diode with B-DLC for three different temperatures using a variable doping concentration. Top: 300K, Middle: 333K, Bottom: 363K

two DLC layers was independent of temperature. However, assuming different activation energies for DLC1 and DLC2, the temperature dependence of the BV voltage can be modified as shown in Fig. 19. In particular, the barrier height Φ of DLC2 has been changed in a range from 0 to 0.23 eV. Such a difference can be due to the different physical properties of the two layers leading to a different hopping transport condition. When the ratio between the two mobilities is high the charge carriers mainly flow in the top region of the DLC leaving the underlying layer effectively more depleted. The excess of positive/negative space charge close to the Si/DLC interface acts on the width of the space charge region along the bevel as discussed before. However, when the mobility of the DLC1 approaches that of the DLC2 due to the increase of temperature, the current density is uniformly distributed in the DLC layers giving rise to a lower amount of space charge, which results in a lower breakdown voltage of the power diode.

IV. Conclusion

The temperature dependence of the breakdown voltage of negatively bevelled power diodes was shown to be lower than the silicon one when passivated with DLC. However, a DLC passivation provides, in the whole temperature range, an improvement of the blocking capability when compared with non-passivated devices or diodes simulated with an ideal SiO_2 passivation. This is especially true at low temperatures, where higher impact ionization rates lead to a lower blocking capability.

The aim of this work, was to provide a physical explanation of the temperature dependences for the reference diode featuring the DLC passivation up to breakdown. To this purpose the validity of the TCAD setup for the DLC material was extended to the temperature analysis. Two different approaches have been proposed: (i) a temperature dependent doping concen-

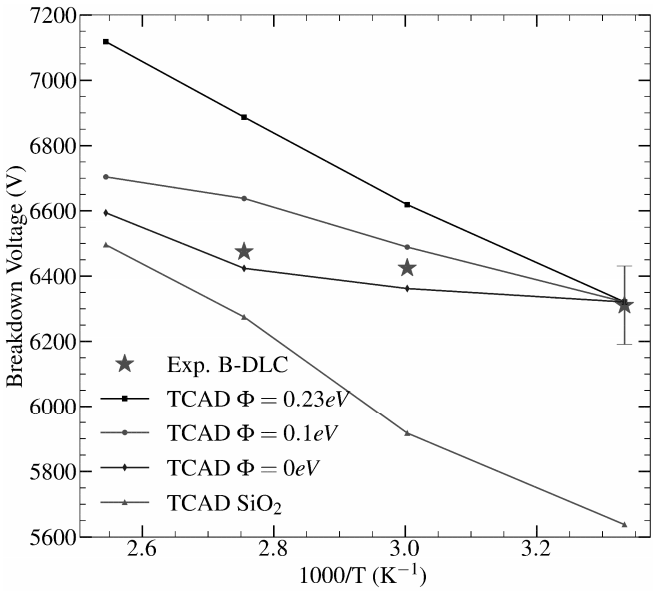

Fig. 19. Breakdown voltage of negative beveled power diode with B-DLC as passivation. TCAD simulations refer to different value of the barrier height Φ in the DLC2 layer.The DLC1 has $\Phi = 0.23eV$ in all simulations. Error bars refer to room temperature measurements shown in Fig. 5. Symbols: experiments. Lines: TCAD simulations

tration which emulates a reduction of the trapped charges as the temperature increases, as predicted by the Poole-Frenkel model; (ii) a different temperature dependence of the interface and top DLC layers mobilities. Since neither the space charge nor the temperature dependence of lateral conductivity have been measured so far, it is not possible to fully determine which of the two phenomena is the dominant one. In this perspective, further analysis would be necessary to improve the modelling of the DLC properties and eventually increase the BV at higher temperatures. This could be achieved by tuning the parameters of the DLC deposition process in order to increase the content of substitutional sites in the carbon network. By doing so, higher active doping concentration can be obtained independently on the ambient temperature. In addition, an high mobility ratio between DLC1 and DLC2 should be preserved up to the allowed maximum junction temperature.

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