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TCAD modeling of bias temperature instabilities in SiC MOSFETs

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ABSTRACT

TCAD simulations of SiC power MOSFETs have been performed to study the dependence of positive-bias temperature instability (PBTI) on temperature and electric field. The model used to describe the kinetics of the transition rates between neutral and charged traps is the extended Non-Radiative Multi Phonon (eNMP). Connections between oxide defect configurations at the interface with SiC substrate have been made. Validation against experiments is shown.

1. Introduction

Silicon Carbide is considered as the most promising substrate for power applications. Although the performance of 4H-SiC MOSFET have been significantly improved in the recent years it still suffers for reliability issues due to the presence of numerous near-interface oxide defects [1]. Such defects affect the transistor behavior causing drifts in the values of the transfer characteristics. Therefore, it is necessary to model the charge trapped at the interface in order to predict the impact on threshold voltage (V_{th}), channel mobility and hysteresis. The temperature dependencies of the hysteresis and positive-bias temperature instability (PBTI) have been recently investigated [2–5]. In particular, an anomalous temperature dependence of the V_{th} shift (ΔV_{th}) was observed, which decreases with increasing ambient temperature in contrast to the behavior shown by Si-based MOSFETs [3]. The SiC-MOSFET PBTI was analyzed through ad-hoc simulation software tools and capture/emission time maps (CET) in [5]. In order to understand the role played by the interface degradation in the PBTI curves, a preliminary work was carried out using a commercial TCAD tool and the reaction–diffusion model in [6]. In this work, a different approach has been adopted in the TCAD setup based on the extended Non-Radiative Multi Phonon models (eNMP) allowing to study the correlation between temperature, electric field and capture/emission time constants of the most relevant SiO_2 defects, leading to the correct description of the PBTI stress and recovery curves.

2. TCAD modeling and model calibration

The device used as reference is a planar n-MOSFET with geometry and channel doping taken from [7] (Fig. 1). A p-body retrograde profile with a blocking voltage of 1.3 kV has been used.

2D TCAD simulations at different ambient temperatures have been carried out by using SDevice by Synopsys [8]. Material-specific models for the incomplete ionization and the channel mobility, accounting for the role of Coulomb scattering and surface roughness, have been adopted. Following [2,9], SiO_2 border traps have been assumed as the most relevant contribution to PBTI. To this purpose, oxide defects randomly distributed in the SiO_2 over a maximum distance of 0.8 nm from the SiC interface have been assumed as detailed in the following.

The turn-on characteristics at different ambient temperatures are reported in Fig. 2. It can be noted that the device characteristics at room temperature are dominated by the channel resistive path up to large V_{GS}, while the drift resistance significantly decreases with temperature reducing the transconductance at high V_{GS}.

The TCAD simulations of the PBTI stress have been carried out by adopting the four-state eNMP model available in the TCAD tool, as it has been shown to be the most accurate one to model SiO_2 defects and their interaction with the semiconductor interface [10]. Following [9], three different types of oxide defects have been investigated in SiO_2, based on DFT calculations [11]. As a SiC substrate is used here, the corresponding interactions with such traps are significantly different with respect to those related to Si-based interface, and the most relevant one is an acceptor-like border-trap band, termed shallow trap in [9]. Differently

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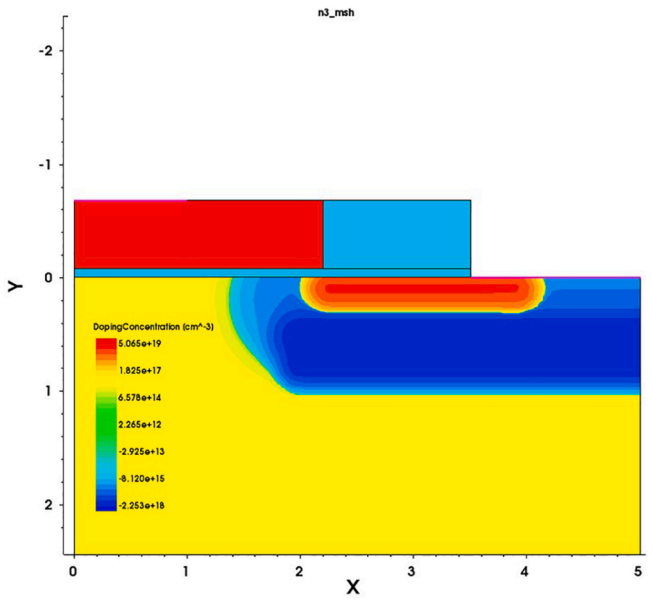

Fig. 1. 2D plot of the SiC-MOSFET structure (half pitch) and doping configuration. The retrograde Al concentration of the p-body is $2x10^{18}$ cm^{-3} and the surface concentration is $5x10^{16}$ cm^{-3} following [7]. The oxide thickness is 80 nm, the gate length is 0.5 μm, the JFET length is 3.0 μm. The TCAD deck was calibrated against experiments as reported in [6].

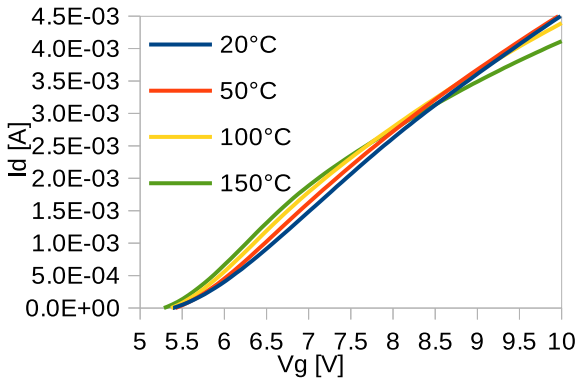

Fig. 2. Simulated turn-on characteristics of the SiC-MOSFET at different ambient temperatures (V_{DS} = 50 mV).

from [9], where a simplified two-state model was used, the four-state eNMP model has been addressed here. In the complete model, the defect can become charged or discharged during a capture or emission event with two stable charge states, labelled as 1 and 2, and two additional metastable states, marked as 1′ and 2′: the whole charge capture or emission process occurs between different charge states but involves a small structural reorganization through one metastable state. A useful picture to understand the general process is given by the representation of the diabatic potentials in the configuration coordinate space, i.e., the nuclear coordinate reference system [11]. The representative diagram of the four-state model for the shallow trap is drawn in Fig. 3 assuming a SiC substrate.

The default parameters of the eNMP model provided in the TCAD deck are related to hole transitions in donor-like traps at the Si/SiO_2 interface. Therefore, the model has been extended through the implementation of a C++ code in the frame of the physical model interface (PMI) [8]. The C++ code allows to define an acceptor-type trap, the electron transitions from the conduction band and the specific eight eNMP transition rates accounting for the SiC conduction band as the reference energy. Moreover, the eNMP model uses a random sampling

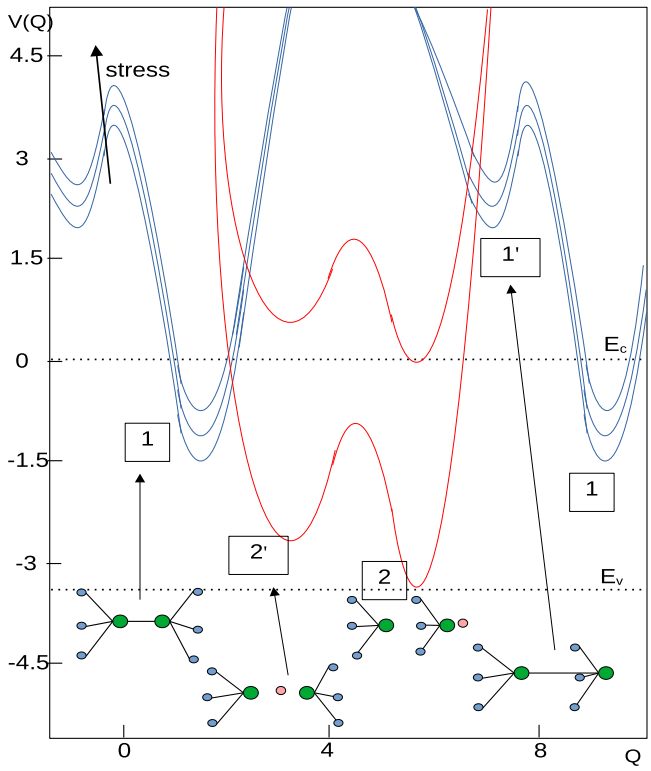

Fig. 3. Schematic configuration coordinate diagram of the diabatic potential of the defect in its neutral (blu solid line) and charged state (red solid line). Bottom: defect configurations for each state. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

technique to obtain the average behavior of multiple defects (a border trap band in the SiO_2). To this purpose, a precursor concentration is assumed at the interface, with a Gaussian distribution for the energy parameters and a trap depth, x_t, uniformly distributed within a range from 0 to 0.8 nm from the SiC/SiO_2 interface.

The defect-band parameters which need to be defined in the eNMP model are graphically reported in Fig. 4. They are:

- E_t, E_t', the energy levels of the defect in the neutral stable/metastable state;
- $R_1 = \omega_1/\omega_{2'}$, $R_2 = \omega_{1'}/\omega_2$, the vibrational frequencies of the states $1 \leftrightarrow 2'$ and $1' \leftrightarrow 2$;
- $S_i\hbar\omega_i$, the relaxation energies where S_i are known as Huang-Rhys factors;
- $\varepsilon_{T2'}$, the energy of the positive metastable state relative to the positive stable state;
- $\varepsilon_{1'1}$, $\varepsilon_{2'2}$, the transition barriers between states $1' \leftrightarrow 1$ and $2' \leftrightarrow 2$, respectively.

Moreover, the following parameters for electrons in SiC need to be defined:

- σ_0, the capture cross-section;
- υ_{th}, the thermal velocity;
- x_0, the tunneling length;
- υ_0, the attempt frequency.

The parameters which have been used to effectively calibrate the model against experiments are the precursor concentration and the capture cross-section, which might be related to the specific processes of each technology. All other parameters have been fixed to values taken directly from the literature [9,11,12] or, eventually, slightly adjusted to

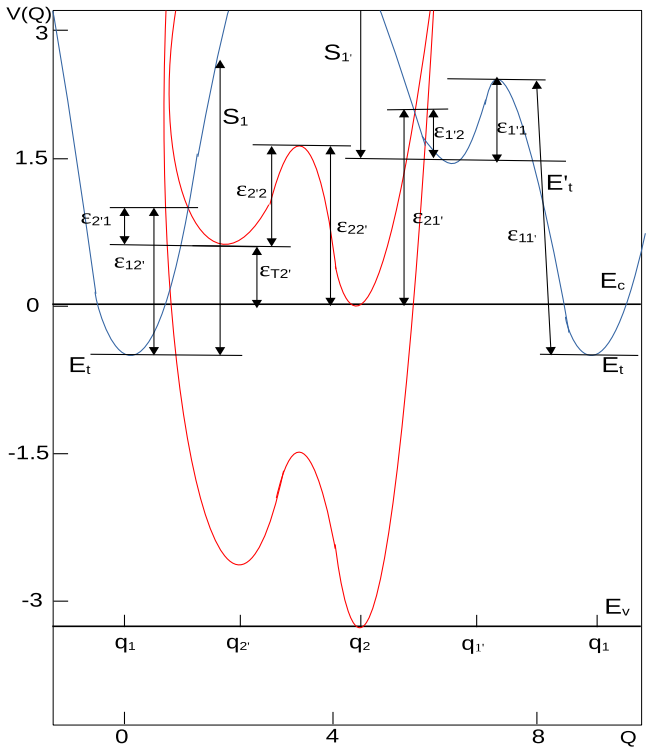

Fig. 4. Top: energy defect levels and their corresponding energetic transitional barriers between the four states as reported in the TCAD eNMP model. Bottom: band diagram of the SiC/SiO_2 interface with the ground state defect level.

improve the model prediction against experiments, as reported in Tables 1 and 2. More specifically, with respect to the calculated SiO_2 defects, a slight shift of the defect energies can be ascribed to the presence of Carbon at the SiC/SiO_2 interface with respect to the Si/SiO_2 one. Recent results on related DFT calculations have been taken into account [13,14]: the trap position E_t has been fixed to a value consistent with the SiO_2-C-O defect shown in [13], which is also compatible with the Silicon interstitial defects of [14].

3. Results and discussion

A comparison with experimental data has been finally used to validate the proposed model and to further understand the PBTI trends at different biases and temperatures.

The power spectral density (PSD) of the drain current in linear regime has been measured at $V_{DS} = 50$ mV and V_{GS} varying between 3.4 V and 5 V, in order to distinguish between carrier and mobility fluctuations and to correlate such contributions to the distributed oxide defects. The PSD of the drain current increases by decreasing the frequency following a $1/f^{\gamma}$ law, with γ of about 0.75 (Fig. 5), which is consistent with a trap distribution in the oxide region increasing towards the

Table 1
Defect band parameters. E_t and $E_{t'}$ are referred to the SiC conduction band minimum.

Symbol	Mean	Standard deviation	Unit
E_t	−0.546	0.26	eV
E'_t	0.13	0.33	eV
R_1	1.27	0.09	1
R_2	1.04	0.28	1
$S_1\hbar\omega_1$	2.68	0.41	eV
$S_2\hbar\omega_2$	1.62	0.65	eV
$\varepsilon_{T2'}$	0.11	0.49	eV
$\varepsilon_{1'1}$	2.91	0.78	eV
$\varepsilon_{2'2}$	0.113	0.49	eV

Table 2
eNMP parameters that have separate values for electrons and holes.

Symbol	Electron Value	Hole Value	Unit
σ_0	1.0×10^{-17}	1.0×10^{-15}	cm^2
υ_{th}	1.5×10^{7}	1.2×10^{7}	cm/s
x_0	0.08	0.08	nm
υ_0	1.0×10^{13}	1.0×10^{13}	s^{-1}

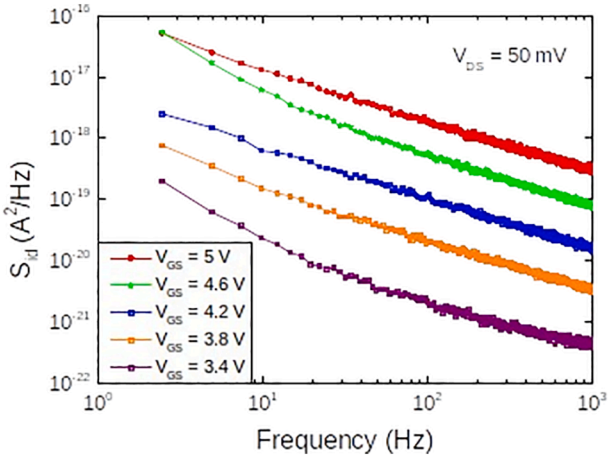

Fig. 5. Measured PSD of drain current in a SiC MOSFET biased in linear regime for different gate voltages.

interface with the semiconductor [15].

The drain current noise normalized with respect to the square of the DC drain current at a fixed frequency of 100 Hz is then plotted against the gate voltage overdrive in Fig. 6 for different devices. Experimental data are fitted with the function $S_{id}/I_D^2 \propto |V_{GS} - V_T|^{\alpha}$. The slope α of this plot gives information about the fundamental fluctuation mechanism. Since the slope is close to – 2 for all investigated samples, as reported in Table 3, number fluctuation can be assumed as the source of noise for the drain current, thus supporting our interpretation that the BTI is mostly given by the charge trapping due to the eNMP transitions.

As far as the PBTI analysis is concerned, the experimental data in [16] have been taken as reference. A qualitative agreement with experiments is expected with some discrepancies due to the lack of information on the specific technology of the measured device. The acceptor-like border trap implemented in the four-state eNMP model is shown to be the most relevant one for the prediction of the PBTI stress at different V_{GS} biases (Fig. 7). TCAD simulations have been also carried

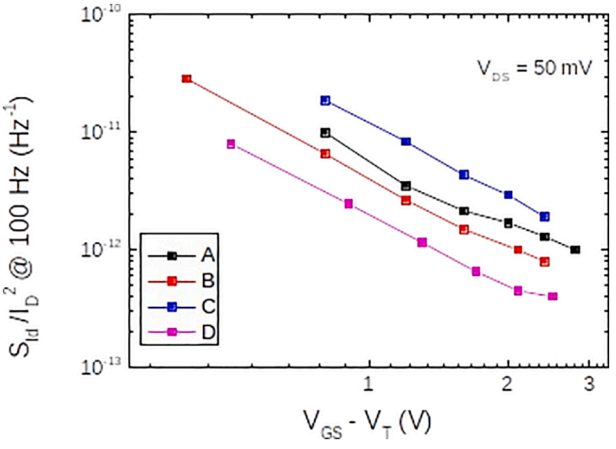

Fig. 6. Normalized drain current noise at a fixed frequency of 100 Hz as a function of gate voltage overdrive for different devices (A, B, C and D).

Table 3
Slopes of the curves shown in Fig. 6.

Device	Slope
A	−1.76
B	−2.04
C	−2.07
D	−1.93

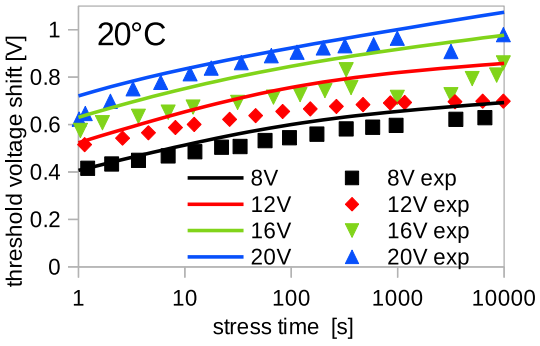

Fig. 7. Threshold voltage shift as a function of stress time at different V_{GS} stress voltages. TCAD simulations (continuous lines) are in nice agreement with experiments at room temperature (filled symbols).

out at different temperatures, clearly showing that ΔV_{th} significantly reduces with increasing temperature (Fig. 8). In order to check the predictivity of the proposed defect-band model, the PBTI recovery curves at different temperatures have been also simulated, showing a good agreement with experiments, therefore validating the physical assumptions adopted in this work (Fig. 9). The Δv_{th} curves at larger T are slightly underestimated, which might be ascribed to the concurrent effect of different traps as shown in [9].

In the full eNMP model, the choice of the mapping scheme for the stable and metastable levels affects the energy barriers experienced by electrons in their transitions. The adopted configuration nicely explains the most relevant trends in terms of capture and emission rates. In particular, the electron emission proceeds through the metastable state 2′, via a thermally activated transition. Therefore, at higher temperatures the emission rate grows faster than the capture one.

As an example, the interface charge obtained from the ensemble average of the oxide charge states at different V_{GS} and T are reported in Fig. 10, while the predicted hysteresis characteristics at different T are reported in Fig. 11, showing a significant hysteresis reduction with T in accordance with the experimental results [6].

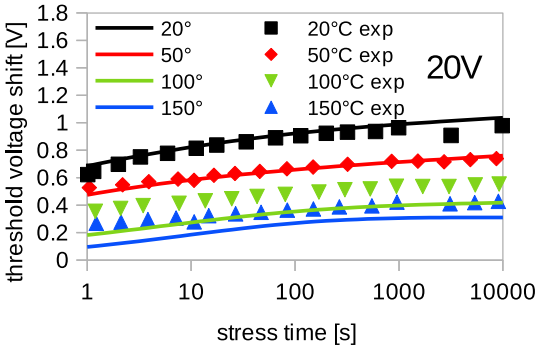

Fig. 8. PBTI-induced ΔV_{th} for different temperatures with $V_{stress} = 8$ V. At larger temperatures ΔV_{th} tends to decrease: TCAD simulations nicely predict such trend.

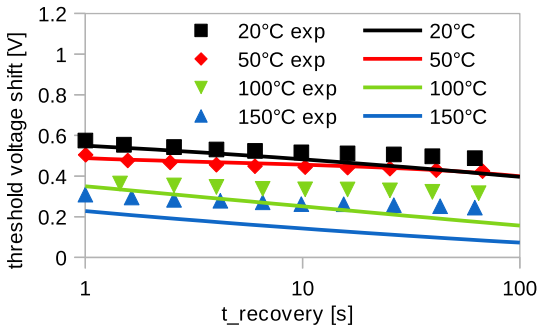

Fig. 9. ΔV_{th} recovery evolution after applying $V_{stress} = 8$ V for $t_{stress} = 10000$ s at different temperatures.

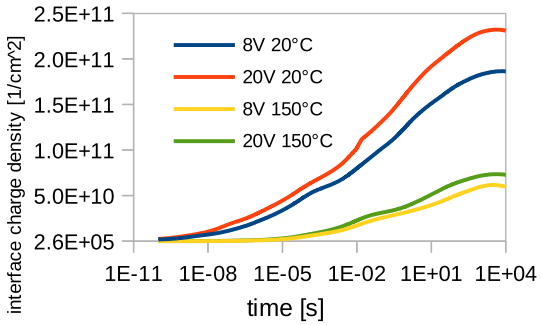

Fig. 10. Interface trap concentration obtained by the eNMP model as a function of stress time for two different stress voltages and temperatures.

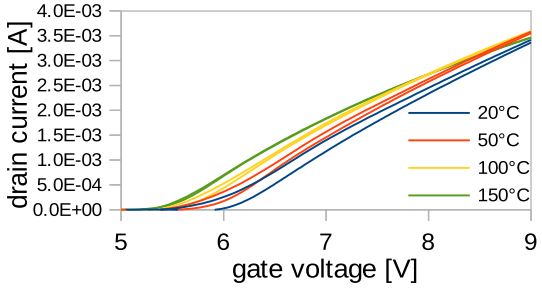

Fig. 11. Top: I_D-V_{GS} hysteresis at different temperatures in SiC-MOSFET. Bottom: mean value of the hysteresis amplitude at $I_D = 5$ mA versus mean value of ΔV_{th} induced by a PBTI stress at $V_{stress} = 20$ V and $t_{stress} = 1$ s at different temperatures. A clear correlation between hysteresis and PBTI is observed.

4. Conclusion

The PBTI of planar SiC MOSFETs has been investigated in this work through experimental data and TCAD simulations. In order to identify the origin of the charge trapping/detrapping and to provide a physically-based explanation, the four-state eNMP model is employed in a commercial TCAD tool. The anomalous PBTI decrease with temperature has been ascribed to the effect of a dominating acceptor-like border-trap in SiO_2, with energy features related to the Carbon atoms. A nice agreement between simulations and experimental results has been achieved, explaining the temperature dependence of PBTI stress and recovery evolutions as well as hysteresis width.

CRediT authorship contribution statement

Greta Carangelo: Conceptualization, Methodology, Software, Formal analysis, Investigation, Data curation, Writing - original draft. **Susanna Reggiani:** Methodology, Formal analysis, Investigation,

Writing - review & editing, Supervision. **Giuseppe Consentino:** Conceptualization, Methodology, Investigation, Formal Analysis. **Felice Crupi:** Conceptualization, Writing - review & editing, Supervision. **Gaudenzio Meneghesso:** Writing - review & editing, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

[1] Puschkarsky K, et al. IEEE TDMR 2018;18:144–53. https://doi.org/10.1109/TDMR.2018.2813063.
[2] Tyaginov SE, et al. IEEE IIRW 2018:1–5. https://doi.org/10.1109/IIRW.2018.8727083.
[3] Puschkarsky K, et al. IEEE TED 2019;66(11):4604–16. https://doi.org/10.1109/TED.2019.2938262.
[4] Vasilev A, et al. IEEE IIRW 2020:1–5. https://doi.org/10.1109/IIRW49815.2020.9312864.
[5] Feil MW, et al. IEEE TED 2021;68(1):236–43. https://doi.org/10.1109/TED.2020.3036321.
[6] Cornigli, et al. IEEE ESSDERC 2019:82–5. https://doi.org/10.1109/ESSDERC.2019.8901761.
[7] Fujihira K, et al. Mater Sci Forum 2007;556–557:827–30.
[8] https://www.synopsys.com/silicon/tcad.html.
[9] Schleich C, et al. IEEE IEDM 2019. https://doi.org/10.1109/IEDM19573.2019.8993446. pp. 20.5.1-20.5.4.
[10] Stathis JH, et al. Microel Reliab 2018;81:244–51. https://doi.org/10.1016/j.microrel.2017.12.035.
[11] Goes W, et al. Microel Reliab 2018;87:286–320. https://doi.org/10.1016/j.microrel.2017.12.021.
[12] Grasser T, et al. IEEE IEDM 2014:530–3. https://doi.org/10.1109/IEDM.2014.7047093.
[13] Waltl M. IEEE IRPS 2020:1–9. https://doi.org/10.1109/IRPS45951.2020.9129539.
[14] Zhang F, et al. Appl Surf Sci 2020;514:145889. https://doi.org/10.1016/j.apsusc.2020.145889.
[15] Jayaraman R, et al. IEEE TED 1990;37(1):305–9. https://doi.org/10.1109/16.43833.
[16] Sanchez L, et al. Microel Reliab 2020;109:113642. https://doi.org/10.1016/j.microrel.2020.113642.

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