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Characterization and numerical analysis of breakdown in thick amorphous SiO_2 capacitors

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***Abstract*—Charge transport in thick amorphous silicon dioxide capacitors for integrated galvanic insulators is experimentally investigated and analyzed through numerical simulations carried out with a commercial TCAD tool. The material intrinsic defectivity and the large biases applied to such devices give rise to a leakage current which is responsible for degradation and failure. Hence it is crucial to have a complete understanding of the charge-transport main physical mechanisms in amorphous silicon oxide. In particular, charge injection at contacts and charge build-up due to trapping/de-trapping mechanisms in the bulk of the oxide are expected to play a crucial role and their complex coupled interaction needs to be investigated via a TCAD-based approach. For this reason, time-dependent dielectric breakdown measurements at constant-current stresses and voltage-ramp stresses up to breakdown have been performed on thick metal-insulator-metal structures, and numerical simulations have been carried out so to predict the failure mechanisms. To this purpose, special attention has been devoted to the physical modeling of defects and impact-ionization generation.**

***Index Terms*—Silicon oxide; Insulators; Reliability; TEOS**

I. Introduction

Metal-insulator-metal (MIM) capacitors embedded in the back-end inter-level dielectric layers have been recently proposed for analog and RF applications [1]–[3]. Silicon dioxide (SiO_2) is the main insulator in the electronic industry because of its near-ideal properties; however, the degradation and failure of MIM devices is still limited by charge buildup in pre-existing defect sites of the oxide layer. Among the specific issues, such capacitors are thick structures in the micrometer range. They are obtained through several deposition steps in order to sustain high electric fields [4].

The tetraethyl orthosilicate (TEOS) is usually adopted as a precursor for the interlayer thick oxides in the plasma-enhanced chemical vapor deposition (PE-CVD). Such technique allows to deposit thick SiO_2 films in the back-end with good physical properties, but they are known to show a much larger density of preexisting defects with respect to the thermally grown SiO_2 on top of silicon bulks. The latter characteristic leads to higher leakage currents while, when compared to thermally-grown oxides on silicon [5], [6], the internal electric fields can be significantly modified by charge build-up, further limiting the expected device performance and reliability [7]. In addition to this, the final application as galvanic insulators implies that very high electric fields are applied. Due to the high electric fields, carriers can gain sufficient kinetic energy to generate electron-hole pairs, i.e., to give rise to non-negligible impact-ionization generation, which needs be taken into account in order to have a complete description of the main physical mechanisms responsible of the breakdown of such devices. For these reasons, a TCAD-based model capable of correctly handling charge transport, trapping and de-trapping mechanisms and avalanche onset in such kind of bulk oxides can be a useful tool for the development and optimization of galvanic insulators in integrated high-voltage systems. Thick back-end MIM structures have been characterized under constant-current, and voltage-ramp stresses with voltage ramps in DC and AC conditions up to breakdown and the main transport features concerning charge injection, traps and avalanche generation have been modeled in a consistent TCAD setup.

II. Test structures and experiments

Fig. 1 shows a cross section of the high-voltage MIM capacitor used in this work. The electrodes are in tantalum nitride (TaN). The bottom metal is deposited on silicon and is grounded, while the high voltage is applied to the circular top metal (diameter $d \approx 150\ \mu$m). The TEOS material is used as intermetal dielectric. The parallel plate capacitor has a nominal thickness $t_{\mathrm{OX}} = 0.9\ \mu$m. No relevant issues concerning with device variability were observed, thus the characteristics of single samples are used as reference for the analyzed curves.

Constant current stresses have been applied to the MIM under study at different temperatures until the breakdown condition was reached measuring the voltage at the top contact.

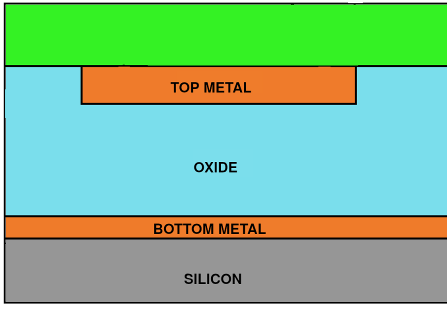

Fig. 1. Schematic view of the TEOS capacitor.

For each temperature, three targets of current density have been used as reported in Table I.

Forcing current directly through the capacitor leads to very long voltage rise-times, as $dV/dt = I/C$, with I the current flowing through the insulator which is very low, C the capacity of the MIM and V the applied bias. To avoid this issue, the following approach is used: at $t = 0$, a constant voltage is applied to the capacitor, the current is measured and considered as the target current level. In order to avoid current reduction due to charge trapping, a small voltage ramp is applied at fixed time intervals of 10s. The new voltage required to force the target current is thus found and set.

Fig. 2 shows the applied electric field calculated as $F_{\mathrm{OX}} = |V|/t_{\mathrm{OX}}$, with V the voltage applied at the top electrode, as a function of the stress time for each current stress and temperature under study.

Table I. Temperature conditions and current targets used in experiments.

	$T = 25$ °C	$T = 150$ °C
J_1 (A/cm^2)	$1.4 \cdot 10^{-8}$	$1.6 \cdot 10^{-8}$
J_2 (A/cm^2)	$3.0 \cdot 10^{-8}$	$3.6 \cdot 10^{-8}$
J_3 (A/cm^2)	$6.3 \cdot 10^{-8}$	$7.5 \cdot 10^{-8}$

The application of a constant current stress substantially allows to keep constant the flux of carriers injected into the oxide during time. The oxide-field increase is an indication of the charge trapping in the oxide. The voltage increase stops when an electric field of about 9 MV/cm is reached, and saturates for longer stress times as shown in Fig. 2. The voltage saturation is a clear indication of the onset of avalanche condition leading to breakdown. It should be noted that the blocking field is almost independent of the current forced in the device and temperature with a value of $F_{\mathrm{OX}}^{\mathrm{BD}} \approx 9$ MV/cm.

In order to gain further insight on the trapping effects and the physical mechanisms involved in the breakdown of such devices, voltage-ramp measurements have been carried out under AC and DC stress conditions. The DC stress was performed by applying a voltage ramp at a constant rate of 6 V/s to the sample until the breakdown condition was reached. The bipolar AC square-wave voltage was applied with pulses of increasing amplitude and a period of 0.82 s up to the

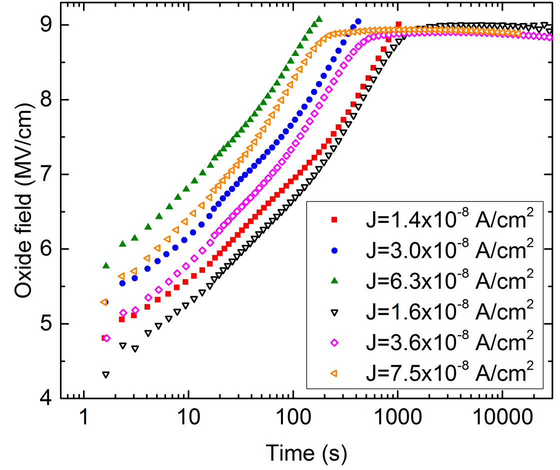

Fig. 2. Constant current measurements performed on the SiO_2 TEOS thick capacitor. Two temperature conditions have been tested, namely $T = 25$ °C (close symbols) and $T = 150$ °C (open symbols).

breakdown. Both cases are depicted in detail in Fig 3. The voltage ramp rate has an impact on the filling probability of the traps due to the trapping time constants, which are proportional to the capture cross-sections [8]. More specifically, a short time sweeping can avoid or minimize trapping of carriers, leading to a larger injection current. In order to fairly compare the outcomes of the different stress conditions, the AC stress was carried out with the same voltage ramp rate of the DC one, namely 6 V/s, which was shown to be slow enough to lead to a significant charge trapping [9]. Moreover, in order to reduce undesired displacement current effects, after each positive or negative ramp, the voltage was kept constant to $V = 0$ for 0.2 s, as shown in Fig. 3, bottom.

Fig. 4 shows the current density as a function of the applied electric field for the AC and DC voltage-ramp stresses. Concerning the AC measurement, the plotted data have been extracted at the center of the time interval at the voltage peak for each period, so that the greatest current recorded for each period is reported. The two characteristics show a similar trend. The first part of the characteristics at low fields, up to about $F_{\mathrm{OX}} = 6$ MV/cm, shows a relevant increase of the current due to charge injection at contacts. The current saturation observed at $F_{\mathrm{OX}} > 6$ MV/cm is a clear indication that charge trapping is the predominant physical effect in this region, as the injected charges are trapped in oxide defect sites and cannot contribute to the current, while the electric field at the contact is reduced limiting the charge tunneling. The current is greater in the case of an AC stress because the polarity change allows for de-trapping at the anode contact thus maintaining the electric field higher at the injecting electrode with respect to the DC stress allowing for a larger charge tunneling. At higher fields (greater than 8 MV/cm) traps become filled and the current starts increasing again up to the

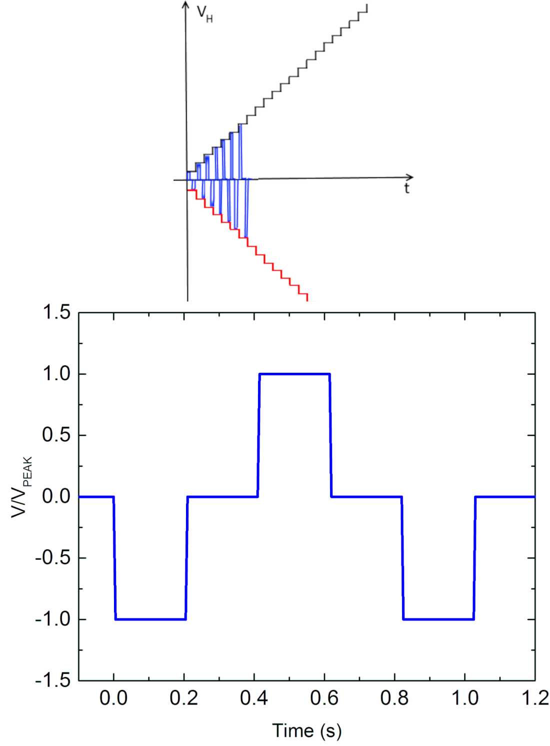

Fig. 3. Top: AC square wave signal applied to the MIM under study. Negative and positive ramps are highlighted.
Bottom: Magnification of the applied signal. The applied voltage to the peak voltage ratio is plotted as a function of time. The period is $T = 0.82$ s.

breakdown, with a slight anticipation in the AC regime: the AC breakdown field is $F_{\rm AC}^{\rm BD} = 8.6$ MV/cm, while the DC one is $F_{\rm DC}^{\rm BD} = 9.1$ MV/cm. Impact ionization should play a relevant role in this portion of the characteristics.

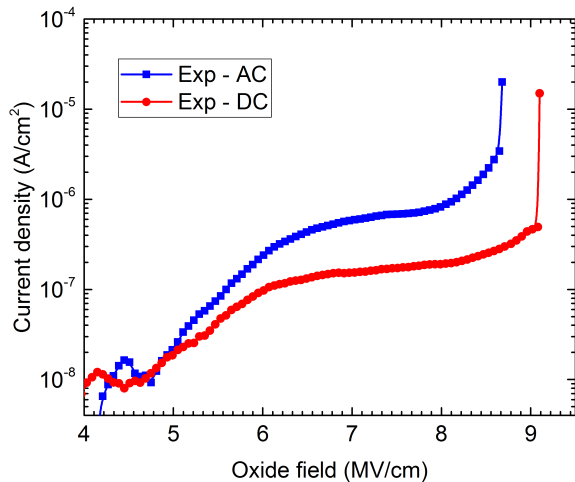

Fig. 4. Current density as a function of the applied electric field for the AC and DC stresses.

III. TCAD MODELING OF THE SiO_2

The conduction model of the TEOS SiO_2 can be described by using a drift-diffusion (DD) transport model with suitable physical parameters, such as the energy-band structure, the presence of distributed defects in the material band-gap, the impact-ionization generation and the tunneling injection at the contacts [9]–[11].

As far as the defects are concerned, we mostly based pur modeling approach on previous works dealing with thermally-grown SiO_2. The experimental data on TEOS oxide structures clearly show the need of a set of two traps with different energy levels. Trapping and de-trapping mechanisms have been taken into account by using a first-order detailed balance equation for each trap as available in the TCAD tool [12]; the trap equations are solved consistently along with Poisson and electron and hole transport equations. The trapped charge is explicitly accounted for in the Poisson equation. This approach requires to define each type of defects by fixing the energy dependence, the concentration and the capture cross-section. Any field-enhanced effect on the capture and emission rates has been assumed to be modeled in the capture cross-section of each trap.

We have defined only acceptor-type traps for electrons, i.e., defects that are neutral when empty and carry a negative charge when occupied by an electron. A uniform spatial distribution is assumed for all traps. Concerning the energy level of the traps, it should be pointed out that, being SiO_2 an amorphous material, energy bands of traps arise instead of discrete trap levels. For this reason, we have defined two uniform distributions of traps in bands of 0.5 eV width with mean energies $E_1 = 6.3$ eV and $E_2 = 6.5$ eV, where the oxide valence band has been taken as the reference level. The energy distribution of traps is represented in Fig. 5, showing also the different distribution functions adopted for the bands. No significant sensitivity to the energetic function was observed when comparing simulation results carried out with the uniform distribution and the equivalent Gaussian functions.

The determination of trap cross-sections requires a special attention to transient responses. In the past years, many authors have reported measurements of electron capture cross sections [13]–[17], with values ranging from 10^{-13} cm^2 to 10^{-18} cm^2. We have used two different cross sections of respectively $\sigma_1 = 1.1{\cdot}10^{-15}$ cm^2 and $\sigma_2 = 9{\cdot}10^{-15}$ cm^2, in fair good agreement with the values reported in [18].

The trap parameters are reported in Table II.

As far as the high-field transport is concerned, the effect of avalanche due to impact ionization cannot be neglected in a complete picture of the relevant physical mechanisms [19]. Thus, the impact-ionization generation has been taken into account in our simulation setup using the van Overstraeten-De Man model [20] fitted against the experimental and theoretical data reported in [19]. Fig. 6 shows the calibrated ionization coefficient against experimental data as a function of the electric field. The phonon energy was fixed to 153 meV, consistently

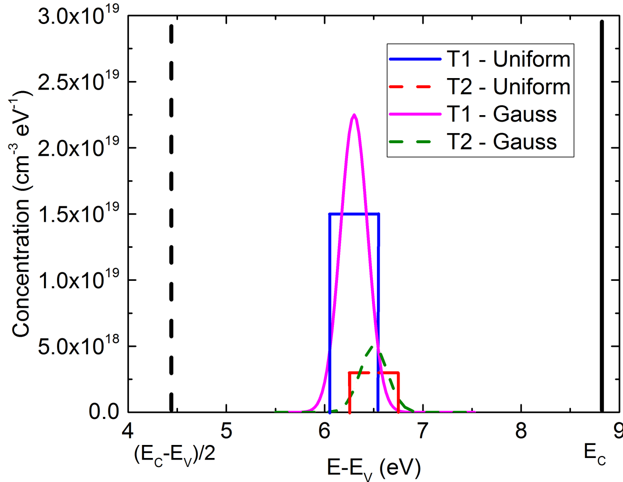

Fig. 5. Energy distribution of traps. Both the uniform distribution adopted and the equivalent densities with Gaussian functions are plotted. The valence band has been taken as the reference level, i.e. $E_{\mathrm{V}} = 0$. The point $(E_{\mathrm{C}} - E_{\mathrm{V}})/2$ represents the mid-band gap. A band-gap $E_G = 8.9$ eV is assumed for SiO_2.

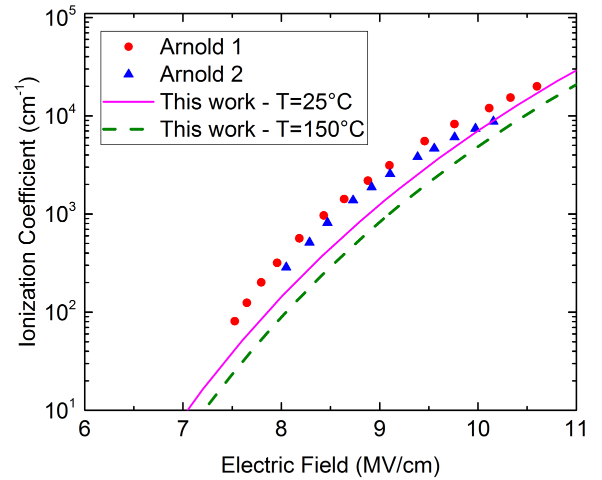

Fig. 6. Electron avalanche coefficient as a function of the electric field. Symbols: experimental data in [19]. Solid line: calibrated TCAD model at room temperature. Dashed line: calibrated TCAD model at $T = 150$°C.

Table II. Trap parameters used for the two trap distributions. Mean energy of the trap level, trap width, electron capture cross section and trap density are reported for each type of traps. The parameter E_{T} is referred to the top of the valence band, taken as the reference level.

Parameter	Trap 1	Trap 2
E_{T} (eV)	6.3	6.5
ΔE (eV)	0.5	0.5
σ_e (cm^2)	$1.1 \cdot 10^{-15}$	$9 \cdot 10^{-15}$
N_{T} (cm^{-3})	$7.5 \cdot 10^{18}$	$1.5 \cdot 10^{18}$

with the indications in [19] showing a limited temperature dependence of the electron impact-ionization coefficient.

IV. Simulation results

The TCAD setup described in the previous Section has been applied to reproduce the experimental data of the constant-current and the AC and DC stresses. To this purpose, a quasi stationary current ramp has been applied up to the desired current level, and a constant-current stress is directly applied to the simulated device. Fig. 7 shows the TCAD results of the oxide field versus time at $T = 25$ and 150 °C. Experiments are qualitatively reproduced, indicating that the rate at which charge is trapped is in agreement with the experimental data, predicting $E_{\mathrm{OX}}^{\mathrm{BD}}$ and the corresponding time to breakdown.

In order to gain insight on the internal phenomena producing the observed breakdown, the electric field distribution across the device is plotted at $T = 25$ °C, $J = 6.3 \cdot 10^{-8}$ A/cm^2 for three stress times, namely $t_1 = 1$s (at the beginning of the stress), $t_2 = 100$s (during the voltage increase) and $t_3 = 1000$s (after the breakdown condition is reached), as shown in Fig. 8. Charge injection from the top electrode ($x = 0$) leads to a charge trapping dynamics and a clear increase of the internal field towards the bottom contact. The maximum field reached

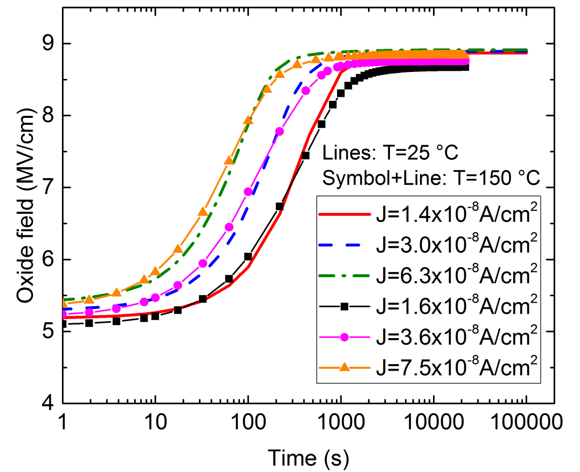

Fig. 7. Simulations of the oxide field plotted as a function of time at different temperatures, namely $T = 25$ °C (lines) and $T = 150$ °C (lines+symbols).

near the bottom electrode at the longest time is as large as 10.5 MV/cm, comparable with the breakdown strength of bulk SiO_2 [19].

In order to further assess the role of trapping mechanisms in the observed constant-current TDDB dynamics, the trapped charge across the device has been extracted from simulations at $T = 25$ °C, $J = 6.3 \cdot 10^{-8}$ A/cm^2 at $t_1 = 1$, 100 and 1000 s, as shown in Fig. 9. It can be noted that at short stress times the trapped charge distribution is substantially flat across the device and simply tends to increase uniformly. Differently, at $t = 1000$ s the trapped charge is higher near both contacts with respect to the central portion of the device. The trapped charge

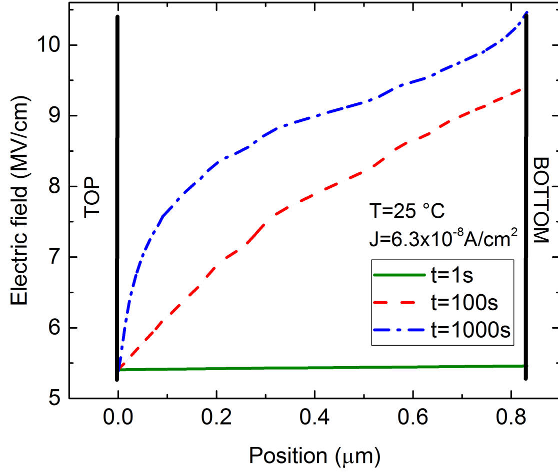

Fig. 8. Electric field distribution across the device at $T = 25$ °C and $J = 6.3 \cdot 10^{-8}$ A/cm^2 for three different stress times.

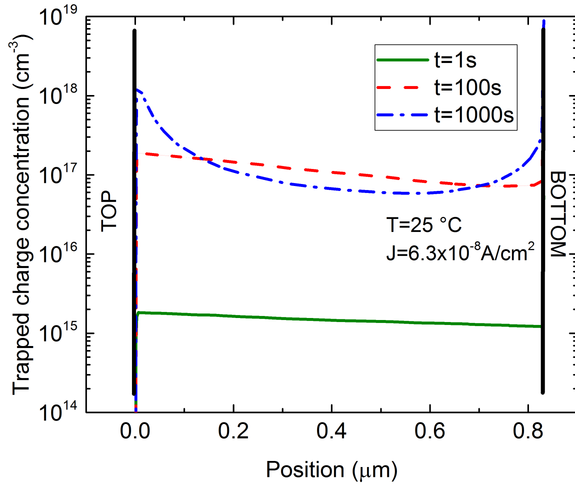

Fig. 9. Total trapped charge across the device at $T = 25$ °C and $J = 6.3 \cdot 10^{-8}$ A/cm^2 for three different stress times.

in the proximity of the top contact is mainly due to electron injection from the cathode: an accumulation of charges trapped in the defects is found in the region where the lowest electric field is observed, while a significant trapped-charge emission is expected to play its role at larger electric fields in the middle of the layer. On the other hand, the enhanced trapping near the bottom contact is an effect of avalanche generation which becomes relevant at long stress times due to the even larger field. In fact, the electrons are generated by impact ionization across the device especially near the anode. Those excess electrons can either be emitted from the bottom contact or be trapped, leading to an enhanced trapping concentration in the proximity of the anode.

This is further confirmed by the avalanche generation rate plotted in Fig. 10, where it can be noted that, for long stress times, the generation of electrons gradually increases moving towards the bottom contact. This means that the largest number of generated electrons is close to the anode.

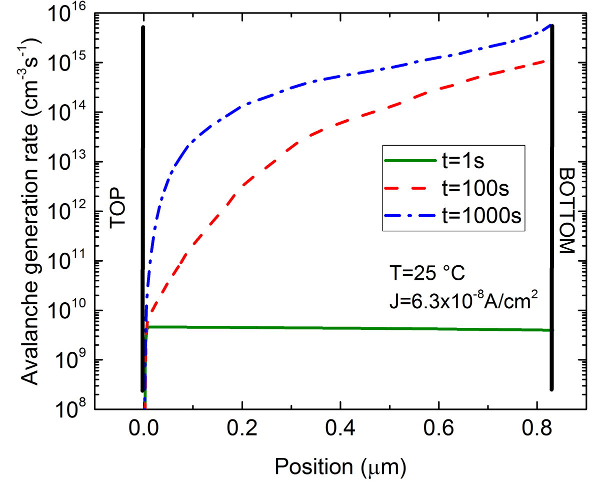

Fig. 10. Avalanche generation rate across the device at $T = 25$ °C and $J = 6.3 \cdot 10^{-8}$ A/cm^2 for three different stress times.

Concerning the AC and DC stresses, a square wave signal and a voltage ramp at a constant rate have been applied to the simulated device. Fig. 11 shows the TCAD results of the current density versus the oxide field for the two stress conditions. The low-electric field ($F_{\mathrm{OX}} < 6$ MV/cm) part of the characteristics is strictly related to the charge injection due to tunneling effect. The difference between simulations and measurements might be ascribed to a perimeter contribution to the total current and trap assisted tunneling effects from the electrodes which are not taken into account in simulations. At intermediate electric fields (up to 8 MV/cm) the current is mainly limited by charge trapping effects. Simulations are in good agreement with experiments, indicating that the relevant charge trapping mechanisms are properly modeled and calibrated. In the high-field regime, namely over 8 MV/cm, the effect of impact ionization can be noted. The slight anticipation of the observed breakdown field in the AC regime with respect to the DC stress condition is nicely captured by simulations.

The total trapped charge and the electric field across the device have been plotted in Fig. 12 and Fig. 13 at two different oxide fields, namely $F_{\mathrm{OX}} = 6$ MV/cm (in the charge-trapping portion of the J-E characteristics) and $F_{\mathrm{OX}} = 8.5$ MV/cm (just before the AC breakdown). The two stress conditions show different behaviors with some common features. In both stresses, even if the great majority of the total charge is already trapped at $F_{\mathrm{OX}} = 6$ MV/cm ($N_T \approx 10^{16}$ cm^{-3}), charge buildup in the oxide continues until the breakdown condition is reached (Fig. 12). However, while the charge distribution in the DC regime is substantially flat at low fields, in the AC regime

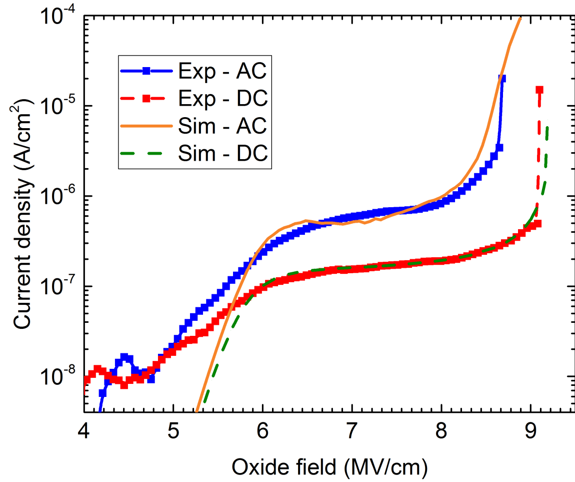

Fig. 11. Current density as a function of the oxide field for the AC and DC voltage ramp stresses. Dots: Experiments. Solid lines: simulations.

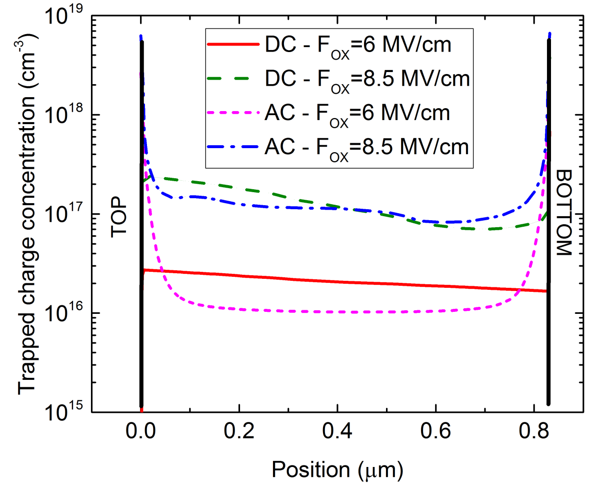

Fig. 12. Trapped charge across the device under AC and DC regimes at two different oxide fields, namely $F_{\mathrm{OX}} = 6$ MV/cm (in the cherge-trapping portion of the J-E characteristics) and $F_{\mathrm{OX}} = 8.5$ MV/cm (just before the AC breakdown).

more charge is accumulated near both contacts, as expected, because charge is injected from both of them alternately. At high fields, the distribution in the DC case shows more trapped charge near the top contact as it is the injecting electrode, while for the AC regime the distribution is similar to the low-field case with the trapped charge being greater near the two contacts with respect to the DC case.

Concerning the electric-field distribution (Fig. 13), at low biases a nearly flat distribution for both the AC and DC regimes is observed, while at greater biases the trapped charge causes a modification of the local electric field, and a greater field is observed in the AC regime with respect to the DC one especially near the contacts explaining why the AC breakdown is slightly anticipated.

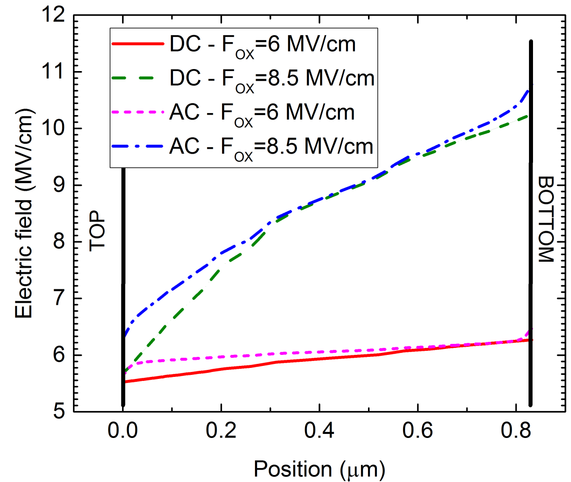

Fig. 13. Electric field distribution across the device under AC and DC regimes at two different oxide fields, namely $F_{\mathrm{OX}} = 6$ MV/cm (in the cherge-trapping portion of the J-E characteristics) and $F_{\mathrm{OX}} = 8.5$ MV/cm (just before the AC breakdown).

V. Conclusions

A TCAD model has been presented to investigate conduction mechanisms in high-voltage silicon oxide thick TEOS capacitors embedded in the back-end inter-level dielectric layers. The TCAD has been proven to be a useful tool for the study of transport in TEOS oxides, as they tend to show different electrical properties with respect to thermally grown SiO_2. The role of traps has been extensively investigated. Different stress conditions, such as constant-current time dependent dielectric breakdown and AC and DC voltage ramp stresses up to breakdown, have been analyzed in order to investigate the role of the main physical mechanisms involved in the breakdown of such devices. The reported predictions are in nice agreement with experiments up to the breakdown condition. From the comparison of TCAD simulations with experiments, we can conclude that impact-ionization is the most relevant mechanism involved in the breakdown of such devices along with the significant charge trapping in the oxide bulk.

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