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Gate Reliability of p-GaN Power HEMTs Under Pulsed Stress Condition

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***Abstract*—A combined experimental/simulation analysis has been performed to study the gate reliability of GaN-HEMTs with p-type gate under pulse stress conditions. Results show that the time-dependent gate breakdown (TDGB) can be determined by two factors: i) the total ON-time during which the device is subjected to a positive gate bias before the failure; ii) the number of pulses, hence the number of switching phases from OFF- to ON-State and vice versa. The severity of the degradation ascribed to transition phases depends on the OFF-time (t_{OFF}) and transition time ($t_{TR} = t_{RISE} = t_{FALL}$). In particular, the shorter t_{OFF} and t_{TR}, the higher the Schottky junction voltage drop and the current peak during the switching phase, respectively. The higher voltage drop is ascribed to the semi-floating potential of the p-GaN layer.**

***Index Terms*—Gallium Nitride, HEMTs Reliability, p-GaN Gate, Pulsed Gate Stress, TCAD Modeling.**

I. Introduction

To date, GaN-based power high electron mobility transistors (HEMTs) emerged as one of the most suitable technology for high-voltage and high-power applications due to their capability to operate at relatively high frequency with higher efficiency when compared with their Silicon-based counterpart [1]-[4]. Among all the solutions for normally-OFF operation, a Magnesium-doped (p-type) GaN layer placed between a gate metal and an AlGaN barrier layer, results to be one of the best choice from performance, stability and cost point of view [5]-[8].

In a typical switching application, e.g. in a power converter, the gate of such transistors is repeatedly switched, at relatively high frequency, between high (ON-state) and low voltage values (OFF-state). Therefore, reliability analysis under pulsed gate conditions is of paramount importance.

Although, the metal/p-GaN Schottky contact effectively limits the gate leakage [9], the semi-floating p-GaN layer potential can lead to charging/discharging processes inside the metal/p-GaN/AlGaN/GaN epi-stack, causing critical reliability and electrical performance degradation concerns under pulsed conditions.

Many papers reported how fast transient and/or pulsed stress/characterization may induce threshold voltage shifts (ΔV_{TH}) [10]-[16]. In [13], He et al. showed that fast-dynamic forward gate stress induces frequency dependent positive ΔV_{TH}. Such behavior has been attributed to carrier injection/emission in/from the p-GaN layer or the AlGaN barrier layer.

Tang et al. [14] observed positive threshold voltage shift ascribed to trapping of electrons, coming from the 2DEG through the AlGaN barrier, in the p-GaN layer. The latter becomes negatively charged until the electron de-traps after a certain relaxation time under zero bias condition.

In [15], a fully recoverable ΔV_{TH} hysteresis under fast sweeping characterization has been reported. In particular, the sweeping time was found to be crucial for threshold voltage shift, i.e., the longer the sweeping time the higher the positive V_{TH} shift. Recently, in [16] has been proposed an accurate TCAD modeling of such phenomena, attributing the dynamic V_{TH} shift to time dependent charging/discharging processes in the floating p-GaN layer, which are ruled by the balance of both the Schottky diode (metal/p-GaN) and p-i-n diode (p-GaN/AlGaN/GaN) leakage currents.

While the time-dependent gate breakdown (TDGB) under static stress condition has been largely analyzed for this technology [17]-[22], only a few papers about the case of pulsed gate stress were reported in the literature so far.

To the best of our knowledge, only a frequency-dependent gate degradation under pulsed stress, up to 100 kHz, has been studied in [23], reporting a weak frequency dependency of the gate Mean Time-to-Failure (MTTF).

In this paper, the time-dependent gate breakdown under dynamic stress condition has been investigated for higher frequencies (up to 3.3 MHz). More specificly, this work aims

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to investigate which are the AC signal features (e.g. ON-time, OFF-time, rise/fall time, etc.), applied to the gate terminal, causing irreversible failure. Experimental results combined to TCAD simulations highlight reliability aspects which could not be identified by DC stress analysis.

II. Device Under Test and Analysis Details

Devices under test (DUTs) are p-GaN gate HEMTs grown by metalorganic chemical vapor deposition (MOCVD) on a 200-mm GaN-on-Si substrate by imec. The epi-stack consists of a 200-nm AlN nucleation layer, a 1.65-μm (Al) GaN superlattice layer, a 1-μm C-doped GaN back barrier, a 200-nm undoped GaN channel layer, a 16-nm thick AlGaN barrier with 23.5% Aluminum (Al) content, and a 70-nm Mg-doped p-GaN layer with a dopant concentration of 3×10^{-19} cm^{-3}. For additional process details see [8].

The considered structures, realized for gate reliability studies, feature equal gate-to-source and gate-to-drain distance (L_{GS} = L_{GD}) of 1.25 µm. The gate width (W_G) and length (L_G) are 10 µm and 0.5 µm, respectively.

The time-dependent gate breakdown analyses under pulsed stress condition have been carried out by applying consecutive square-wave at the gate contact by means of a Pulse Wave Generator (PWG), while the source and drain contacts are both forced to 0 V through a Source Measure Unit (SMU), as shown in the schematic reported in Fig. 1. The SMU monitors the leakage current (Gate Current) in order to indirectly detect the gate breakdown. Furthermore, an oscilloscope has been connected, together with the PWG, at the gate contact to monitor the applied signals during the tests. Thanks to appropriate 50 Ohm impedance matching and control of parasitics, the measured waveforms do not show any significant voltage overshoot/spike in the considered frequency ranges.

The Time to Failure (TTF) is defined as the time at which the current abruptly increases over a certain value (1 mA in this work). The experimental results are analyzed in terms of: a) mean time-to-failure (MTTF) extrapolated with an arithmetic average on the time-to-breakdown of 7-15 devices; b) mean number of pulses necessary to reach the breakdown, defined as: Mean N° of Pulses = MTTF/Period; c) mean Total ON-Time, i.e. the total time in which the device is in ON-State before the breakdown (Mean N° of Pulses*T_{ON}).

To sense the current peaks at the transition phases, an additional experimental setup has been employed. As before, a square waveform is applied at the gate contact while the drain and the source contacts are shorted. Here, the current flows through a shunt/sensing resistor and the voltage drop across it is monitored by means of a high-resolution oscilloscope (see Fig. 2).

For the scope of this work, the applied square-waves at the gate terminal feature different ON-Time (t_{ON}), OFF-time (t_{OFF}) and rise/fall time (or transition time t_{TR}), while the amplitude (V_G) is 9.4 V and 8V for the TTF and current

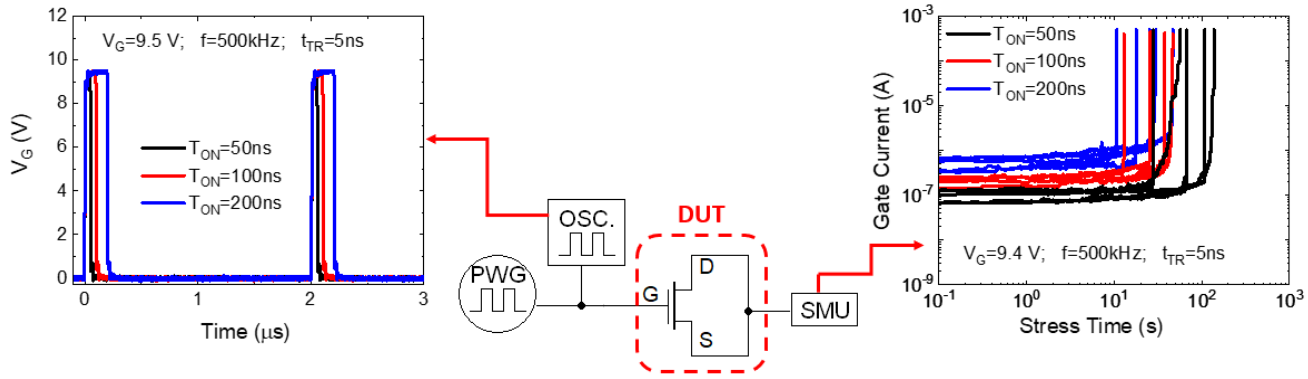

Fig. 1. Schematic of the experimental setup for time-dependent gate breakdown pulsed analysis.

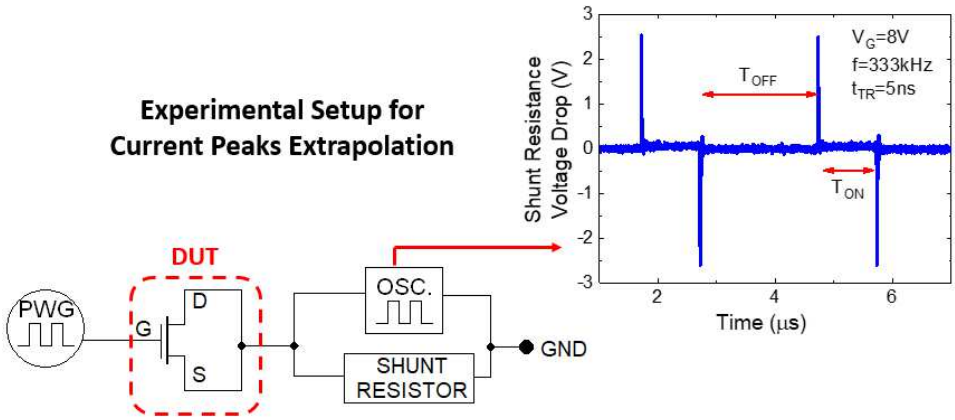

Fig. 2. Schematic of the experimental setup for current peaks extrapolation at the transition phases.

peaks extrapolation, respectively. The temperature is fixed at 150° C for all the experiments.

The experimental results are supported by TCAD simulations. In the case of HEMTs with p-type gate, the modeling of the gate leakage is of paramount importance, playing an important role on the devices' threshold voltage [24]. Specifically, the balancing between the metal/p-GaN Schottky junction and p-GaN/AlGaN/GaN (p-i-n) junction leakage components determines the charging state of the semi-floating p-GaN layer. As a matter of fact, nonlocal tunneling models [25] in combination with thermionic emission contributions have been adopted and defined for both junctions. Hole tunneling, reproducing the hole injection from the metal to p-GaN valence band, has been activated and calibrated at the Schottky gate contact, whereas nonlocal trap assisted tunneling (TAT) has been used to model the leakage current through the AlGaN barrier. Such TAT is allowed for both electrons and holes coming from 2DEG (two-dimensional electron gas) and 2DHG (two-dimensional hole gas), respectively, and includes both inelastic phonon-assisted and elastic processes. More details about the adopted models and calibration can be found in [16].

III. Results and Discussion

Fig. 3(a) shows the mean time-to-failure as a function of t_{ON} for two fixed t_{OFF} values, 250 ns and 5 µs. In the first case, the MTTF increases with t_{ON}, whereas an opposite trend is observed with t_{OFF} = 5 µs. For a better understanding, the mean Total ON-Time is compared with the DC case in Fig. 3(b). DC condition represents the mean time-to-failure extrapolated by typical Constant Voltage Stress (CVS) tests at 9.4 V, i.e. the same value of the square-wave amplitude used for pulsed stress test.

From Fig. 3(b) emerges that, in the case of t_{OFF} = 250 ns, for $t_{ON} \leq 2$ µs the mean total ON-time is shorter than the DC case. On the other hand, for $t_{ON} > 2$ µs, as well as for longer t_{OFF} (5 µs), the mean total ON-time features values close to that one extrapolated by CVS tests. From these preliminary results, it can be hypothesized that dynamic gate stress, hence the transition phases, introduces degradation effects in addition to the total time during which the applied gate voltage is at the higher value. This is supported by Fig. 3(c), showing that for relatively short ON- and OFF-time (< 1 µs and 250 ns, respectively), the mean N° of pulses is roughly constant independently of t_{ON}, suggesting that the number of transition phases is determining the TDGB. On the contrary, by further increasing t_{ON} (> 2 µs), the degradation ascribed to Total ON-Time starts to be dominant, leading to a gate TTF with a reduced N° of pulses. As a result, the degradation induced by the transition phase is reduced as well, giving rise to a Total ON-Time to failure equal to DC-MTTF (Fig. 3b). Same behavior is observed with a t_{OFF} = 5 µs, suggesting that a longer t_{OFF} is weakening the degrading effect of the transition phase, in fact, once again, the Total ON-time to failure equals the DC case (Fig. 3b).

In order to understand which factors impact the transition phase degradation effect, dynamic time-dependent gate breakdown tests with different OFF-time (ranging from 100 ns to 20 µs) and transition time (5 ns, 20 ns and 80 ns) have been performed at fixed t_{ON} =1 µs.

Fig. 4(a) shows that the mean Total ON-time depends on both t_{OFF} and t_{TR}. In particular, the shorter t_{TR}, the shorter the mean Total ON-Time to failure. To explain such trend, the current has been monitored with experimental setup described in the previous section (Fig. 2), by varying the transition time (from 5 ns to 80 ns) and by fixing t_{ON} = 1 µs, t_{OFF} = 250 ns and V_G = 8 V. Fig. 5(a) shows that the current peaks occurring during the rising and falling phases are strongly impacted by the transition time. In particular, the shorter the transition time, the higher and tighter the current peaks at

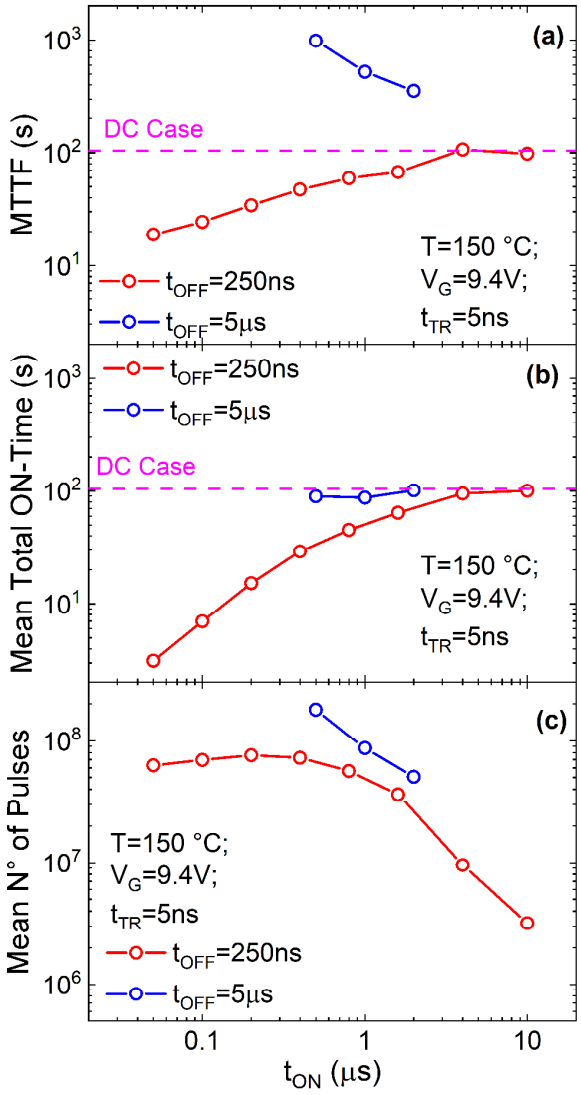

Fig. 3. ON-Time dependency of the Mean Time-to-Failure (a), Mean Total ON-Time to Failure (b) and Mean Number of Pulses (c) with two fixed OFF time, i.e., 250 ns (red) and 5 µs (blue). Results of time-dependent gate breakdown tests with V_G = 9.4 V, T = 150 °C and t_{TR} = 5 ns. Each experimental data point is the average over 7-15 devices.

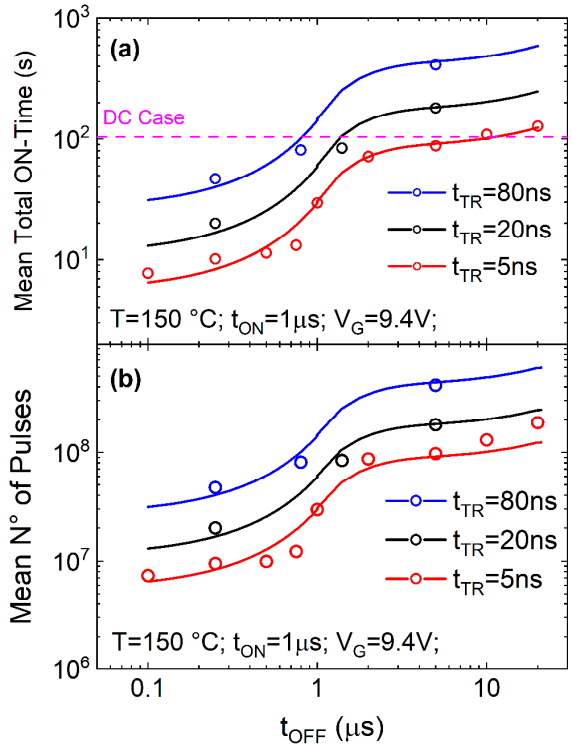

Fig. 4. OFF-Time dependency of the Mean Total ON-Time (a) and Mean Number of Pulses (b) with fixed ON-time (1 µs). Results of time dependent gate breakdown tests with V_G = 9.4 V, T = 150 °C and three different t_{TR} (5 ns, 20 ns and 80 ns). Each experimental data point is the average over 7-15 devices.

both rise and fall switching phases. As a result, the faster is the transition phase the stronger is the degradation effect induced by the current spikes, possibly responsible of the gate time-to-failure reduction. A good agreement has been found with the TCAD-simulated gate current (Fig. 5b), reproducing the same t_{TR} dependency and confirming that the current overshoots are not introduced by the stray inductance of the test circuit but by the gate stack structure itself.

In addition to t_{TR} dependency, results show that the degradation effect associated to the transition phase is effectively reduced also increasing t_{OFF}. This is confirmed by Fig. 4(b), showing that the N° of pulses that the device can handle before the gate breakdown increases with both t_{OFF} and t_{TR}.

Moreover, it is worth noting that for longer t_{TR} and t_{OFF}, the mean Total ON-time is longer than DC-MTTF (Fig. 4(a)). This might be possible if the defects produced during the ON-time are partially recovered during the OFF-time, assuming the degradation due to switching phases is negligible thanks to long t_{TR} (relatively low leakage current peak). From percolation theory [26]-[28], when a relatively high electric field is applied to a defective region, new defects/traps are created in addition to pre-existent ones. Once a critical number of defects forms in a specific location, a percolation path, inducing layer/device breakdown, is created. Such processes are time dependent. Unlike DC case, under pulsed stress condition the time necessary to reach the failure (i.e.,

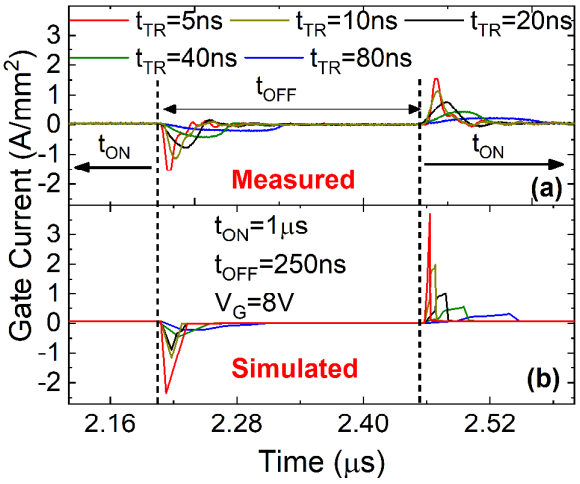

Fig. 5. Measured (a) and simulated (b) gate current with t_{ON} = 1 µs and t_{OFF} = 250 ns and different transition times.

the creation of enough new defects) might be longer since the stress time is interrupted (OFF-time); this relaxation period possibly induces a partial recovery of the failure processes.

The t_{OFF} dependency cannot be explained by the current peak during the switching phase since, as confirmed by experiments and TCAD simulations, it does not change by varying the OFF-time (Fig. 6), even if the gate reliability is strongly influenced by t_{OFF} as shown in Fig. 4.

Thanks to TCAD simulations, the electrostatic potential has been monitored by varying t_{OFF} in the middle of the semi-floating p-GaN layer (at 40 nm away from gate metal and pGaN/AlGaN interface), in a region where the carrier density is constant since it is far away from the Schottky depletion region and the 2DHG layer (Fig. 7a). In Fig. 7 (b), it can be observed that after the transition from ON- to OFF-state (fall time) the p-GaN potential is at the same level whatever the t_{OFF} is. During the OFF-state phase (i.e. V_G = 0 V) such potential changes/recovers and then, when the device turn-on

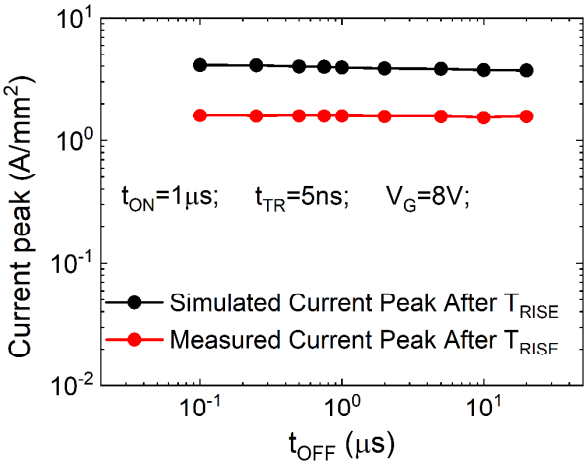

Fig. 6. OFF-Time dependency of the measured (red) and simulated (black) current peak at the switching phase.

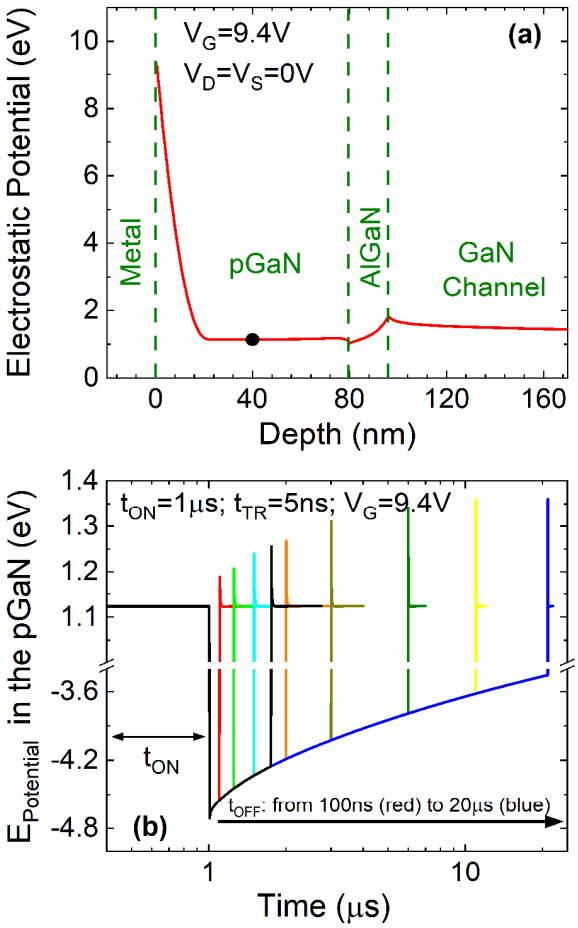

Fig. 7. Simulated electrostatic potential along the device at V_G = 9.4 V and V_S = V_D = 0 V (a). TCAD simulation of the electrostatic potential monitored in the semi-floating p-GaN layer with different OFF-Time (b).

occurs, it shows a peak after the rise time. Such phenomenon is ruled by the recovery time, i.e. the longer the OFF-time the higher the height of the potential peak, inducing a lower Schottky junction voltage drop, hence a lower electric field across the Schottky depletion region (see Fig. 8). This explains the reason why a longer t_{OFF} leads to a longer MTTF.

Fig. 8 reports the Electrostatic Potential peaks after the rise time and the correspondent Electric Field across the Schottky depletion region. It is worth noticing that the observed dependency on the t_{OFF} is similar to the one shown in the case of mean Total ON-time and mean N° of pulses (Fig. 4).

IV. Conclusion

An in-depth analysis of TDGB of p-GaN HEMTs under pulsed stress condition at 150 ° C has been proposed. The gate time-to-failure has been investigated by means of applied consecutive square-waves, featuring different ON-time, OFF-time and rise/fall time, supported by transient current sensing and TCAD simulations.

Two main factors determine the time-dependent gate breakdown of GaN-HEMTs with p-type gate under pulsed

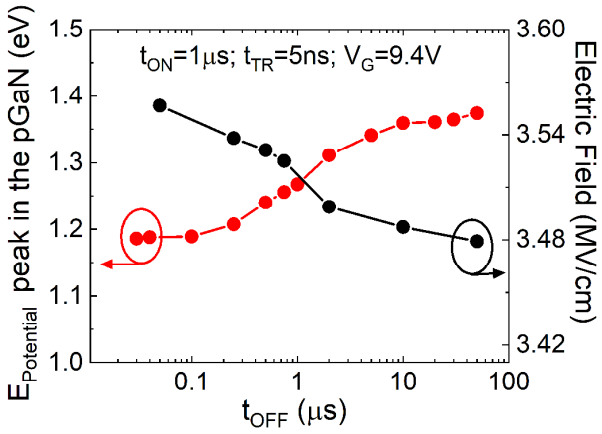

Fig. 8. OFF-Time dependency of the Electrostatic potential peaks at the transition from OFF- to ON-State (just after t_{RISE}) and corresponding mean electric field evaluated across the depletion region of the Schottky junction.

stress conditions: the switching phase (number of applied pulses) and the time in which the device is kept in ON-State, plus a possible recovery mechanism occurring during the t_{OFF}.

The amount of degradation coming from the switching phase depends on both t_{OFF} and t_{TR}. The latter is responsible of altering the amplitude of the current peak during the switching phase. The longer the t_{TR}, the lower the amplitude of such current spikes, the longer the TTF. A good agreement between simulations and experiments has been found.

The OFF-time dependency is ascribed to electrostatic potential in the semi-floating p-GaN layer at the switching phase (from OFF to ON). From TCAD simulations, it emerged that the potential peak increases with the OFF-time leading to a lower voltage drop, hence electric field, on the Schottky depletion region. The simulated p-GaN potential and the Mean Total ON-Time show similar trends with t_{OFF}.

In conclusion, it can be stated that a too short t_{TR} and t_{OFF} gives rise to a shorter time-dependent gate breakdown compared to DC stress condition.

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