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Early Detection of Photovoltaic System Inverter Faults

Martin Omaña, Marco Grossi, Cecilia Metra

Corresponding author: martin.omana@unibo.it , Tel. 0039-0512093038

Department of Electrical Energy and Information Engineering "Guglielmo Marconi" (DEI), University of Bologna, Bologna, Italy

Abstract

Photovoltaic (PV) systems are increasingly adopted as a source of green energy. The reliability of PV systems mainly depends on the reliability of the power MOSFETs of their inverter(s). It has been shown that short and open faults are the most frequent power MOSFET faults. They may compromise the inverter reliability, with consequent significant impact on the PV system energy efficiency. It has been proven that the likelihood of such faults is related to the value of the MOSFET ON-state resistance, which may increase over time due to aging mechanisms. When the value of such a resistance reaches a critical value, the likelihood of the MOSFETs subsequently failing as open or short becomes very high. In this paper, we first evaluate the effects of the MOSFETs' ON-state resistance increase on the harmonic components of the inverter input and output currents. Then, based on the obtained results, we propose an innovative strategy for the early detection (also referred to as condition monitoring [1]) of inverter faults, which enables to generate an alarm message when the ON-state resistance of any inverter MOSFET reaches the critical value. Upon the generation of such an alarm message, proper recovery strategies can be activated, to enable the online replacement of the affected transistors before they actually become faulty. Our detection strategy does not require to interrupt the inverter normal operation in the field and can be implemented using the microcontroller typically embedded within the control circuitry of PV systems.

Keywords: photovoltaic system, aging, reliability, inverter, MOSFET.

1. Introduction

Photovoltaic (PV) systems are increasingly adopted as a source of green energy [2, 3], since their energy conversion efficiency is higher than that of alternate sources of green energy [4, 5]. As a consequence of the high economic investment required for the installation of PV systems, their reliability is becoming of great concern [6, 7].

A typical PV system consists of the following parts: 1) solar modules, that harvest the sunlight and transform it into a continuous DC voltage [8]; 2) an energy harvesting management module, that monitors the available solar energy and tries to maximize the extracted energy by means of maximum power point tracking (MPPT) methods [9, 10]; 3) an energy storage element (*e.g.,* a battery, supercapacitor, etc.) where the extracted electrical energy is stored [11, 12]; 4) a DC/AC converter, or inverter, that generates an alternate (AC) voltage, that is delivered to the load [13, 14].

The reliability of a PV system depends on the reliability of the different modules that compose it. Among them, solar modules have demonstrated high reliability, with a lifetime of approximately 20 years that, consequently, covers the economic lifetime of a typical PV system.

Instead, it has been shown that, under certain operating conditions, the Mean Time Between Failures (MTBF) of inverters can be as low as 2.25 years [15]. Moreover, in [16, 17] it has been indicated that the failure rate of power MOSFETs is considerably higher than that of any other component of the inverter and PV array [6, 18-20]. Additionally, in [6, 19] it has been shown that faults affecting the inverter MOSFETs may have catastrophic effects on the power delivered to the load, with reductions up to 80%.

In order to cope with this problem, some approaches have been proposed to detect faults affecting PV inverters [6, 19, 20]. However, they enable the detection of faults only after their occurrence, when the efficiency of the PV system has already been severely reduced.

In addition, in [22-27] it has been shown that the increase in the ON-state resistance of power MOSFETs is a failure precursor. In particular, in [27] it has been proven that, during system operation, the MOSFET ON-state resistance increases over time due to aging mechanisms, and that when such a resistance reaches a critical value (approximately a 5% increase of the initial value), the likelihood that the MOSFET will subsequently fail as open or short becomes very high.

In this context, recently, in [21] a circuit to measure the degradation of the conductance of inverter transistors (based on the MOSFET V_{DS} measurement) has been proposed. An analog signal proportional to the performed measurement is generated, that enables to detect the presence of degraded transitors. However, such an approach does not enable to identify which inverter's transistors are degraded, thus requiring to replace the whole inverter, rather than single transistors, to recover from the measured transistors' degradation.

Based on these considerations, in this paper, we first analyze the effects of the increase in the ON-state resistance of inverters' MOSFETs on the harmonic components of the inverter's input and output currents. We will show that the increase in the MOSFET ON-state resistance can be easily related to the change in the harmonic components of the inverter's input/output currents. In particular, we will show that the 50Hz (100Hz) harmonic of the inverter input (output) current presents an approximately linear increase with the increase in the ON-state resistance of the MOSFETs. Our analysis enables to identify the values of the harmonics of the inverter's input/output currents that correspond to the critical value of the MOSFET ON-state resistance.

We then propose an innovative approach for the early detection (also referred to as condition monitoring [1]) of faults affecting inverter's power MOSFETs. It is based on the innovative idea to monitor periodically the variation in the harmonics of the inverter's input/output currents, and generate an alarm message when such harmonics become equal to those that we have found corresponding to the critical value of the MOSFET ON-state resistance. The alarm message can be exploited at system level to activate a proper recovery strategy to replace the affected transistors before they actually become faulty. Our early detection strategy can be for instance easily implemented by using the microcontroller that is typically embedded within the control circuitry of PV systems. Our strategy is robust with respect to high levels of noise on the monitored signals, and variations of the power delivered to the load by the inverter. Moreover, our strategy does not require to interrupt the inverter normal operation in the field, thus not affecting the power efficiency of the PV system.

The paper is organized as follows. In Section 2, we present the inverter considered here as a realistic example. In Section 3, we describe the performed analyses and the achieved results. In Section 4, we describe our proposed early detection scheme and we discuss its costs. Finally, in Section 5, we draw some conclusive remarks.

2. Considered case study inverter

As a realistic case study, we here consider the inverter represented in Fig. 1 [6, 15, 18, 28, 29]. It converts the DC voltage (V_{CC}) generated by the solar modules into an AC voltage suitable to be delivered to the grid. It is worth noticing that in our analyses we realistically considered V_{CC} as a constant voltage, since it is provided by a battery that is usually placed within the PV system, at the output of the MPPT. As represented in Fig. 1, the considered inverter consists of an H-bridge block and an Inverter Control Circuitry [28]. The H-bridge block consists of four n-channel power MOSFETs (M1-M4), and four external power diodes (D1-D4). These diodes are connected in parallel to the MOSFETs, in order to avoid the generation of high voltage glitches, that could damage the MOSFETs. As a realistic example, we have considered the STMicroelectronics STP8NM60 transistors [30] to implement the four MOSFETs (M1-M4). They feature an ON-state resistance (R_{ON}) of 0.9Ω, and a maximum drain-source voltage of 650V. As for the diodes (D1-D4), we have considered diodes of the kind in [31], with V_{ON}=0.7V and breakdown voltage of 600V. It is worth noticing that, even though the considered MOSFETs already include integral antiparallel diodes, we have included external diodes D1-D4, in order to make our analysis more general. In fact, many inverters include external diodes, despite the presence of MOSFETs' integral diodes. This because the switching speed of the MOSFET integral diode is generally slow and may induce excessive power losses, limiting the inverter operating frequency and efficiency. However, we have verified that the results reported in the paper do not change if the external diodes are not employed.

For our analysis we have assumed V_{CC}=10V, which corresponds to the voltage generated by a single PV module [20]. In addition, we have considered a realistic inverter load, consisting of the series of: 1) an inductor L_T, that emulates the inductance of the transformer that is usually connected to the output of PV inverters [28, 29], to convert the inverter output voltage into the power grid voltage; 2) a resistive load (R_L), that represents the inverter load [28]. As a realistic example, we have assumed L_T=20mH, and R_L=1Ω. This latter emulates a load receiving a power of 100W, which is the maximum power that typical PV modules can generate [20].

As for the Inverter Control Circuitry, it generates the control signal V_A (V_B) for the couple of transistors M2-M4 (M1-M3). V_A and V_B are complemented periodic square wave signals, with frequency f_S. We have considered $f_S = 12.5kHz$, that is a value within the range of frequencies that are typically employed for the inverter control signals [28]. The Inverter Control Circuitry block compares an external reference signal V_{ref} (a 50 Hz sinusoidal waveform) with the H-bridge V+ output, and selects the time interval during which M1-M3 and M4-M2 are conductive, so that the 50Hz harmonics of the voltage/current at the H-bridge V+ output follows V_{ref} [6].

3. Analysis of the Effects of MOSFETs' ON-State Resistance Increase

As recalled in the Introduction, in [27] it has been shown that, after an increase in the R_{ON} of the inverter's MOSFETs of 5%, the likelihood that MOSFETs fail as opens or shorts becomes very high. Consequently, a critical value for the MOSFETs' R_{ON} (R_{ON_CRIT}) has been defined in [27] as the R_{ON} value corresponding to a R_{ON} increase (ΔR_{ON}) of 5%.

Based on these previous results, we performed analytical analyses, as well as electrical level simulations, to study how the harmonic components of the inverter's input/output currents change with the R_{ON} increase (ΔR_{ON}). This will allow us to identify threshold values for the harmonics that correspond to R_{ON} becoming uqual to R_{ON_CRIT}. Such threshold values will then be exploited to implement our proposed strategy for the early detection of faults affecting inverter's MOSFETs.

Let us first describe our performed analytical analyses on how the harmonics of the inverter input/output currents change with the increase in the MOSFET R_{ON} (ΔR_{ON}). As dicussed in Section 2, for our analyses we have assumed a sinusoidal wave form for the inverter output current I_{OUT}, with a frequency f=50Hz. Moreover, for simplicity, we have assumed that the four MOSFETs of the inverter in Fig. 1 are ideal switches (with an instantaneous switching time), and that only one of the MOSFETs (M4 in Fig. 1) presents a R_{ON} increase.

Figs. 2(a) and (b) show the schematic representation of the inverter input and output currents (I_{IN} and I_{OUT}, respectively), for the case of a fresh (not aged) inverter. They also report the first harmonics of the Fourier series of I_{IN} and I_{OUT} for the fresh inverter.

As can be seen from Fig. 2(a), the input current I_{IN} of a fresh inverter is a fully rectified sine wave, with a frequency of 100Hz (while the frequency of the non-rectified sine wave was f=50Hz), and an amplitude I_{INp} that depends mainly on the inverter input voltage and load. Therefore, the input current can be expressed by the following equation:

$$I_{IN}(t) = \left|I_{INp} \cdot \sin(2\pi f t)\right| \tag{1}$$

The Fourier series of such a fully rectified sine wave can be expressed by this equation:

$$I_{IN}(t) = I_{INp}\left(\frac{2}{\pi} - \frac{4}{\pi} \sum_{n=2,4,6,\ldots}^{\infty} \frac{cos(2n\pi f t)}{n^2 - 1}\right) \tag{2}$$

The harmonics of I_{IN} of the fresh inverter are also reported in Fig. 2(a), for the case of f= 50Hz. As can be seen, I_{IN} presents a DC harmonic component, and harmonics at multiples of 100Hz (i.e., at 100Hz, 200Hz, 300Hz, etc.) with a decreasing amplitude.

Instead, Fig. 2(b) shows that the output current (I_{OUT}) of a fresh inverter is a sine wave with a frequency f=50Hz, and an amplitude I_{OUTp}, that depends mainly on the inverter input voltage and load. Therefore, the output current can be simply expressed as follows:

$$I_{OUT}(t) = I_{OUTp} \cdot \sin(2\pi f t) \tag{3}$$

Therefore, as reported in Fig. 2(b), the output current I_{OUT} of the fresh inverter presents only an harmonic component at 50Hz.

Now let us study the harmonics of the inverter input/output currents for the case in which the MOSFET M4 (Fig. 1) presents a R_{ON} increase (ΔR_{ON}) due to degradation.

In this case, the ΔR_{ON} of M4 produces an unbalance between the currents flowing through the M1-M3 and the M2-M4 series transistors, resulting in different amplitudes between the positive and negative current semi-cycles of I_{OUT}, and the subsequent semi-cycles of I_{IN}.

This case is schematically represented in Figs. 2(c) and (d) for I_{IN} and I_{OUT}, respectively. As can be seen, in the semi-cycles during which the degraded MOSFET M4 is conductive (i.e., the odd cycles for I_{IN}, and the positive semi-cycles for I_{OUT}), the peak value of I_{IN} (I_{OUT}) is reduced by a certain value ΔI_{IN} (ΔI_{OUT}) that, in turn, depends linearly on the ΔR_{ON} value.

As for the input current, in the degraded inverter, the Fourier series of I_{IN} can be obtained as the superposition of: 1) the Fourier series of I_{IN} in the non-degraded inverter (Eq. 2); 2) the Fourier series of a half-rectified sine wave with an amplitude equal to the current mismatch ΔI_{IN}. The resulting Fourier series of I_{IN} is expressed by Eq (4), and is schematically represented in Fig. 2(c).

$$I_{IN}(t) = I_{INp}\left(\frac{2}{\pi} - \frac{4}{\pi}\sum_{n=2,4,6,\ldots}^{\infty}\frac{cos(2n\pi ft)}{n^2-1}\right)$$

$$- \Delta I_{IN}\left(\frac{1}{\pi} + \frac{1}{2}\sin(2\pi ft) - \frac{2}{\pi}\sum_{n=2,4,6,\ldots}^{\infty}\frac{cos(2n\pi ft)}{n^2-1}\right) \qquad (4)$$

By comparing the Fourier series of I_{IN} for the fresh (Fig. 2(a)) and degraded (Fig. 2(c)) inverters, we can observe that, in the degraded inverter, I_{IN} presents the same DC component as in the fresh inverter, and harmonics at multiples of 100Hz (i.e., at 100Hz, 200Hz, 300Hz, etc.) as in the fresh inverter, but with a lower amplitude. From Eq. (4) and Fig. 2(c), we can note that, in the degraded inverter, the harmonics are reduced by a value proportional to ΔI_{IN}. Such reductions may be in practice negligible, since the value of ΔI_{IN} is typically much lower than the amplitude of I_{IN} (I_{INp}).

Moreover, from Eq. (4) and Fig. 2(c) we can observe that the I_{IN} of the degraded inverter presents an additional harmonic component at 50Hz ($I_{IN,50Hz}$), which was not present in the fresh inverter. The amplitude of $I_{IN,50Hz}$ is proportional to ΔI_{IN}, so that it is also proportional to the value of the degraded MOSFET R_{ON} (ΔR_{ON}).

As for the output current, in the degraded inverter the Fourier series of I_{OUT} can be also obtained as the superposition of: 1) the Fourier series of I_{OUT} in the non-degraded inverter (Eq. 3); 2) the Fourier series of a half-rectified sine wave with an amplitude equal to the current mismatch ΔI_{OUT}. The resulting Fourier series of I_{OUT} for the degraded inverter is expressed by Eq. (5) below, and is schematically represented in Fig. 2(d).

$$I_{OUT}(t) = I_{OUTp} \cdot \sin(2\pi f t) - \Delta I_{OUT}\left(\frac{1}{\pi} + \frac{1}{2}\sin(2\pi f t) - \frac{2}{\pi}\sum_{n=2,4,6,\ldots}^{\infty} \frac{cos(4n\pi f t)}{n^2 - 1}\right) \quad (5)$$

By comparing the Fourier series of I_{OUT} for the fresh (Fig. 2(b)) and degraded (Fig. 2(d)) inverters, we can see that, in the degraded inverter, I_{OUT} still presents an harmonic at 50Hz, but with an amplitude reduced by a value proportional to ΔI_{OUT}. Such a reduction may be in practice negligible, since the value of ΔI_{OUT} is typically much lower than the amplitude of I_{OUT} (I_{OUTp}).

Finally, we can see that, in the degraded inverter, I_{OUT} presents an additional DC component and additional harmonics at multiples of 100Hz (i.e., at 100Hz, 200Hz, 300Hz, etc.), that were not present in the I_{OUT} of the fresh inverter. The amplitude of the additional harmonics is proportional to ΔI_{OUT}, so that they are also proportional to the value of the degraded MOSFET R_{ON} (ΔR_{ON}).

The results achieved by the described analytical analyses have also been verified by means of electrical level simulations performed by LTspice [32].

In our simulations, we emulated the increase in R_{ON} during circuit lifetime due to aging by connecting a resistance (ΔR_{ON}) in series to the source of each transistor.

As for ΔR_{ON}, we have considered a range of values varying from 0Ω (for a fresh device) to 45mΩ (R_{ON_CRIT}). In particular, we have considered eleven different values of ΔR_{ON}: 0, 4.5, 9, 13.5, 21, 22.5, 27, 31.5, 36, 40.5 and 45mΩ.

Fig. 3 shows the obtained harmonic components of: a) the input current (I_{IN}) absorbed by the inverter from V_{CC} (Fig. 3(a)); b) the output current (I_{OUT}) delivered to the resistive load (Fig. 3(b)). Such harmonics have been obtained by performing the Fast Fourier Transform (FFT) of the time-domain waveforms of I_{IN} and I_{OUT} by LTspice. In particular, Fig. 3(a) and 3(b) report the harmonic components of I_{IN} and I_{OUT}, respectively, for four different values of ΔR_{ON} of the MOSFET M1: ΔR_{ON}=0mΩ (fresh device), ΔR_{ON} =4.5mΩ (0.5% increase wrt a fresh device), ΔR_{ON}=13.5mΩ (1.5% increase wrt a fresh device) and ΔR_{ON}=45mΩ (i.e., $R_{ON} = R_{ON\_CRIT}$).

As can be seen, the obtained simulation results are in good agreement with our previous analytical results (Fig. 2).

In particular, as for I_{IN}, the harmonic at 100Hz ($I_{IN,100Hz}$) presents a weak dependence on R_{ON}, while the 50Hz harmonic ($I_{IN,50Hz}$) shows a clear dependence on R_{ON}. As for I_{OUT}, the harmonic at 50Hz ($I_{OUT,50Hz}$) presents a weak dependence on R_{ON}, while the harmonic at 100Hz ($I_{OUT,100Hz}$) shows a clear dependence on the R_{ON} value.

The amplitude of $I_{IN,50Hz}$ is significantly larger than that of $I_{OUT,100Hz}$. In fact, the amplitude of $I_{IN,50Hz}$ changes from -82.5 dB (for ΔR_{ON} = 0mΩ), to -51.6 dB (for ΔR_{ON} = 45mΩ). Instead, the amplitude of $I_{OUT,100Hz}$ changes from -92.1 dB (for ΔR_{ON} = 0mΩ), to -62.7 dB (for ΔR_{ON} = 45mΩ).

To estimate the R_{ON} increase over lifetime, we have defined two dimensionless metrics, F_{IN} and F_{OUT}, as follows:

$$F_{IN} = 1000 \times \frac{I_{IN,50Hz}}{I_{IN,100Hz}} \tag{6}$$

$$F_{OUT} = 1000 \times \frac{I_{OUT,100Hz}}{I_{OUT,50Hz}} \tag{7}$$

In the following Subsections, we analyze how the metrics defined by (6) and (7) vary as a function of: 1) different degradation (*i.e.,* different values of ΔR_{ON}) for the transistors of the inverter; 2) different values of the power delivered by the inverter to the load (*i.e.,* different values of R_L); 3) different values of the power supply voltage (Vcc); 4) different transistor models (featuring different voltage ratings); 5) different values of the operating temperature; 6) variations on the MOSFETs parameters initial values; 7) presence of noise on the monitored currents (I_{IN} and I_{OUT}).

3.1 Results for Different Degradation of Inverter Transistors

Under real operating conditions, the four MOSFETs of the inverter in Fig. 1 can experience a different level of degradation. Therefore, each transistor can be characterized by a particular value of R_{ON}. To analyze this effect, we have considered four different representative cases: i) a single MOSFET (M1) experiences degradation (i.e., its R_{ON} increases with time), while the other three MOSFETs are fresh devices; ii) the two MOSFETs in the upper part of the inverter (M1 and M4) experience the same R_{ON} degradation, while the MOSFETs in the bottom part of the inverter (M2 and M3) are fresh devices; iii) one MOSFET in the upper part (M1) and one MOSFET in the bottom part (M2) of the inverter experience the same R_{ON} degradation, while the others (M3 and M4) are fresh devices; iv) all four MOSFETs experience the same R_{ON} degradation.

The obtained results are summarized in Fig. 4. In particular, Fig. 4(a) and Fig. 4(b) show F_{IN} and F_{OUT} for the four cases described above, as a function of the R_{ON} increase (ΔR_{ON}) in the degraded MOSFET(s). We can observe that F_{IN} and F_{OUT} change linearly with ΔR_{ON}. Moreover, in all four cases, F_{IN} presents a higher variation than F_{OUT}, as a function of ΔR_{ON}. The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} (i.e. the slopes $\delta F_{IN}/\delta \Delta R_{ON}$ and $\delta F_{OUT}/\delta \Delta R_{ON}$) are reported in Table 1. We can also observe that the highest variation of F_{IN} and F_{OUT} occurs when only a single MOSFET experiences degradation.

Based on these results, we have performed electrical level simulations to analyze the F_{IN} and F_{OUT} variations, depending on which one of the four inverter MOSFETs experiences a R_{ON} degradation. The achieved results are reported in Fig. 5, that shows the values of F_{IN} and F_{OUT}, as a function of ΔR_{ON} of any of the four MOSFETs of the inverter, when a single MOSFET is degraded. Particularly, Fig. 5(b) shows that the increase in F_{OUT} is approximately the same, independently of the degraded MOSFET. Instead, Fig. 5(a) shows that F_{IN} presents a higher increase, when an upper MOSFET (M1 or M4), rather than a bottom MOSFET (M2 or M3), is degraded. The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} for all the four transistors of the inverter are reported in Table 2.

3.2 Results for Different Power Values Delivered to the Load

Under real operating conditions, the power required by the load usually varies over time. Therefore, we have evaluated the effects of variations in the power delivered to the load on F_{IN} and F_{OUT}.

In order to emulate variations in the power delivered by the inverter, we have modified the value of the resistive load R_L that emulates the inverter load. In particular, we have considered three different realistic values for R_L: 1) $R_L = 1\Omega$ (power of 100W); 2) $R_L = 1.4\Omega$ (power of 70W); 3) $R_L = 1.8\Omega$ (power of 55W). In addition, we have considered the case of a single degraded MOSFET (M1) that, as discussed in Subsection 3.1, results in the highest increase of F_{IN} and F_{OUT}.

The achieved results are reported in Fig. 6. From Fig. 6(a), we can observe that the value of F_{IN} depends on R_L, while Fig. 6(b) shows that the value of F_{OUT} is less sensitive to R_L changes than F_{IN}. The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} as function of the resistance load R_L are reported in Table 3. For both F_{IN} and F_{OUT}, the sensitivity decreases with R_L but the variation is stronger in the case of F_{IN} (sensitivity variation of 21.4% in the case of F_{IN} and 5.3% in the case of F_{OUT}). Therefore, if the value of R_L is unknown (or is expected to change during operation), F_{OUT} can be more conveniently adopted than F_{IN} to estimate the variation of R_{ON}.

It is worth noticing that, when the value of R_L tends to infinite (i.e., when the ouput of the inverter is left in a high impedance state), the inverter input and output currents tend both to 0A. Therefore, also all harmonics of the input/output currents tend to 0, so that the resulting values of F_{IN} and F_{OUT} are meaningless.

3.3 Results for Different Power Supply Voltages

We have analyzed the impact of the inverter input voltage Vcc on the values of the metrics F_{IN} and F_{OUT}. The inverter input DC voltage value (Vcc) depends mainly on the PV system configuration and remains costant during the inverter operation. In fact, as clarified in Section 2, Vcc is provided by a battery that is usually placed between the output of the maximum power point tracker (MPPT) and the input of the inverter.

For our analyses, we have considered three different realistic V_{CC} values: 10V, 50V and 200V. We have also considered the case of a single degraded MOSFET (M1) that, as discussed in Subsection 3.1, results in the highest increase of F_{IN} and F_{OUT}.

The obtained simulation results are reported in Fig. 7(a) and Fig. 7(b) for F_{IN} and F_{OUT}, respectively. As can be seen, both F_{IN} and F_{OUT} have a linear dependence on ΔR_{ON}, with a slope strongly depending on the V_{CC} value.

The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} as function of the Vcc value are reported in Table 4. In particular, the sensitivity of F_{IN} increases as the value of Vcc increases. In fact, it is: $\delta F_{IN}/\delta\Delta R_{ON} = 0.1359\ m\Omega^{-1}$, for $V_{CC} = 10V$; $\delta F_{IN}/\delta\Delta R_{ON} = 0.1857\ m\Omega^{-1}$, for $V_{CC} = 50V$; $\delta F_{IN}/\delta\Delta R_{ON} = 0.2008\ m\Omega^{-1}$, for $V_{CC} = 200$ V. On the other hand, the sensitivity of F_{OUT} decreases as the value of Vcc increases. In fact, it is: $\delta F_{OUT}/\delta\Delta R_{ON} = 0.018\ m\Omega^{-1}$, for $V_{CC} = 10V$; $\delta F_{OUT}/\delta\Delta R_{ON} = 0.01273\ m\Omega^{-1}$, for $V_{CC} = 50V$; $\delta F_{OUT}/\delta\Delta R_{ON} = 0.01124\ m\Omega^{-1}$, for $V_{CC} = 200$ V.

It is worth noticing that, since Vcc is constant during the inverter operation, Fin and Fout can be easily evaluated for the considered Vcc.

3.4 Results for Different Transistor Models

Since different transistor devices are characterized by different characteristics, we have tested the proposed technique for three different MOSFET models: STP8NM60 by ST-Microelectronics [30], featuring a maximum voltage rating of 650V, IRF510 by Vishay [33], featuring a maximum voltage rating of 100V and RHU003N03 by Rohm [34], featuring a maximum voltage rating of 30V. Simulations have been carried out for eleven different values of ΔR_{ON} between 0 Ω and the critical value (approximately a 5% increase of the initial R_{ON} value). We have also considered the case of a single degraded MOSFET (M1) that, as discussed in Subsection 3.1, results in the highest increase of F_{IN} and F_{OUT}.

The obtained simulation results are reported in Fig. 8(a) and Fig. 8(b) for F_{IN} and F_{OUT}, respectively. As can be seen, both F_{IN} and F_{OUT} have a linear dependence on ΔR_{ON} for all transistor models, with a slope that is comparable for the investigated devices.

The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} for the investigated transistor models are reported in Table 5. The sensitivity variation among the different transistor models is higher in the case of F_{IN} (15.6%) than F_{OUT} (6.3%).

3.5 Results for Different Values of Operating Temperature

We have analyzed the impact of the inverter operating temperature on the values of the metrics F_{IN} and F_{OUT}. For our analysis, we have considered five different temperatures: 15 °C, 27 °C, 38 °C, 70 °C and 120 °C. We have also considered the case of a single degraded MOSFET (M1) that, as discussed in Subsection 3.1, results in the highest increase of F_{IN} and F_{OUT}.

The obtained simulation results are reported in Fig. 9(a) and Fig. 9(b) for F_{IN} and F_{OUT}, respectively. As can be seen, both F_{IN} and F_{OUT} present a low variation with the inverter operating temperature. In particular, for the considered operating temperatures, F_{IN} and F_{OUT} present an average variation (over the considered range of MOSFET ΔR_{ON} degradation) of only 9.5% and 10.2%, respectively.

The values of the sensitivity of F_{IN} and F_{OUT} to ΔR_{ON} for the investigated operating temperatures are reported in Table 6.

Therefore, F_{IN} and F_{OUT} present only a small dependence on the inverter operating temperature, so that no temperature compensation is needed for F_{IN} and F_{OUT}.

3.6 Results for Variations on the MOSFETs Parameters Initial Value

We have analyzed the impact of MOSFET parameter variations occurring during fabrication on the values of the metrics F_{IN} and F_{OUT}. For this analysis, we have performed Monte Carlo simulations considering statistical variations (with uniform distribution) up to 10% of the MOSFETs: threshold voltage, intrinsic conductance, and initial ON-state resistance R_{ON}. As in the previous Subsections, for Monte Carlo simulations we have considered the degradation (i.e., ΔR_{ON} increase) of a single MOSFET (M1) that, as discussed above, results in the highest increase of F_{IN} and F_{OUT}.

The obtained results have shown that variations of the MOSFETs' threshold voltage and intrinsic conductance negligibly affect the values of F_{IN} and F_{OUT} (Eqs 6 and 7, respectively).

On the other hand, we have observed that variations of the initial value of R_{ON} result in significant variations of F_{IN} and F_{OUT}. As an example, Figs. 10(a) and 10(b) report some simulation results showing the values of F_{IN} and F_{OUT} as a function of ΔR_{ON} increase, respectively, for the following four different combinations of the initial R_{ON} value of the four MOSFETs: 1) the ideal case with the four MOSFETs presenting the same R_{ON} (considered as a reference); 2) M4 presenting a R_{ON} 22.5mΩ higher than the initial R_{ON} value, and the other MOSFETs presenting the initial R_{ON} value; 3) M4 presenting a R_{ON} 22.5mΩ higher than the initial R_{ON} value, both M2 and M3 presenting a R_{ON} 9mΩ higher than the initial R_{ON} value, and M1 presenting the initial R_{ON} value.

As anticipated before, variations of MOSFETs' R_{ON} result in significant variations of F_{IN} and F_{OUT} with respect to the values obtained for the ideal case of the four MOSFETs with the initial R_{ON} value. Moreover, from Figs. 10(a) and (b) we can also observe that, for some cases, F_{IN} and F_{OUT} present a non-monotonous variation with ΔR_{ON} (i.e., F_{IN} and F_{OUT} initially decrease with ΔR_{ON} up to a given ΔR_{ON} value, to then increase). This non-monotonous variation is caused by the unbalance between the currents flowing through the inverter's M1-M3 and M2-M4 transistor series.

However, the effects of R_{ON} variations on F_{IN} and F_{OUT} can be easily compensated, by applying the following linear transformations:

$$F^*_{IN,k} = \begin{cases} 0 & k = 0 \\ F^*_{IN,k-1} + \left|F_{IN,k} - F_{IN,k-1}\right| & k = 1,2,3 \ldots \end{cases} \tag{8}$$

$$F^*_{OUT,k} = \begin{cases} 0 & k = 0 \\ F^*_{OUT,k-1} + \left|F_{OUT,k} - F_{OUT,k-1}\right| & k = 1,2,3 \ldots \end{cases} \tag{9}$$

where $F_{IN,k}$ and $F_{OUT,k}$ are the values of F_{IN} and F_{OUT} at the k^{th} sample of ΔR_{ON}.

As an example, Figs. 11(a) and 11(b) show the values of the compensated metrics F^*_{IN} and F^*_{OUT} as a function of ΔR_{ON} increase, respectively, for the same R_{ON} variations considered for the simulations in Figs. 9(a) and 9(b).

As can be seen from Figs. 11(a) and (b), the compensated metrics F^*_{IN} and F^*_{OUT} are in very good agreement with the metrics F_{IN} and F_{OUT} obtained for the ideal case where the four MOSFETs of the inverter present the initial R_{ON} value.

For simplicity, in the remainder of the paper we will assume that the four MOSFETs of the inverter present the initial R_{ON} value (900 mΩ). However, as clarified before, should this be not the case, the transformations defined by Eqs. (8) and (9) could be applied to compensate R_{ON} variations.

3.7 Results for Noisy Inverter Currents

We have also performed simulations to evaluate the impact on F_{IN} and F_{OUT} of noise affecting the inverter input/output currents. We have considered again the case of aging degradation on a single MOSFET (M1). We have added different levels of white noise (with peak amplitudes of 0.01A, 0.05A, 0.2A and 0.5A, corresponding to 1%, 5%, 20% and 50% of I_{IN} amplitude, respectively) to the inverter input (I_{IN}) and output (I_{OUT}) currents. We have also evaluated the effects of noise, as a function of the number of periods used in the FFT to derive the I_{IN} and I_{OUT} harmonics. For our analyses we have considered 5, 30, 60 and 100 periods.

As an example, Fig. 12 reports the obtained results for F_{OUT}. In particular, Fig. 12(a) and Fig. 12(b) report the standard deviation of the F_{OUT} distribution, as a function of the noise amplitude and the number of I_{OUT} periods (used to calculate F_{OUT}), respectively. As expected, the standard deviation increases linearly with the noise amplitude, while it decreases with the reciprocal of the square root of the number of analyzed periods. Therefore, for a given value of expected noise amplitude, the accuracy in the estimation of F_{OUT} can be improved by simply increasing the number of periods used to calculate the I_{OUT} FFT.

Moreover, Fig. 12(c) reports the distribution of F_{OUT} values for four different values of R_{ON}, considering 100 periods to evaluate the I_{OUT} FFT. Finally, Fig. 12(d) shows the average value of F_{OUT}, as a function of the R_{ON} increase (ΔR_{ON}), for the considered four different levels of noise. As can be seen, ΔR_{ON} due to aging can be accurately estimated from F_{OUT}, also in case of high levels of noise, if the current is averaged on a suitable number of periods.

Similar results have been obtained also for F_{IN}, but for the fact that F_{IN} is characterized by a higher signal-to-noise ratio than F_{OUT}. This can be observed from Table 7, where the coefficient of variation (CV), *i.e.*, the ratio between the standard deviation and the mean value, is reported for the distributions of both F_{IN} and F_{OUT}, for different numbers of periods and different levels of noise.

The maximum error in the estimation of R_{ON} at the critical value ($R_{ON,CRIT}$, i.e. 5% increase on the value of R_{ON} for the fresh device) for four different number of analysed periods (5, 30, 60 and 100) and four different noise levels (0.01A, 0.05A, 0.2A and 0.5A) has been also calculated and the results are presented in Table 8.

Therefore, the results reported in Fig. 12 and Table 8 demonstrate that both F_{IN} and F_{OUT} can be used to estimate accurately ΔR_{ON}, also in case of noisy environment, provided that the monitored currents are averaged on a suitable number of periods. Since F_{IN} is characterized by a higher signal-to-noise ratio, the same level of accuracy can be achieved in a shorter time by considering F_{IN}, rather than F_{OUT}.

4. Proposed early detection strategy

The simulation results described in Section 3 have shown that the increase in the MOSFET R_{ON} (ΔR_{ON}) can be estimated by means of the introduced F_{IN} and F_{OUT} metrics, which are derived from the monitored input and output currents of the inverter.

Based on these results, in this section we propose a strategy for the early detection of inverter faults, which can be periodically activated (after a programmable time interval t_{det}) during the inverter in-field operation. The basic idea of our approach is to calculate the values of the F_{IN} and F_{OUT} metrics associated to each MOSFET of the inverter, and to generate an alarm message when they become equal or higher than those corresponding to the MOSFET R_{ON} critical value. It should be noted that our strategy can be performed concurrently with the inverter normal operation in the field, thus not affecting the PV system power efficiency.

Our proposed strategy is based on the algorithm schematically represented in Fig. 13, that can be implemented by simple modifications to the inverter internal structure and using the microcontroller that is typically embedded within the electronic control circuitry of PV systems. As shown in Fig. 13, initially an Alarm signal is set to 0, and a timer is set to a desired value t_{det}, after which our detection strategy is activated. The timer is performing a count down during the inverter normal operation. When the timer reaches the 0 value, our strategy is activated, and calculates (as described later in this Section) the values of the metrics F_{IN} and F_{OUT} associated to the R_{ON} increase of each MOSFET of the inverter (i.e., F_{IN_i} and F_{OUT_i}, i = 1, …, 4).

The calculated F_{IN_i} and F_{OUT_i} values are compared to their respective critical values ($F_{IN\_i\_CRIT}$ and $F_{OUT\_i\_CRIT}$), which have been obtained by simulations (as reported in the previous Section) and which correspond to the R_{ON} critical increase (*i.e.*, an increase of 5% over the R_{ON} initial value). It should be noted that our strategy can be applied to any kind of inverter, by properly deriving the $F_{IN\_i\_CRIT}$ and $F_{OUT\_i\_CRIT}$ values by performing simulations of the inverter.

As an example, these are the values of $F_{IN\_i\_CRIT}$ and $F_{OUT\_i\_CRIT}$ (i=1, …, 4) obtained by electrical level simulations of the considered inverter: $F_{IN\_1\_CRIT} = F_{IN\_4\_CRIT} = 5$, $F_{IN\_2\_CRIT} = F_{IN\_3\_CRIT} = 4$, and $F_{OUT\_i\_CRIT} = 0.7$ (i=1, …, 4).

According to our proposed algorithm, if at least one of the evaluated metrics is higher or equal than the respective critical value, an alarm message is activated (Alarm = 1). Otherwise, our early detection strategy maintains Alarm = 0, and sets the timer equal to t_{det} again. The generated alarm message can then be exploited at system level to activate a recovery approach, to replace the affected transistor before it actually becomes faulty.

In order to calculate the F_{IN_i} and F_{OUT_i} values, the inverter (Fig. 1) can be modified as schematically represented in Fig. 14.

As can be seen, we add two current sensors (CS1 and CS2) to measure the currents I_{IN} and I_{OUT}. As discussed in the previous Section, the values of these currents enable to derive the values of F_{IN} and F_{OUT}, as described by Eqs. (1) and (2). In order to make our scheme able to detect the MOSFET R_{ON} critical increase, the current sensors should feature a resolution high enough to measure the variations of the inverter currents' harmonics induced by the MOSFET R_{ON} increase. In particular, the increase of the 50Hz (100Hz) harmonics of the inverter input (output) current corresponding to the critical R_{ON} increase is of approximately 2.608mA (749.75 μA). Thus, current sensors CS1 and CS2 should feature a resolution high enough to measure such current values.

As an example, we implemented CS1 and CS2 by means of the Hall Effect sensors in [35], which feature a measurement resolution of approximately 76.3 μA, that is high enough to measure the variations of the inverter currents' harmonics induced by the MOSFET R_{ON} increase.

In particular, the current sensor CS1 generates a voltage $V_{HALL,IN} = k\ I_{IN}$, while the sensor CS2 generates a voltage $V_{HALL,OUT} = k\ I_{OUT}$, where k = 667mΩ is the equivalent transresistance of the considered Hall Effect current sensors. The voltages $V_{HALL,IN}$ and $V_{HALL,OUT}$ are acquired using the Analog to Digital Converter (ADC) integrated inside the microcontroller.

Moreover, as represented in Fig. 13, we need to calculate the F_{IN} and F_{OUT} associated to the increase in R_{ON} of each individual MOSFET of the inverter (*i.e.,* F_{IN_i} and F_{OUT_i} for Mi, i = 1, …, 4). To achieve this goal, the inverter internal structure can be modified by adding four additional MOSFETs (*i.e.,* M5-M8 in Fig 14) connected in parallel to the original inverter MOSFETs (*i.e.,* M1-M4). The additional MOSFETs (M5-M8) are conductive only when our scheme is activated to calculate the R_{ON} value of the M1-M4 MOSFETs. Therefore, the time intervals during which M5-M8 are conductive is negligible compared to the inverter lifetime. We can consequently reasonably assume that the extra MOSFETs (M5-M8) are minimally degraded over time, and that they can always be considered as fresh devices.

Moreover, we added a control circuitry (Control Block – CB in Fig. 14), that receives signal $V_{HALL,IN}$ from CS1, $V_{HALL,OUT}$ from CS2, and V_A and V_B from the Inverter Control Circuitry. CB generates eight independent control signals (V_i, i=1, …, 8) to control the state of conductance of the eight transistors (Mi, i=1, …, 8) in the modified inverter. In addition, CB generates the Alarm signal, that is activated when the increase in R_{ON} of one of the original MOSFETs composing the inverter (M1…M4) reaches the critical value.

In particular, in the time intervals during which our strategy is not activated, CB makes $V_5 = V_6 = V_7 = V_8 = 0$, so that all additional MOSFETs (M5-M8) are OFF. Moreover, during this time interval, CB makes $V_1 = V_3 = V_B$ and $V_2 = V_4 = V_A$. This way, the original MOSFETs (M1-M4) are driven by signals V_A and V_B, as in the unmodified inverter in Fig. 1.

Instead, in the time intervals during which our strategy is activated, CB alternatively replaces the original transistors (M1-M4) with the fresh MOSFETs (M5-M8). This way, the values of F_{IN_i} and F_{OUT_i} for Mi (i = 1, …, 4) can be evaluated, as required by our early detection strategy.

In order to calculate the values of F_{IN_i} and F_{OUT_i} for a given Mi (i = 1, …, 4), CB maintains the aged transistor M_i ON, and makes OFF the remaining three aged transistors. As an example, in order to determine F_{IN_1} and F_{OUT_1} for M_1, CB makes: a) $V_1 = V_B$, so that M1 works as during the inverter normal operation; b) $V_5 = 0$, so that the additional transistor M5 is OFF; c) $V_2 = V_3 = V_4 = 0$, so that the remaining inverter original transistors (M2, M3, M4) are all OFF; d) $V_6 = V_8 = V_A$, so that the additional fresh transistors M6 and M8 are ON, while M2 and M4 are OFF; e) $V_7 = V_B$, so that the additional fresh transistor M7 is ON, while M2 is OFF. Under these conditions, the values of F_{IN_1} and F_{OUT_1} for M1 can be obtained by measuring signals $V_{HALL,IN}$, and $V_{HALL,OUT}$. As described in Section 3, in order to make the measurement robust against noise, many periods of signals $V_{HALL,IN}$ and $V_{HALL,OUT}$ can be taken. The metrics F_{IN_i} and F_{OUT_i} (i = 2, 3, 4) are calculated in a similar way.

As described before in this Section, CB compares the values of F_{IN_i} and F_{OUT_i} (i = 1, …, 4) to their respective critical values $F_{IN\_i\_CRIT}$ and $F_{OUT\_i\_CRIT}$. If it is $F_{IN\_i} \geq F_{IN\_i\_CRIT}$, or $F_{OUT\_i} \geq F_{OUT\_i\_CRIT}$ (i = 1, …, 4), CB makes Alarm = 1, so that a proper recovery approach can be activated. Otherwise, CB keeps Alarm = 0.

As discussed in Subsection 3.2, when the value of R_L tends to infinite (i.e., when the ouput of the inverter is left in a high impedance state) the inverter input and output currents tend both to 0A. Thus, also all harmonics of the input/output currents tend to 0, so that the resulting values of F_{IN} and F_{OUT} are meaningless. Therefore, our approach is able to estimate the MOSFETs' R_{ON} increase only in the time intervals during which the current absorbed by the load is different from 0A (which corresponds to an infinite load, or open circuit). In order to cope with this issue, we can simply enable our detection approach only in the time intervals during which the current absorbed by the load is different from 0, which occurs most of the time in PV inverters.

As for area overhead, our scheme requires four extra MOSFETs (M5-M8), thus some additional area on the board implementing the H-bridge of the inverter. However, the area overhead required by such extra transistors is very limited compared to that of the inverter electronic control circuitry, so that it can be considered negligible with respect to the inverter overall area. Moreover, as reported in [36], the cost of power semiconductor devices represents approximately only the 3.5% of the cost of typical inverters used in PV systems. Therefore, the additional 4 MOSFETs required to implement our detection strategy imply a minimal cost increase over the original PV inverter. Additionally, the four additional MOSFETs required to implement our strategy can be integrated on a separate PCB board, with no need to modify the inverter’s design.

As for the power consumed by our scheme, it is negligible compared to the power consumed by the inverter. In fact, the extra power consumed by our scheme is due to the signal elaboration performed by CB, which is negligible compared to the power consumed/dissipated by the inverter.

Our strategy can be performed concurrently with the inverter normal operation in the field, thus not affecting the PV system power efficiency.

Finally, even though our scheme has not been specifically designed to detect faults (*e.g.,* opens or shorts [16, 17]) affecting the inverter external power diodes (D1-D4), it can detect the effects of such faults that result in a reduction of the PV inverter efficiency. As clarified in Section 2, these diodes are normally OFF during the inverter normal operation in the field. They are used only to protect the

MOSFETs from possible high voltage glitches at the output of the inverter, that may occur as a consequence of the non-simultaneous switching of the MOSFETs (e.g., due to possible small delays among their control signals) when the inverter is driving high inductive loads.

In particular, as for shorts affecting the diodes, it has been shown [19, 20] that they result in a significant distortion on the inverter output current, with a significant increase of its 100Hz harmonic component, and a significant impact on the inverter's power delivered to the load. Since the increase in the 100Hz harmonic of the inverter output current due to a diode failing as a short is higher than that observed for the case of a MOSFET R_{ON} increase higher than the critical value, our scheme will detect also diodes failing as shorts.

As for opens affecting the diodes, they do not affect the inverter output current [19, 20]. Therefore, they cannot be detected by our scheme. However, since such diodes are normally OFF, these faults do not affect the operation of the inverter in the field, and they do not impact the power delivered to the load. However, opens affecting diodes inhibit the protection of the MOSFETs against possible high voltage glitches at the output of the inverter. Consequently, the MOSFETs may successively be affected by catastrophic faults (i.e., failing as opens or shorts, due to high voltage glitches at the output of the inverter), with a consequent impact on the inverter's power delivered to the load. However, after a MOSFET catastrophic fault, the inverter output current will present a significant distortion [19, 20], with a considerable increase of its 100Hz harmonic component (which will be higher than that observed for a MOSFET R_{ON} increase higher than the critical value). Therefore, although our scheme does not directly detect opens affecting the diodes, it enables to detect possible MOSFET catastrophic faults, that result in a reduction of the PV inverter efficiency.

5. Conclusions

In this paper, we have shown that the increase in the MOSFET ON-state resistance can be easily related to the change in the harmonic components of the inverter's input/output currents. We have shown that the 50Hz (100Hz) harmonic of the inverter input (output) current presents an approximately linear increase, with the increase in the ON-state resistance of the MOSFETs. Our analyses enable to identify the values of the harmonics of the inverter's input/output currents that correspond to the critical value of MOSFET ON-state resistance.

Based on these results, we have then proposed an innovative strategy for the early detection (also referred to as condition monitoring) of inverter faults, which enables the generation of an alarm message when the ON-state resistance of any MOSFET of the inverter reaches the critical value. Upon the generation of such an alarm message, recovery strategies can be activated, to enable the online replacement of the affected transistors before they actually become faulty, thus avoiding energy efficiency loss. Our early detection strategy can be implemented by simple modifications to the inverter internal structure and using the microcontroller that is typically embedded within the control circuitry of PV systems. Finally, our strategy does not require to interrupt the inverter normal operation in the field, thus not affecting the PV system power efficiency.

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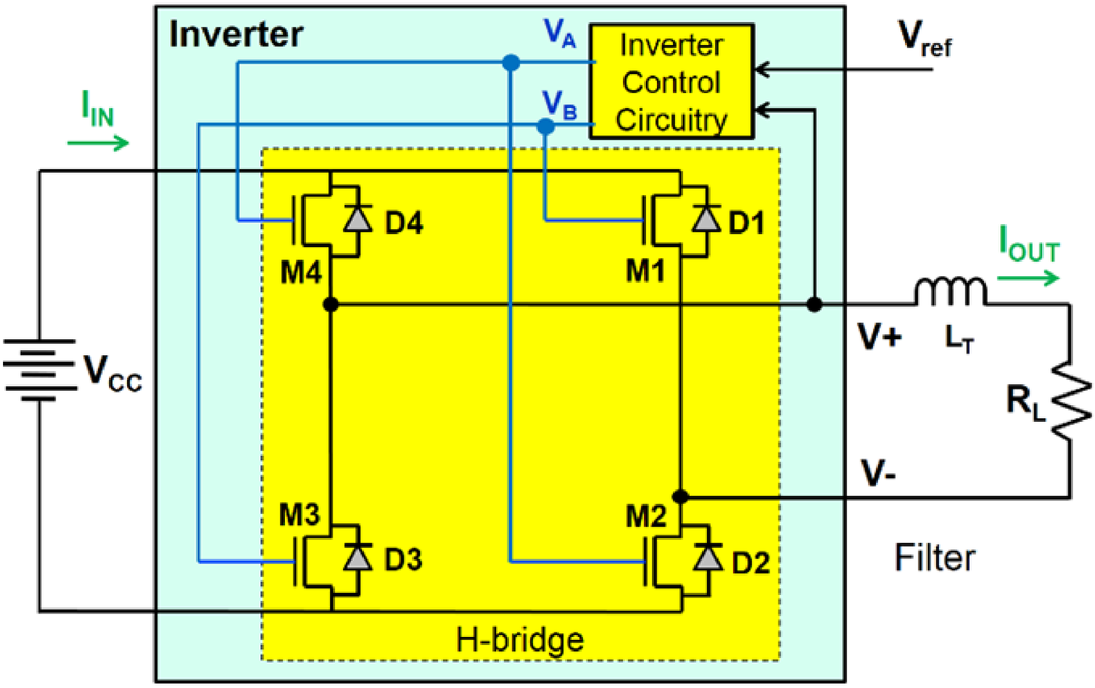

Fig. 1 Schematic representation of the considered inverter.

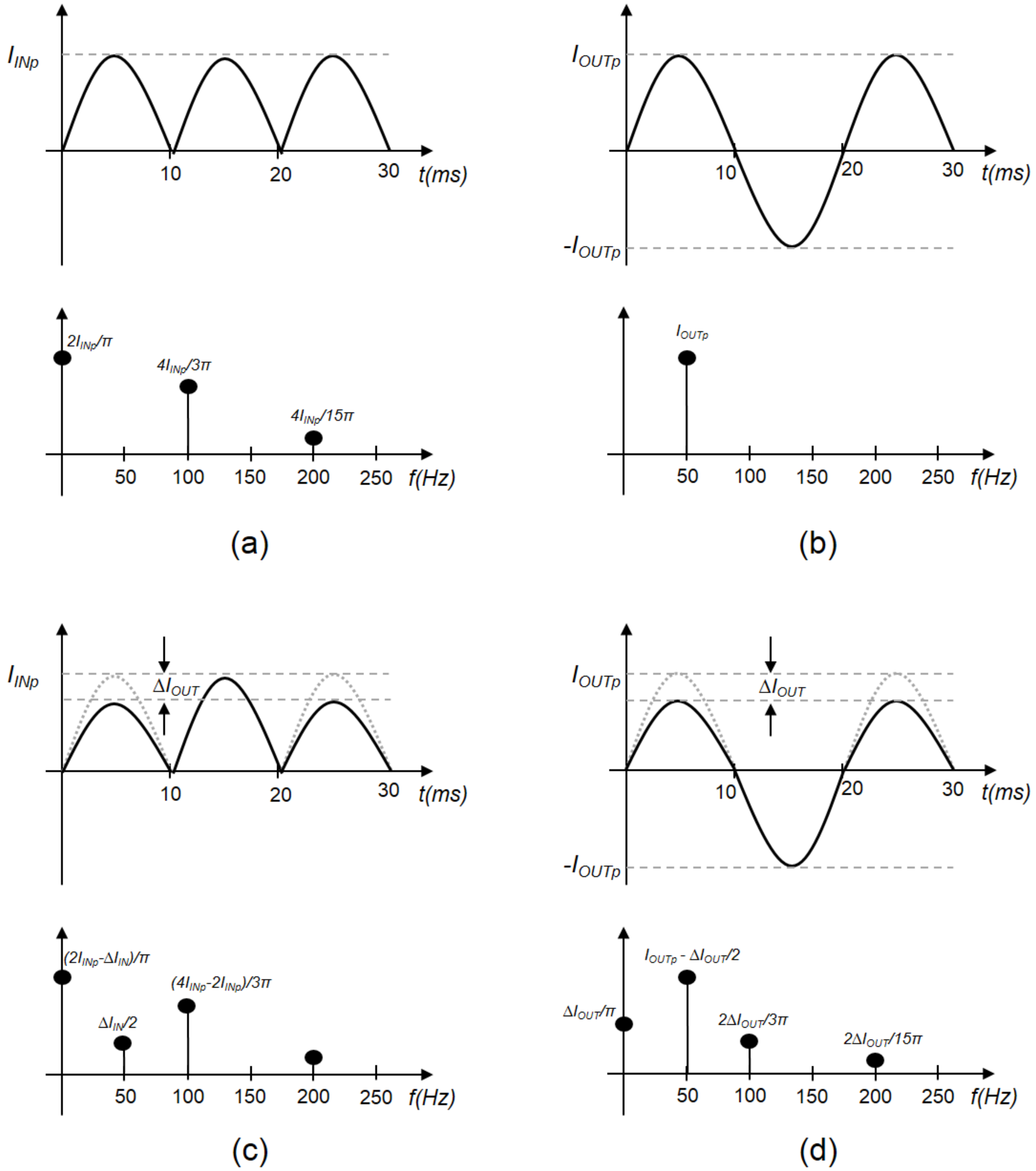

Fig. 2 Schematic representation of the inverter input/output waveforms and their Fourier series: a) I_{IN} and first components of its Fourier series for a fresh inverter; b) I_{OUT} and first components of its Fourier series for a fresh inverter; c) I_{IN} and first components of its Fourier series for a degraded inverter; d) I_{OUT} and first components of its Fourier series for a degraded inverter.

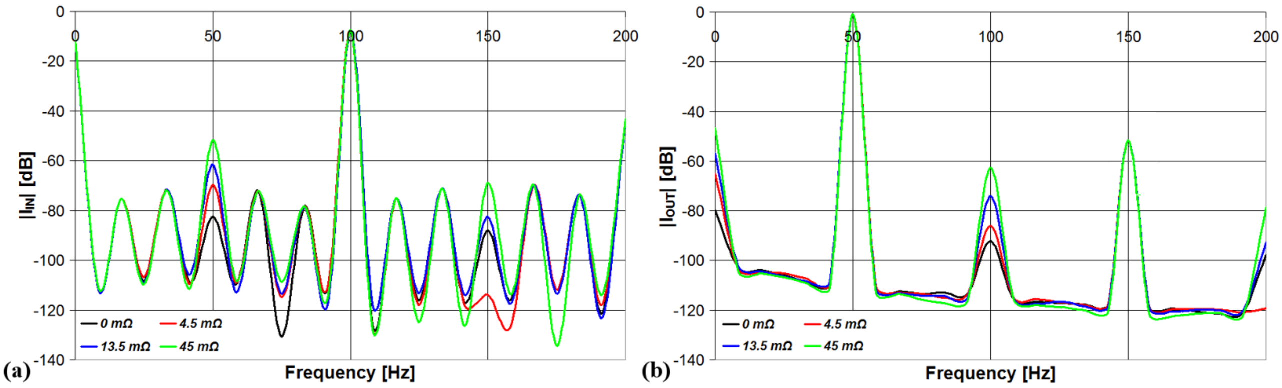

Fig. 3 Harmonic components of (a) the inverter input current (I_{IN}), and (b) the inverter output current (I_{OUT}), for the case of four different values of R_{ON} increase of the MOSFET M1 (Fig. 1): $\Delta R_{ON} = 0\Omega$ (for fresh device), $\Delta R_{ON} = 4.5m\Omega$, $\Delta R_{ON} = 12.5m\Omega$ and $\Delta R_{ON} = 45m\Omega$ ($R_{ON} = R_{ON\_CRIT}$).

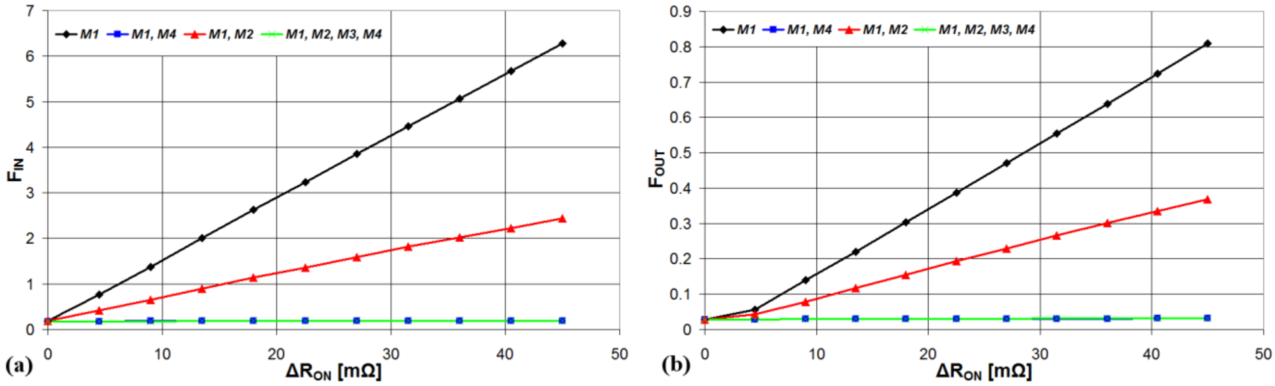

Fig. 4 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the change in the transistor ON-state resistance (ΔR_{ON}), for the case of degradation of a different number of transistors composing the inverter.

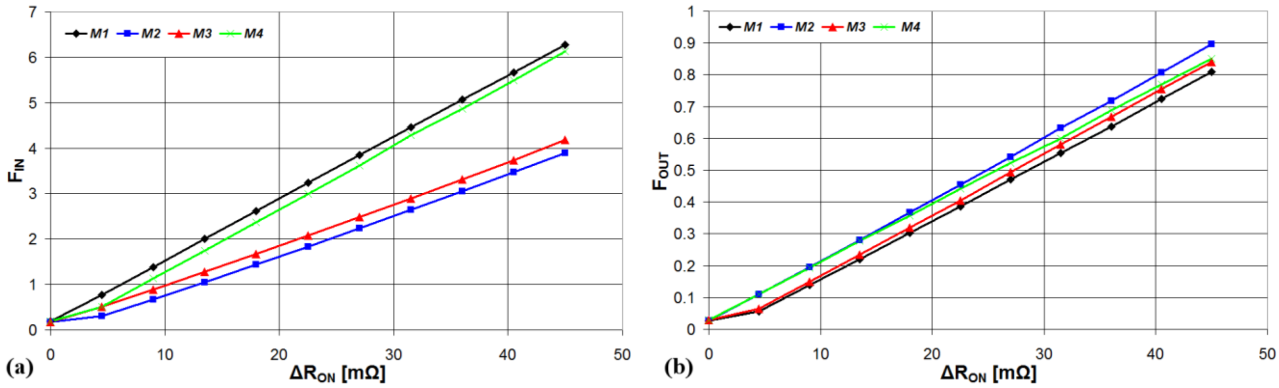

Fig. 5 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as function of the change in the transistor ON-state resistance (ΔR_{ON}), for the case of degradation of a single transistor.

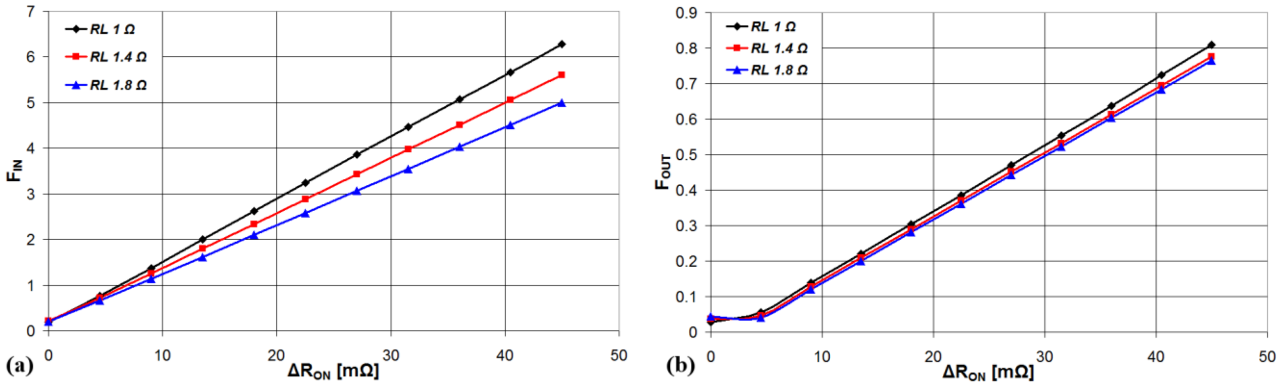

Fig. 6 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for different values of resistive load.

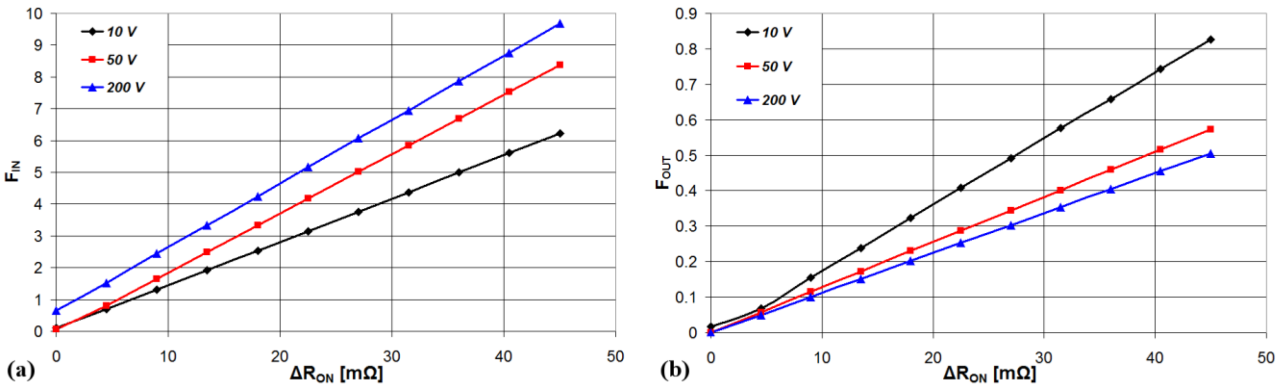

Fig. 7 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for different values of the power supply.

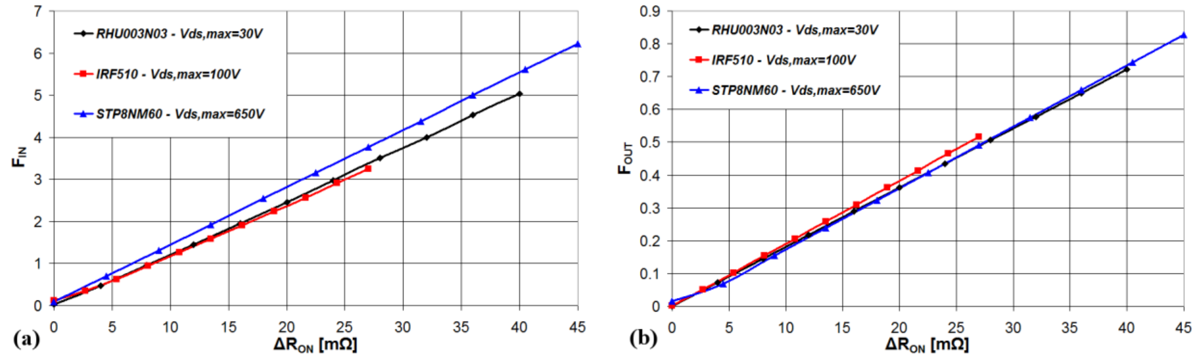

Fig. 8 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for different transistor models.

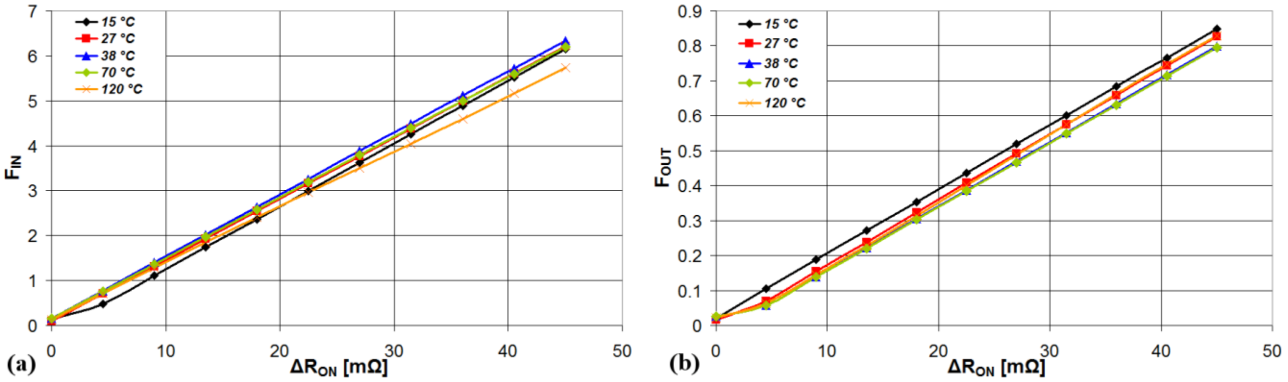

Fig. 9 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for different values of operating temperature.

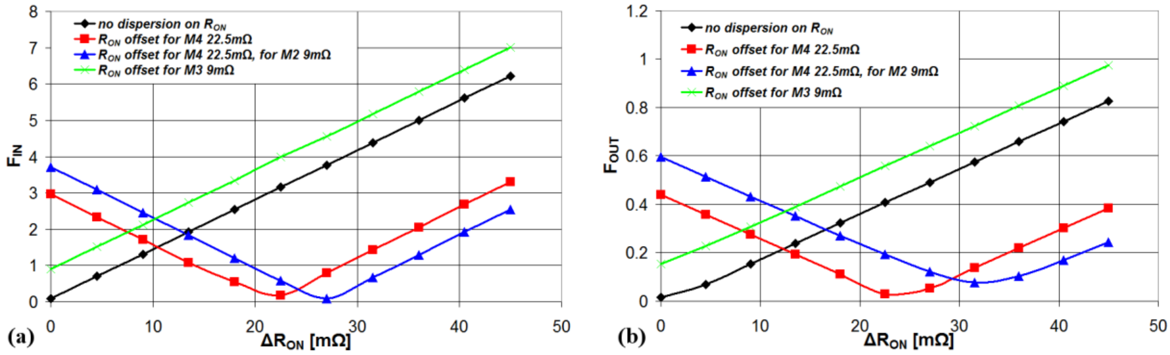

Fig. 10 Results of the performed simulations showing the variation of F_{IN} (a) and F_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for four different combinations of the initial values of the ON-state resistance (R_{ON}) of the inverter transistors.

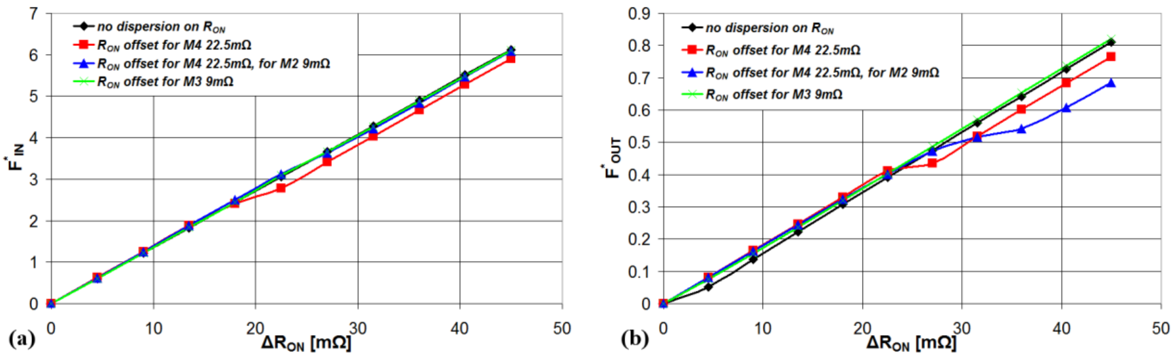

Fig. 11 Results of the performed simulations showing the variation of the corrected parameters F^{*}_{IN} (a) and F^{*}_{OUT} (b), as a function of the variation of the M_1 transistor ON-state resistance (ΔR_{ON}), for four different combinations of initial values of the ON-state resistance (R_{ON}) of the inverter transistors.

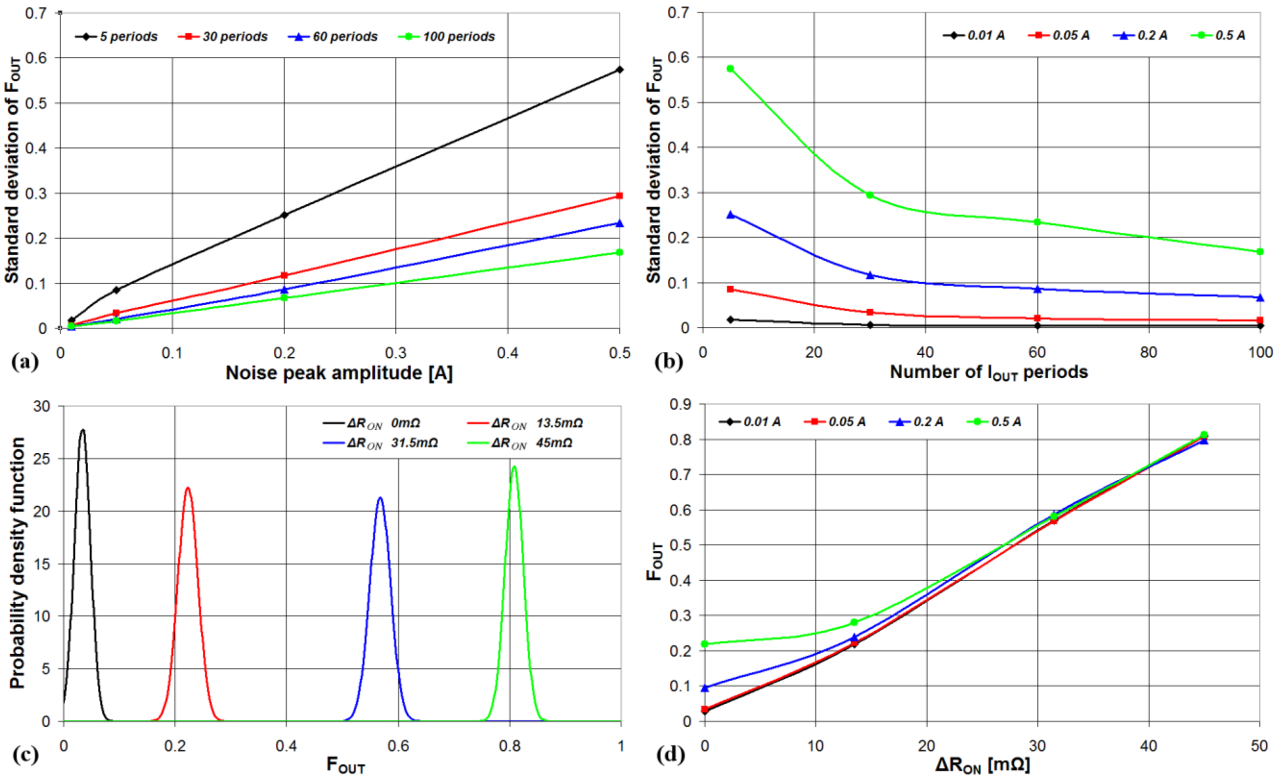

Fig. 12 Results of the performed simulations reporting the effects of noise on F_{OUT}: (a) Standard deviation of the F_{OUT} distribution, as a function of noise amplitude; (b) Standard deviation of the F_{OUT} distribution, as a function of the number of considered I_{OUT} periods; (c) Distribution of F_{OUT} for four different values of transistor R_{ON}; (d) Mean value of the F_{OUT} distribution, as a function of the transistor R_{ON} increase for four different values of noise peak amplitude.

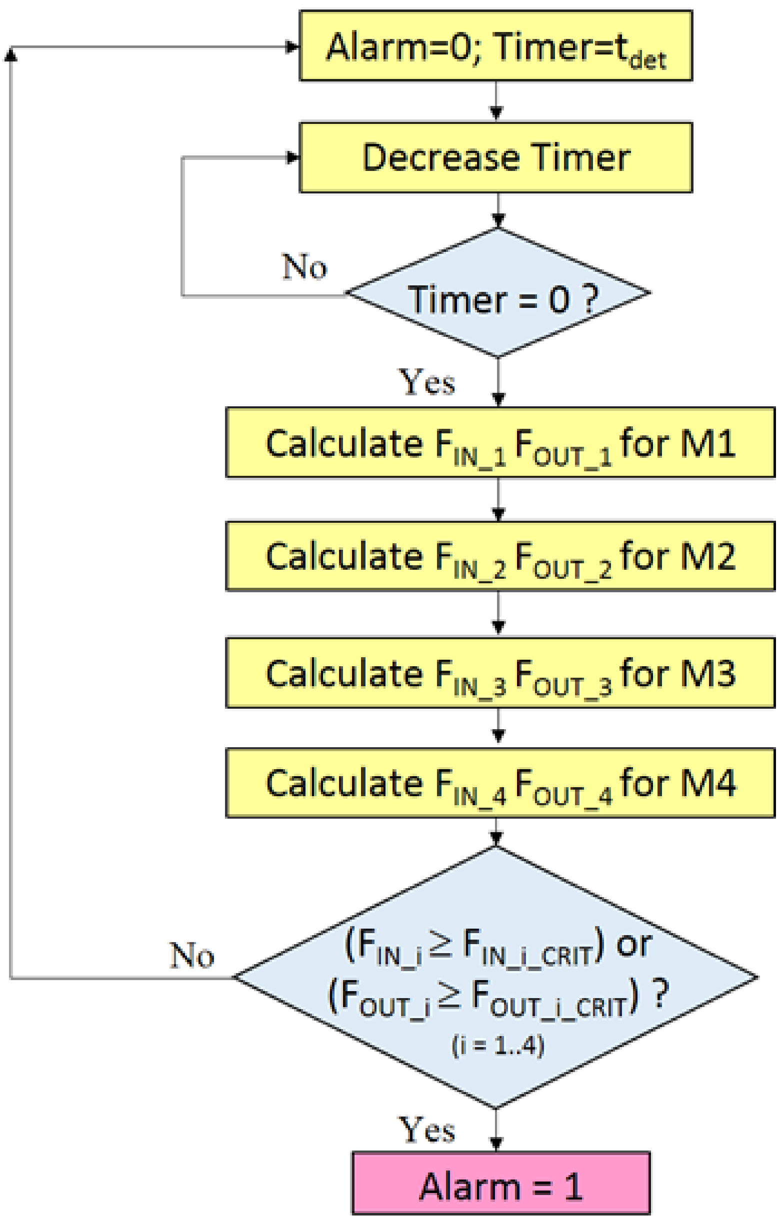

Fig. 13 Innovative algorithm used by our proposed strategy to early detect the increase in R_{ON} of MOSET transistors of PV inverters.

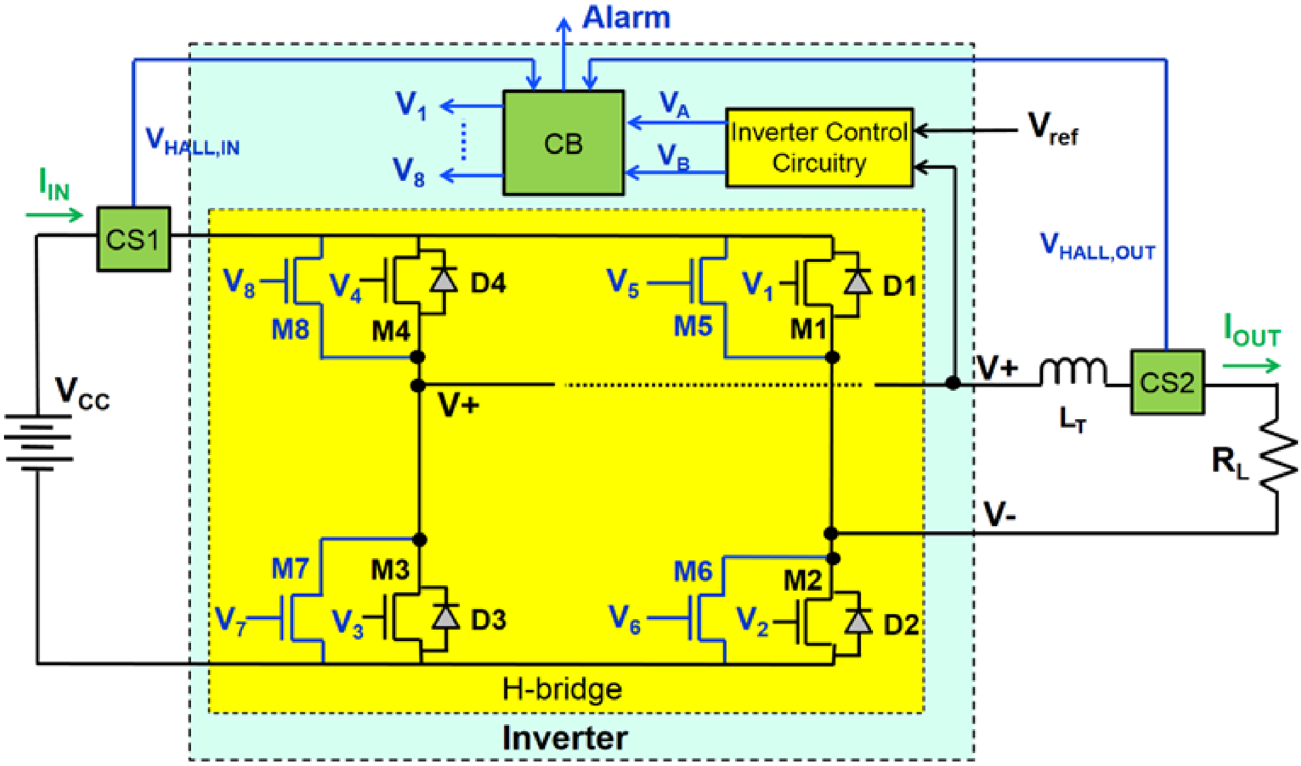

Fig. 14 Modifications to the inverter structure (Fig. 1) to implement our proposed early detection strategy.

Table 1 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of aging affecting a different number of MOSFETs in the inverter circuit.

Aged transistors	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
M1	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$
M1 M2	$50.3 \cdot 10^{-3}$	$7.9 \cdot 10^{-3}$
M1 M4	$0.289 \cdot 10^{-3}$	$0.08 \cdot 10^{-3}$
M1 M2 M3 M4	$0.442 \cdot 10^{-3}$	$0.08 \cdot 10^{-3}$

Table 2 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of aging affecting a single MOSFET in the inverter circuit.

Aged transistor	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
M1	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$
M2	$85.59 \cdot 10^{-3}$	$19.35 \cdot 10^{-3}$
M3	$89.17 \cdot 10^{-3}$	$18.69 \cdot 10^{-3}$
M4	$135.6 \cdot 10^{-3}$	$18.27 \cdot 10^{-3}$

Table 3 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of different values of the resistive load R_L.

R_L (Ω)	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
1	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$
1.4	$120.1 \cdot 10^{-3}$	$17.29 \cdot 10^{-3}$
1.8	$106.84 \cdot 10^{-3}$	$17.04 \cdot 10^{-3}$

Table 4 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of different values of the power supply voltage (V_{cc}).

V_{cc} (V)	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
10	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$
50	$185.73 \cdot 10^{-3}$	$12.73 \cdot 10^{-3}$
200	$200.82 \cdot 10^{-3}$	$11.24 \cdot 10^{-3}$

Table 5 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of different transistor devices.

Transistor model	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
RHU003N03 $V_{ds,max}$=30V	$125.98 \cdot 10^{-3}$	$18.04 \cdot 10^{-3}$
IRF510 $V_{ds,max}$=100V	$117.58 \cdot 10^{-3}$	$19.14 \cdot 10^{-3}$
STP8NM60 $V_{ds,max}$=650V	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$

Table 6 Sensitivity of F_{IN} and F_{OUT} to R_{ON} increase (ΔR_{ON}) in the case of different operative temperatures (T).

T (°C)	$\partial F_{IN}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)	$\partial F_{OUT}/\partial \Delta R_{ON}$ ($m\Omega^{-1}$)
15	$137.01 \cdot 10^{-3}$	$18.38 \cdot 10^{-3}$
27	$135.94 \cdot 10^{-3}$	$18 \cdot 10^{-3}$
38	$137.42 \cdot 10^{-3}$	$17.81 \cdot 10^{-3}$
70	$134.36 \cdot 10^{-3}$	$17.71 \cdot 10^{-3}$
120	$123.87 \cdot 10^{-3}$	$18.59 \cdot 10^{-3}$

Table 7 Relative variation of F_{IN} and F_{OUT} for four different number of analysed periods (5, 30, 60 and 100) and four different noise levels (0.01A, 0.05A, 0.2A and 0.5A).

	Input current I_{IN}				Output current I_{OUT}			
Noise [A]	5 periods	30 periods	60 periods	100 periods	5 periods	30 periods	60 periods	100 periods
0.01	0.005903	0.002419	0.001540	0.001173	0.021131	0.007324	0.005700	0.004531
0.05	0.025067	0.011316	0.008316	0.006771	0.104254	0.042054	0.025633	0.020249
0.2	0.127359	0.042950	0.036231	0.027316	0.311237	0.144780	0.105939	0.083660
0.5	0.235996	0.125199	0.077709	0.071284	0.711855	0.364116	0.289329	0.207763

Table 8 Maximum error in the estimation of R_{ON} at the critical value for four different number of analysed periods (5, 30, 60 and 100) and four different noise levels (0.01A, 0.05A, 0.2A and 0.5A).

	Input current I_{IN}				Output current I_{OUT}			
Noise [A]	5 periods	30 periods	60 periods	100 periods	5 periods	30 periods	60 periods	100 periods
0.01	12μΩ	12μΩ	9μΩ	7μΩ	86μΩ	65μΩ	41μΩ	23μΩ
0.05	18μΩ	17μΩ	17μΩ	15μΩ	200μΩ	181μΩ	143μΩ	34μΩ
0.2	62μΩ	51μΩ	47μΩ	46μΩ	2.57mΩ	813μΩ	511μΩ	207μΩ
0.5	1.66mΩ	424μΩ	220μΩ	58μΩ	>40mΩ	5.88mΩ	2.77mΩ	435μΩ