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# Influence of the DLC Passivation Conductivity on the Performance of Silicon High-Power Diodes Over an Extended Temperature Range

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**ABSTRACT** The diamond-like carbon (DLC) is important for passivation of junction termination in high power devices due to its excellent electrical, mechanical, and thermal properties. While the role of conductivity and polarization of the DLC layer on the blocking capability of a p-n junction has been explained recently, the thermal behavior still needs to be addressed. For this purpose, the diode leakage current was measured on large area power diodes with negative bevel coated by the DLC in a typical industrial range between 300 and 413 K. An unusual deviation from the expected Arrhenius law was experimentally observed. A predictive TCAD model, which incorporates the effect of the DLC layer, has been developed to study the impact of the DLC layer parameters on diode thermal performance. Both the electrostatic features and charge transport mechanisms through and along the DLC/Silicon interface have been modeled over a wide range of temperatures. Different DLC/Silicon doping combinations have been analyzed to explain the main effects determining the temperature dependence of diode leakage current and breakdown voltage. A complete validation of the TCAD approach has been achieved.

**INDEX TERMS** Diamond-like carbon (DLC), junction termination (JT), negative bevel, power semiconductor devices, TCAD modeling.

## I. INTRODUCTION

The increase of maximal allowed junction temperature $T_{jmax}$ of power semiconductors while preserving long-term blocking stability belongs to one of three methods to increase the output current and hereby the efficiency of high-power converters. The $T_{jmax}$ of industrial silicon chips and discrete devices is nowadays ranging from 363 to 448 K depending on voltage class, packaging technology, and cooling concept. The parameter determining the blocking stability and hereby the $T_{jmax}$ is the leakage current $I_{OFF}$ generated in the active area and at junction termination (JT). The parameter determining the efficiency of device design is the size of the JT relative to the active area. The leakage current grows exponentially with increasing temperature T according to the Arrhenius law approximately as $exp[-Eg/(2k_BT)]$, where Eg is the energy gap and $k_B$ the Boltzmann constant [2]. The underlying physical mechanism is the thermal generation taking place in the depleted region of the pn-junction, which geometrically extends in the overall silicon active area up to the JT region. The only possibility to reduce this sort of leakage current is to reduce the concentration of deep energetic levels in the bandgap caused by a contamination and/or carrier lifetime control. What can further improve the situation is an optimized behavior of the JT in terms of robustness and area consumption, which depends on the surface passivation material and its processing.In addition to the electrostatic effect of the JT geometry and doping, if a semi-insulating passivation layer is used on top of the junction termination of the diode, $I_{OFF}$ (T) is influenced also by the conductivity features of the passivation material leading to a modulation of the leakage current. A physically-based model of the passivation layer is thus needed for optimization of the

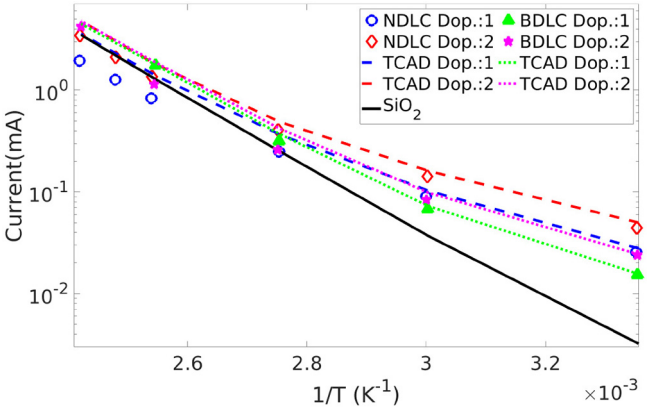


**FIGURE 1. Leakage currents of the reference diode measured for a reverse bias of 4kV at different ambient temperatures (symbols). The passivation DLC has been doped with Nitrogen (NDLC) and Boron (BDLC). Two doping levels for each type are reported, with "dop2" corresponding to an atomic concentration about 2 times larger than "dop1". The simulated temperature dependence of the leakage current as function of temperature for different DLC doping type and concentrations (dashed lines) is compared with experiments (symbols). The ideal case of a diode with a perfect insulator as passivation layer is also reported (solid line).**

OFF-state performance. Our attention is paid to the state-of-the-art large-area discrete diodes with JT using a negative or positive bevel JT and insulating passivation layer directly on top of the beveled silicon surface. In this way, a stable blocking capability is obtained without a significant reduction of the active area. For similar reason, the Diamond like-Carbon (DLC) has been applied on the passivation of planar JT of IGBT chips [3].The results of our work are applicable on both chips and discrete devices.

Recently, the semi-insulating properties of doped DLCs for improved blocking stability have been shown using experimentally calibrated TCAD model to explain the physical effects in the DLC layer and to show their influence on behavior of an industrial 4.5kV fast-recovery diode [4], [5]. In this work, the previously proposed TCAD model is extended to account for the temperature dependencies of the DLC transport to fully understand their influence on the $I_{OFF}$(T) curves. Our experiments show that the additional contribution to $I_{OFF}$(T) given by doped DLC passivation layer leads to an unusual deviation from the Arrhenius law. The modeling of silicon/DLC interface and charge transport in the DLC material have been deeply addressed to predict such effects. Beside the commercial fast recovery 4.5 kV diode a special MIS test structure has been used for rigorous calibration of parameters describing the transport of charged carriers through the silicon/DLC interface in the TCAD simulator. A nice agreement with the experiments was found and self-contained approach to the modeling of DLC passivation is reported for the first time.

## II. EXPERIMENTS AND SIMULATION APPROACH

Fig. 1 shows the experimental leakage currents versus temperature for the reference 4.5kV fast-recovery diode with different DLC recipes compared against the TCAD predictions reported in this work. The black solid line is the simulated $I_{OFF}$(T) when an ideal $SiO_2$ (perfect insulator with no additional conductive path) is used as a passivation layer. The expected Arrhenius law is found in this case in the whole range of T from 300 to 413 K. On the other hand, the use of differently doped DLC layers clearly show a significant deviation at low temperatures, where $I_{OFF}$ increases relative to the pn- junction contribution. This means that the conductivity of the DLC gives a relevant contribution to the overall $I_{OFF}$(T) and exhibits a weaker temperature dependence in comparison with silicon. Following [4], two doping types are compared (Boron and Nitrogen) with different doping concentrations. Experimental results clearly show that such kinds of doping in DLC deposition are of substitutional type. However, they are strongly compensated and accompanied by an increased defect density in the band gap [6], [7], [8]. In the [4], different atomic concentrations have been used to study the role of doping in the DLC conductivity and diode breakdown voltage. A significant increase of the blocking voltage was found for both doping types, leading to quite the same breakdown voltage. But the amount of required Nitrogen atomic concentration was 4-5 times larger than the Boron one. This can be ascribed to the role played by the passivation layer in releasing the surface electric field. As in this kind of diodes the onset of avalanche in silicon takes place below the surface along the bevel, the DLC provides an effect similar to the SIPOS field-plate structures [9], [10], [11]. The difference between Nitrogen and Boron arises from the role of the different type of free charges moving in the passivation layer, as explained with the numerical analysis reported in [4]. The doping configurations "dop1" and "dop2" in Fig. 1 correspond to atomic concentrations of each type giving quite the same improvements of blocking voltage. The largest doping levels are labeled "dop2" and correspond to the Nitrogen/Boron cases showing the maximum breakdown voltage. Thus, they can be considered as optimal conditions, while levels labeled "dop1" correspond to a halved atomic concentration for each type, respectively. A clear dependence of $I_{OFF}$ on the DLC doping level is visible. As the four cases correspond to different atomic concentrations, they are expected to give rise to different DLC conductivities. Moreover, when moving our analysis to larger temperatures, a difference in the highest $I_{OFF}$ value is also found among the experimental data what might play a role in the diode RBSOA. However, it is not straightforward to correlate the role of the DLC conductivity on the $I_{OFF}$(T) as will be discussed in the following.

### A. SIMULATION DECK OF THE LARGE-AREA DIODE

The device under test is a circular discrete diode as schematically represented in Fig. 2. The DLC is used as passivation layer directly in contact with the silicon bevel edge. The same device geometry was used with different DLC depositions for the investigation of the DLC. The 2D radial description has been used in the framework of the commercial TCAD tool [12] by assuming cylindrical coordinates. The

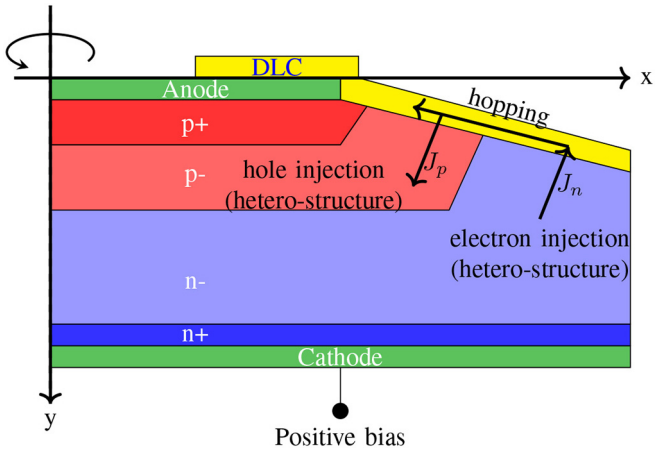


**FIGURE 2.** **Schematic representation of a power diode. Arrows in the DLC indicate the contributions of the current density along the bevel and across the DLC/Si heterostructure assuming the diode under reverse-bias condition. In the depleted region along the bevel, the DLC/Si structure contributes with hole injection in the region close to the anode, while electrons are injected from DLC to Silicon in the cathode termination. Thermionic injection is assumed at the DLC/Si interface, Poole-Frenkel-like hopping transport is assumed in the bulk DLC. The energy-band diagrams of the corresponding positions along the bevel are reported in Fig. 18.**

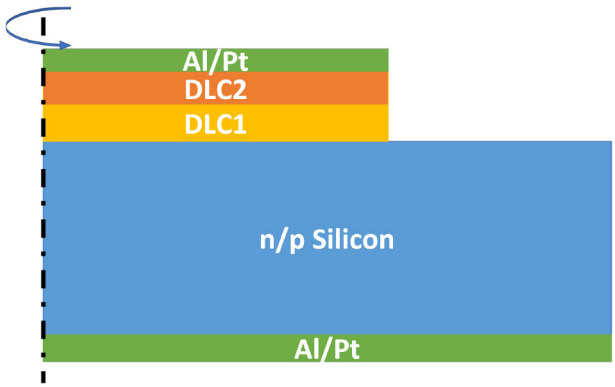


**FIGURE 3.** **Schematic view of the cross-section of a Metal-DLC-Si device. The structure is not in scale. TCAD simulations were carried out with a cylindrical symmetry in order to predict the current spreading in the Si substrate.**

fabricated diodes did not experience the usual shaping of the lifetime through irradiation, which would require electrothermal simulations to calibrate the deep energetic levels in the bandgap introduced by this process [13]. Thus, the drift-diffusion isothermal simulations have been carried out to investigate the OFF-state regime up to the avalanche breakdown. The doping profiles were received from the spreading resistance profiling. As far as the Silicon material is concerned, the Shockley-Read-Hall model for the thermal generation-recombination has been used with carrier lifetime fitted against the reverse leakage current curves at different temperatures when an undoped DLC was used as the passivation layer. The predicted $I_{OFF}$ values correspond to the simulated curve for an ideal $SiO_2$ passivation reported in Fig. 1. The Van Overstraeten model for the impact-ionization generation has been used for Silicon with default parameters. As far as the DLC passivation is concerned, the simulation setup has been prepared following [4] by assuming a two-layer DLC stack [14]. More specifically, a first interface layer of the DLC close to the silicon substrate (DLC1) has been realized in the TCAD structure assuming a relatively low carrier mobility. An interface layer thickness of about 70 nm has been identified using TEM images. The top layer (DLC2) is modeled by simply assuming a larger carrier mobility. Such assumption was made by comparing the measured DLC conductivity of Metal-Insulator-Semiconductor (MIS) test structures with current flowing vertically through the interlayer and top DLC and surface lateral structures of the industrial 4.5 kV diodes with current flowing mainly in the top layer. The lateral and vertical conductivities of the DLC layers have been experimentally observed to vary by a factor 100 independently of the type of DLC. We are mostly interested in the analysis of the diode OFF-state, a regime experiencing depletion both in the silicon area under the bevel and in the DLC top layer. The industrial diode structure has the DLC stack on top of both the n-type and p-type silicon regions. It is therefore important to correctly model the vertical Si/DLC interface in both cases. To this purpose, the MIS test structures have been characterized and used as a reference.

### *B. CHARACTERIZATION OF MIS STRUCTURES*

MIS structures featuring the DLC material as semi-insulating layer on top of silicon have been realized as illustrated in Fig. 3 [15], [16]. The experimental investigations have been extended here accounting for both p-type and n-type Si substrates to correlate the vertical features of the reverse bias condition of the MIS diode to the corresponding regions along the beveled interface of the real power diode from Fig. 2. Moreover, the top electrode has been realized with Aluminum or Platinum. Despite these two metals have very different work functions (4.28 eV for Al and 5.12-5.93 eV for Pt), the Al-DLC-Si and Pt-DLC-Si hetero-junctions do not exhibit relevant changes of the measured current-voltage curves. This can be ascribed to the large number of available conductive states inside the DLC energy gap close to the mid-gap as shown in [7] and [17], inducing a strong pinning of the Fermi-level $E_F$ at the mid-gap and a very small Schottky-barrier effect.

Fig. 4 shows the experimental J-V curves of the MIS structures with different substrate doping for both Boron- and Nitrogen-doped DLCs (the cases with maximum doping level are used here as reference). The doped DLC provides a strong increase of the current under forward bias if compared with the undoped case [15], [16]. Moreover, here we compare the forward-bias current curves of MIS structures with different doping types of the substrate (p-Si and n-Si).

No significant threshold voltage is observed in the two different substrate doping configurations and symmetric forward-bias curves have been found in any DLC doping

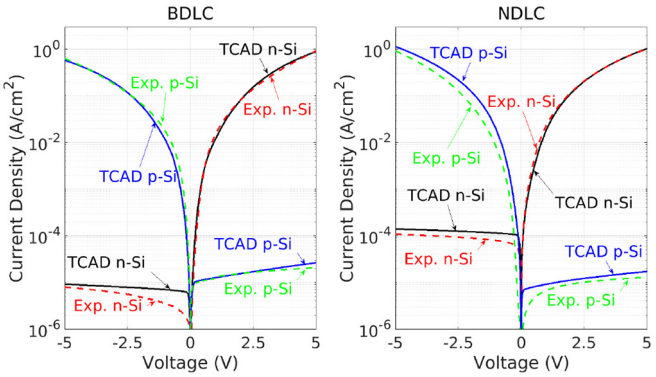


**FIGURE 4.** J-V curves of MIS structures at room temperature for different silicon substrates. Experiments (dashed lines) are compared with TCAD predictions (solid lines). (left): Boron-doped DLC. (right): Nitrogen-Doped DLC.

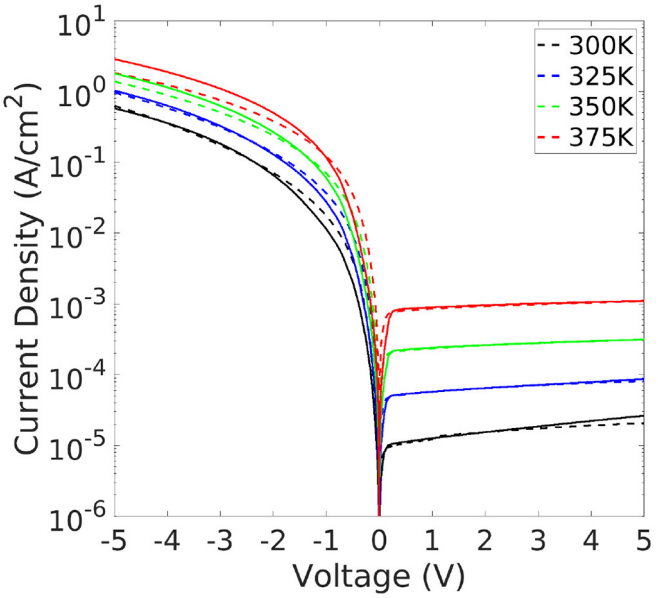


**FIGURE 5.** J-V curves of MIS structures with p-type silicon substrate and BDLC at different temperatures. Experiments (dashed lines) are compared with TCAD predictions (solid lines).

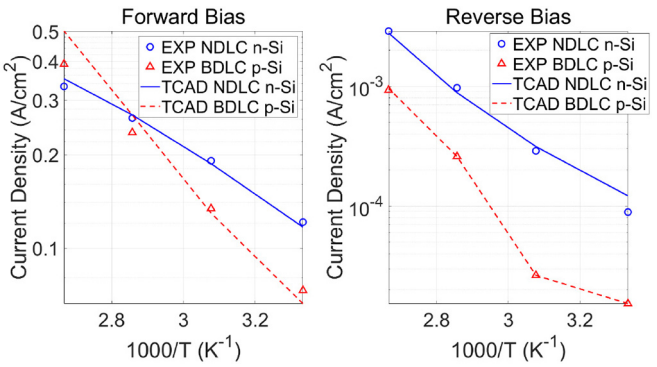


**FIGURE 6.** Current density extracted at Vbias = ± 2V as function of temperature. Experiments (symbols) are compared with TCAD predictions (lines).

configuration. The symmetry of the forward-bias curves, the absence of a threshold voltage and the previous check on the role of the top metal clearly suggest that the current contribution due to the electrons or holes as injected from the top metal is equivalent, independently of the differently doped silicon substrates at the bottom This can be ascribed to the expected effect of a high concentration of traps (hopping states) in the DLC bandgap leading to a relatively high leakage current. Under reverse bias condition, the MIS structures with different substrate doping show similar values of the saturation current confirming the assumption of Fermi-level pinning at the mid-gap. However, for the Boron doped case (BDLC), samples with p-doped Silicon show a slightly higher current when compared with the corresponding n-doped ones (Fig. 4 (a)). The opposite is true for Nitrogen-doped DLC (NDLC), with a more relevant asymmetry (Fig. 4 (b)) Thus, the latter features should be correlated to the DLC doping type and impurity concentrations.

To further distinguish the different transport regimes, the J-V characteristics were measured at 300, 325, 350 and 375 K. As an example, the measurements of the BDLC case on a p-type silicon are reported in Fig. 5, where the maximal current/voltage have been limited to safe operating regimes. Two qualitatively different temperature dependencies are observed in the forward and reverse regimes. As it is better visible when representing the current densities at a fixed bias versus temperature, Fig. 5 is redrawn to Fig. 6.

In the forward-bias regime, similar temperature dependencies have been found for different silicon-substrate doping (not shown). On the other hand, a slight difference between the NDLC and BDLC is found which can be ascribed to a different trap-to-trap hopping in the DLC due to a different trap concentration. Under reverse-bias, different saturation levels have been observed but with similar activation energies. This implies that, the Si/DLC interface must play a role along with the trap concentrations.

### C. MODELLING OF DLC BULK AND SI/DLC INTERFACE

The TCAD setup of the MIS structure has been implemented to account for all the physical effects relevant for the analysis of the temperature dependencies. Each physical model has been calibrated and validated against experiments.

The DLC charge transport has been addressed by using the drift-diffusion model assuming two symmetric Gaussian densities of states (G-DOSs) within the energy gap and the thermionic emission model at the Si-DLC interface for both electrons and holes [12].

A qualitative picture of the MIS band diagram is given in Fig. 7.

Each G-DOS can be written as:

$$\Gamma(E) = \frac{N_t}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(E-E_0)^2}{2\sigma^2}\right] \quad (1)$$

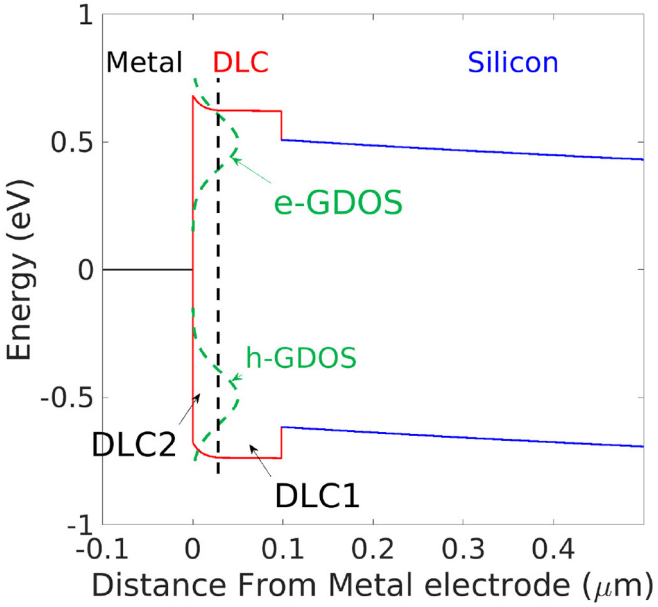


**FIGURE 7.** Energy band diagram of a MIS structure with Nitrogen doped DLC and n-type Silicon substrate.

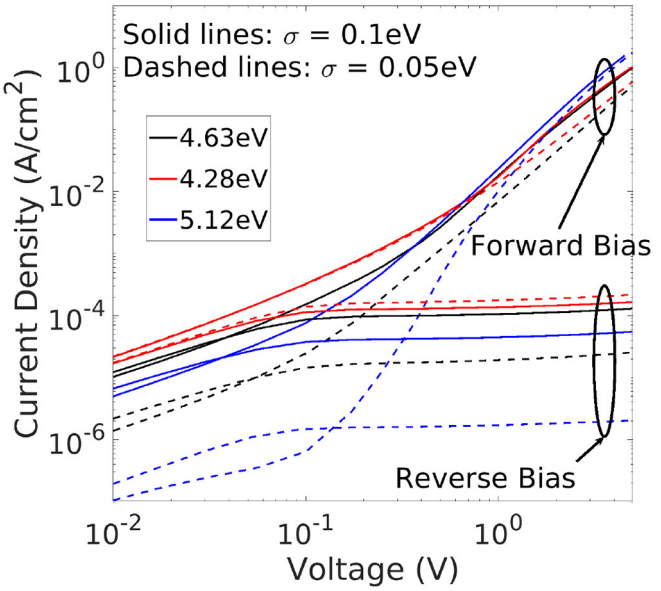


**FIGURE 8.** J-V curves of a MIS structure with Nitrogen doped DLC and n-type Silicon substrate for different values of the metal workfunction and two different values of the standard deviation of the G-DOS.

where $N_t$ is the concentration of hopping states, $\sigma$ the standard deviation and $E_0$ the energy shift with respect to the conduction band for electrons and valence band for holes. Electrons and holes experience the same $N_t$ and $\sigma$, while $E_{0,e} = -E_{0,h} = E_0$. The band gap between the peaks of the G-DOSs has been fixed close to the optical one (1eV). The devices with boron and nitrogen doped DLC have been modeled by assuming the corresponding acceptor- and donor-type doping. As the amount of active impurities was not experimentally available, the doping concentrations have been tuned against the asymmetries of the reverse-bias J-V curves (Fig. 4). The carrier concentration at the Metal/DLC interface is very high due to the contribution of the band tails, providing the desired lowering of the Schottky barrier effect. The impact of the value of the metal work-function on the MIS J-V curves is reported in Fig. 8 for two different G-DOS standard deviations. By using a broad G-DOS for both electrons and holes ($\sigma$ = 0.1eV), the J-V curves show a very limited dependence on the metal work-function due to partial $E_F$ pinning given by the band tails. However, to obtain symmetrical J-V curves as shown in it Fig. 4, it is still necessary to fix the metal work-function of the top electrode at $\varphi_M = \chi_{DLC} + E_{gDLC}/2$, where $\chi_{DLC}$ is the electron affinity of the DLC and $E_{gDLC}$ is the DLC energy gap , thus assuming a strong$E_F$ pinning at the mid-gap as reported in [7] and [17]. In this way, electrons and holes experience the same energy barrier at the metal-DLC interface and consequently give the same contribution to current both in positive and negative bias regimes. This is a key element to find symmetric forward-bias J-V curves with no threshold voltage. The effect of the band tails as shown in the literature, e.g., [7], [8], [17] can be modulated by acting on $\sigma$. Here $\sigma = 0.1$ eV has been assumed for all DLCs. $N_t$ can be tuned in a way to give the equivalent increase of free carriers, while keeping the symmetric J-V curves. As an increase of localized defects in the bandgap due to doping was experimentally verified through the $I_D/I_G$ ratio, with $I_D$ the intensity of the peak originated by disordered $sp^2$ carbon atoms and $I_G$ the intensity of the graphite peak [16], a larger $N_t$ is expected for the higher doping concentrations. The temperature dependence of the intrinsic carrier density is completely different from the usual one for semiconductors, because it depends on the form of the G-DOSs: by changing $\sigma$, we can modulate this dependence as shown in Fig. 9. By fixing $\sigma$ to 0.1 eV a very limited temperature dependence is obtained.

Following [4] and [15], a polarization effect has been accounted for in the TCAD setup through the ferroelectric model of the TCAD tool [12]. The most relevant parameter is the permanent polarization $P_r$ (the value of the polarization vector when the applied electric field is zero) which has been fitted against the capacitance peaks of the CV curves as shown in [4]. The frequency dependence of such peak has been modeled by tuning the time constant $\tau$ of the Debye equation as shown in [4]. Finally, an almost linear dependence of the polarization with the electric field has been obtained by fixing a low coercive field $F_c$ and a high saturation polarization $P_s$(see Table 1). The main expected role of the polarization is that of further reduced threshold voltage in the MIS forward-biased J-V curves of the MIS structure and that of changing the electrostatic effect of the top DLC layer. No specific role is expected as far as the temperature dependencies are concerned. The temperature dependence of the J-V curves has been deeply investigated through TCAD analysis. Under forward bias condition, a

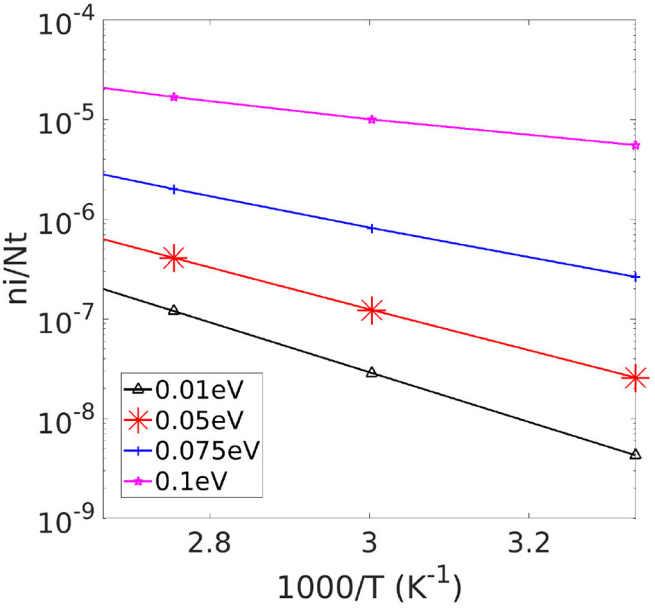


**FIGURE 9.** Temperature dependence of the intrinsic carrier density as a function of the reciprocal of temperature for different $\sigma$. The energy gap between the two G-DOSs is fixed at 1eV.

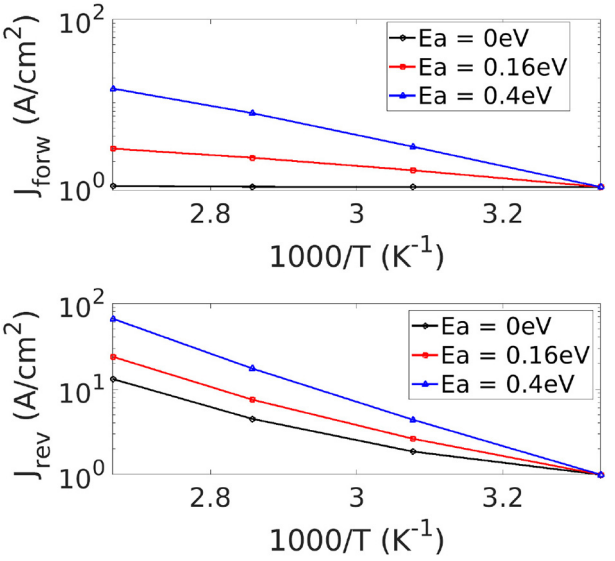


**FIGURE 10.** Normalized current density of MIS structure with NDLC and n-type Silicon extracted at V = ± 1V as function of the inverse temperature for different values of the Poole-Frenkel activation energy $E_a$ under (top) forward bias condition, (bottom) reverse bias condition.

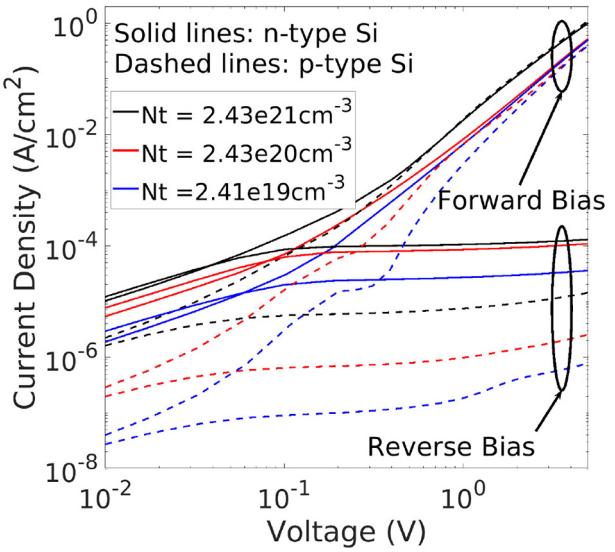


**FIGURE 11.** Simulated J-V curves of MIS structure with NDLC and different doping substrate.

Poole-Frenkel mobility has been adopted to reproduce the J-V trends within the full range of biase voltages [15]. It reads:

$$\mu = \mu_0 exp\left(-\frac{E_a}{k_B T}\right) exp\left(\frac{\beta\sqrt{E}}{T}\right) \tag{2}$$

where $\mu_0$ is the low-field mobility, $E_a$ is the activation energy of the hopping carriers and $\beta$ is a fitting parameter. The low-field mobility $\mu_0$ has been fitted against J-V curves at low-bias, where the ohmic regime is dominating ($J \propto V$) while$\beta$ has been calibrated against the J-V curves in the high-bias regime, where $J \propto V^n$ with $n > 2$ as reported in [15]. The same values have been used for electrons and holes. Different values have been used for differently doped DLC layers as reported in the Table 1. The activation energy $E_a$ has been chosen by comparing the J-V curves at different temperatures as extracted in Fig. 6. The values reported in Table 1 are in agreement with the activation energy extracted by linear fitting on Arrenhius plot at ±2V As expected, the temperature dependence of the forward current density is totally modulated by $E_a$ as shown in Fig. 10 (top). Viceversa, a negligible variation is found with $E_a$ under reverse-bias,when the DLC mobility plays a minor role (Fig. 10 (bottom)).

The reverse-bias curves are expected to be strongly affected by the DLC intrinsic carrier concentration: in Fig. 11, the simulated J-V curves are reported for different $N_t$ in the G-DOS. The figure clearly shows a significant dependence of the saturation current levels on $N_t$ and an undesired threshold voltage in the forward curve of the p-type MIS for the lowest magnitudes of $N_t$. As the temperature dependence of the J-V curves under reverse-bias conditions is key for the leakage current in the real power diode, we analyzed the behavior of the Si/DLC energy barrier in more details. We assumed a barrier height $\Delta E_c = \Delta E_v$ defined as $\Delta E_c = \chi_{Si} - \chi_{DLC}$. By changing the barrier height from 0.12 to 0.3 eV, the depletion region on the silicon side close to the interface is differently modulated (Fig. 12), giving rise to a correlated temperature dependence as shown in Fig. 13. In the following, the role of $\Delta E_c$ on the real 4.5 kV diode at elevated temperatures is also addressed (Fig. 20).

Finally, the difference in the saturation current between the MIS structures with differently doped substrates can be

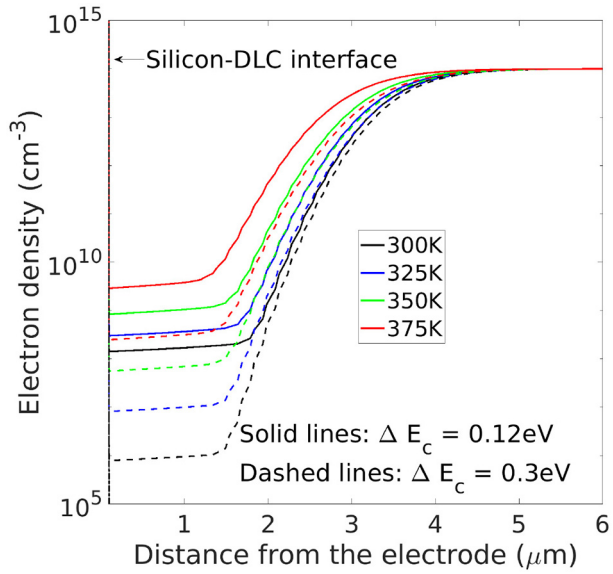


**FIGURE 12.** Simulated electron density at the DLC/Si interface for different temperature and different values of $\Delta E_C$ for a MIS structure with NDLC and n-type Silicon.

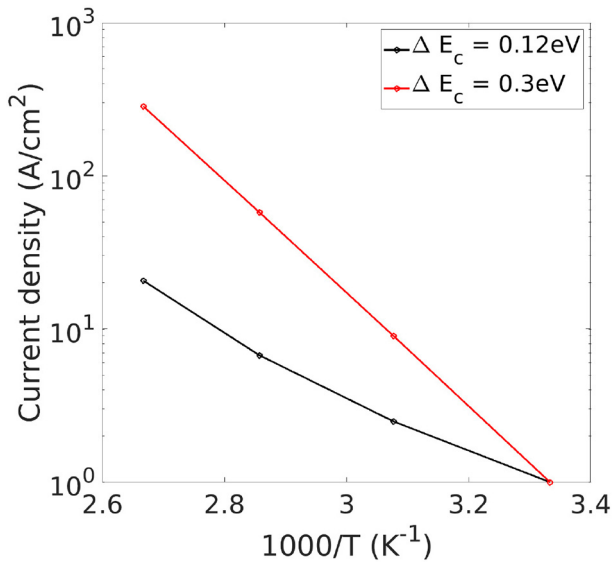


**FIGURE 13.** Simulated normalized current density under reverse bias condition at -5V for different temperature and different values of $\Delta E_C$ for a MIS structure with NDLC and n-type Silicon.

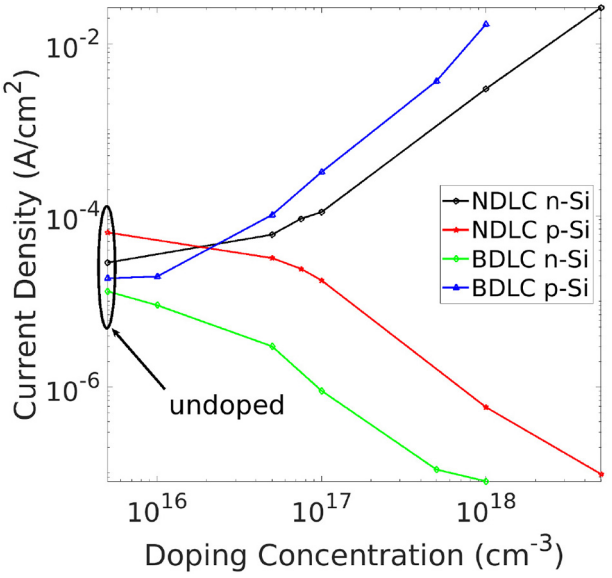


**FIGURE 14.** Simulated value of the saturation current density of MIS structure at room temperature under reverse bias condition for different doping concentrations extracted at ±5V.

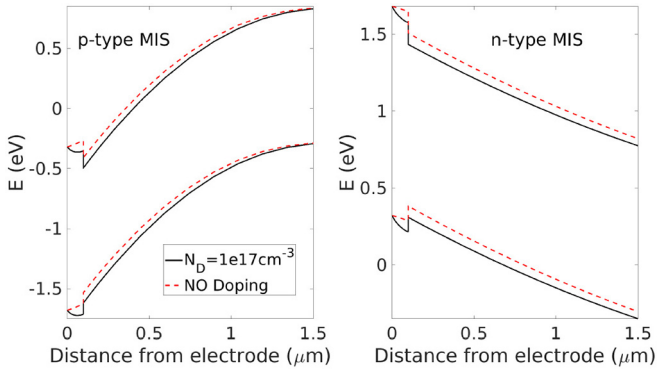


**FIGURE 15.** Band diagrams of MIS structure with or without doping. Left: p-type MIS, right: n-type MIS.

related to the doping concentrations. This is shown in Fig. 14, where the modulation of the saturation current asymmetry is obtained for different type of doping.

With the NDLC, the silicon bands are shifted toward lower energy reducing the difference between the conduction band and the Fermi level (not shown). If the silicon substrate is n-doped (Fig. 15 right) this results into a slightly higher electron concentration close to the Si/DLC interface what reduces the resistivity of the MIS structure. On the contrary, for a p-doped silicon the energy difference between the valence band and the Fermi level is increased with a consequent reduction of the hole concentration. Close to the Si/DLC interface, the silicon resistivity is then increased with the consequence of a lower reverse current density (Fig. 15 left). Symmetric considerations can be made for the BDLC. In Fig. 16 the band diagrams and the hole density corresponding to the MIS structure with BDLC at T = 300K shown in Fig. 5 are reported for three different bias conditions. Under forward bias (V = −2V) the applied voltage mainly drops across the DLC layer injecting holes in the DLC1 layer. Under reverse bias condition (V = +2V), the leakage current is limited by the depleted Si substrate. Figs. 4, 5, and 6 report the simulated data nicely compared with experiments.

All the parameter values used for the modeling of the conduction mechanism inside DLC and at Si/DLC interface are summarized in Table 1. The role of temperature is intrinsically accounted for through the implemented physically-based models [12]. All the reported values agree with available literature data [4], [7], [15], [17]. The G-DOS

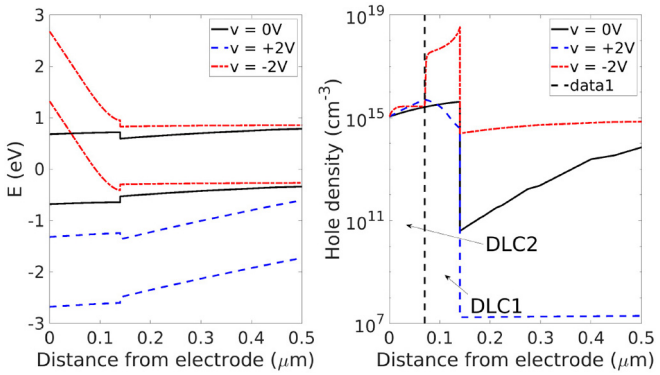


**FIGURE 16.** Band diagrams (left) and Hole density (right) corresponding to the MIS structure with BDLC shown in Fig. 5 at 300K for different value of the applied voltage.

**TABLE 1.** TCAD parameters set.

| Symbol | Quantity | NDLC | BDLC |
|---|---|---|---|
| $t_{DLC}$ | Measured total DLC thickness (nm) | 98 | 140 |
| $t_{DLC1}$ | DLC1 thickness (nm) | 70 | 70 |
| $t_{DLC2}$ | DLC2 thickness (nm) | 28 | 70 |
| $E_g$ | Energy gap (eV) | 1.36 | 1.36 |
| $\chi$ | Electron Affinity (eV) | 3.95 | 3.95 |
| $\Phi_M$ | Metal Work function (eV) | 4.63 | 4.63 |
| $N_t$ | Number of hopping states ($cm^{-3}$) | 2.43e21 | 2e20 |
| $E_{0,e}$ | Electron G-DOS energy position (eV) | 0.18 | 0.18 |
| $\sigma$ | Standard deviation (eV) | 0.1 | 0.1 |
| $N_D$ | Doping concentration ($cm^{-3}$) | 1e17 | 1e16 |
| $\mu_{0,DLC1}$ | DLC1 Low-field mobility ($cm^2/Vs$) | 3.07e-4 | 0.01 |
| $\mu_{0,DLC2}$ | DLC2 Low-field mobility ($cm^2/Vs$) | 3.07e-2 | 1 |
| $E_a$ | Poole-Frenkel activation energy (eV) | 0.16 | 0.23 |
| $\beta$ | Fitting parameter ($Kcm^{0.5}/V^{0.5}$) | 1.2 | 1.7 |
| $\epsilon_r$ | Relative dielectric constant | 4 | 5.4 |
| $P_s$ | Saturation Polarization ($C/cm^2$) | 1.5e-6 | 1.5e-6 |
| $P_r$ | Permanent Polarization ($C/cm^2$) | 3e-8 | 6e-8 |
| $F_c$ | Coercive Field (kV/cm) | 1e4 | 1e4 |
| $\tau$ | Relaxion time (s) | 1.7e-5 | 3.1e-5 |

parameters have been deduced by the comparison against experiments discussed above.

### D. FINAL VALIDATION AGAINST DIODE EXPERIMENTS

The 4.5kV diode under test is schematically shown in Fig. 2. A final validation of the DLC model has been carried out by comparing the TCAD predictions with the measured I-V curves of the reverse-biased diode at room temperature for the four differently doped passivations. A nice agreement has been found up to the onset of avalanche regime Fig. 17.

The band diagrams of the Si-DLC vertical structure along the bevel and the corresponding MIS devices are reported in Fig. 18. In the p- region (Fig. 18 (a), silicon is fully depleted at the surface and the equivalent MIS structure is reverse-biased Fig. 18 (c): holes are injected from DLC into silicon, the leakage current is limited by the reverse-biased regime. In the n-doped region Fig. 18 (b), silicon is fully depleted at the surface and the equivalent MIS structure is reverse-biased Fig. 18 (d): electrons are injected from DLC

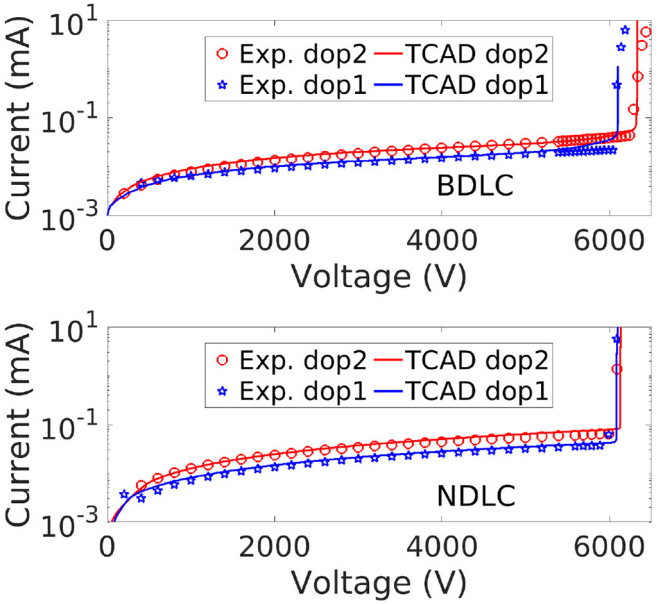


**FIGURE 17.** I-V curves of the power diode under reverse bias condition for different DLC passivation layer (T = 300K).

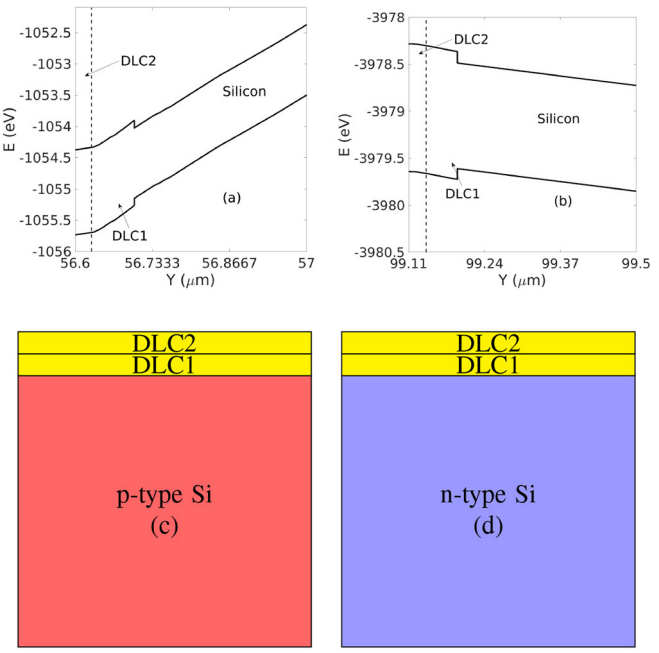


**FIGURE 18.** Band plot of the Si-DLC vertical structure along the bevel of the power diode at different x-positions. (a) p-/DLC interface in the space charge region (b) n-/DLC interface into the space charge region. (c) and (d): MIS structures corresponding to the band diagrams in the p- and n-region respectively. Data extracted at V = 4000V and T = 300K. A Nitrogen doped DLC has been used.

into silicon, but the leakage current is limited by the reverse-biased regime. When moving to the quasi-neutral regions at the p+ or at the bevel edge, silicon is no more depleted at the surface, but the equivalent MIS structure is still slightly reverse-biased (at the anode side) or switched off. Thus, $I_{OFF}$ depends mainly on the intrinsic carrier density and the

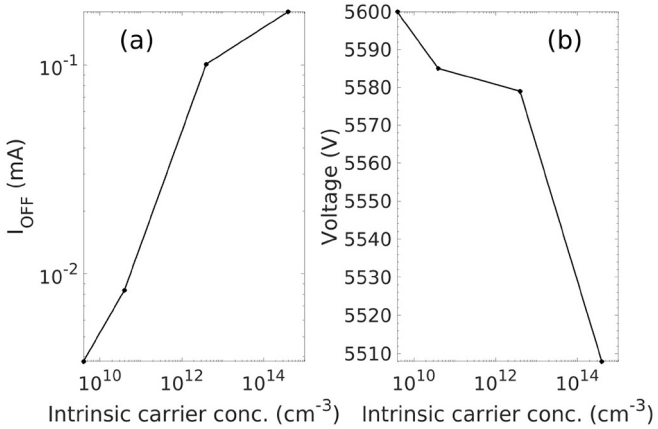


**FIGURE 19.** Simulated leakage current ($I_{OFF}$) (a) and breakdown voltage (b) at room temperature as function of the intrinsic carrier density of the passivation layer. An undoped DLC has been used.

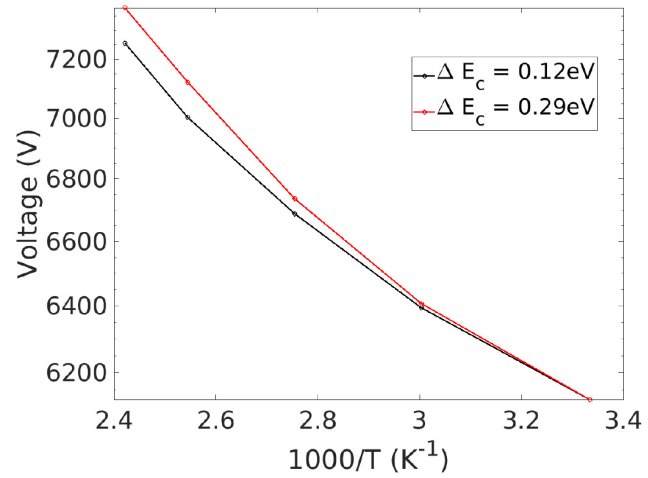


**FIGURE 20.** Simulated value of the diode breakdown voltage as function of the reciprocal ambient temperature for two different value of $\Delta E_C$.

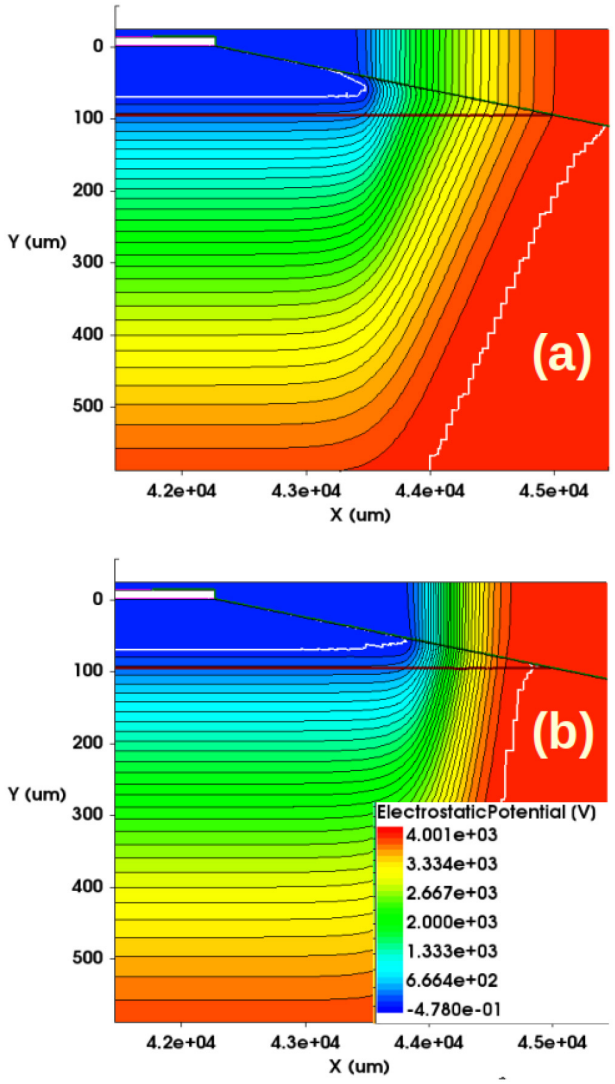


**FIGURE 21.** 2-D potential contour plots of the diode JT extracted at V = 4000V under reverse bias condition. (a) NDLC at 300K, (b) NDLC at 413K.

doping concentration of the DLC as in the reverse biased MIS devices. At room temperature, the $I_{OFF}$ can be tuned by acting on the G-DOS without significant changes in the breakdown voltage as shown in Fig. 19.

In Figs. 21 and 22, the 2-D contour plots of the electrostatic potential at the junction termination of the 4.5kV diode are reported (white lines correspond to the depletion limits of the pn-junction).

The avalanche onset is located at the anode-side edge of the depletion region along the p-n junction, where the peak of the electric field is observed (Fig. 23).

At room temperature, the depletion region width at the Si/DLC interface is strongly influenced by the doping type inside the DLC. When the NDLC is used, silicon at the interface is more depleted in the p- region since positive ions in the DLC improve the p-doped silicon depletion underneath. Symmetric considerations can be made for electrons in the silicon n-region when the passivation layer a BDLC. At T = 413K (Figs. 21 (b) and 22 (b)) the doping effects are compensated by the thermal generation in silicon. Thus, the depletion region shows the same width independently of the kind of passivation layer used. Since the electrostatic effects induced by the DLC passivation become negligible, the electric field profile along the bevel is expected to become equivalent to that of a diode with a purely-insulating passivation layer. In Fig. 20 the temperature dependence of the breakdown voltage is reported for two different values of the Si/DLC energy barrier $\Delta E_c$. As discussed for the room temperature above, the width of the depletion region is determined by the doping concentration and then the role of $\Delta E_c$ is negligible. At higher temperatures, the doping effects disappear. A high $\Delta E_c$ leads to slightly more depleted silicon close to the Si/DLC interface (as shown in the analysis of the MIS device) leading to a small increase of the breakdown voltage. The proposed TCAD approach accounts fully for the role played by charge carriers and then nicely compares against experiments providing a full validation of the approach.

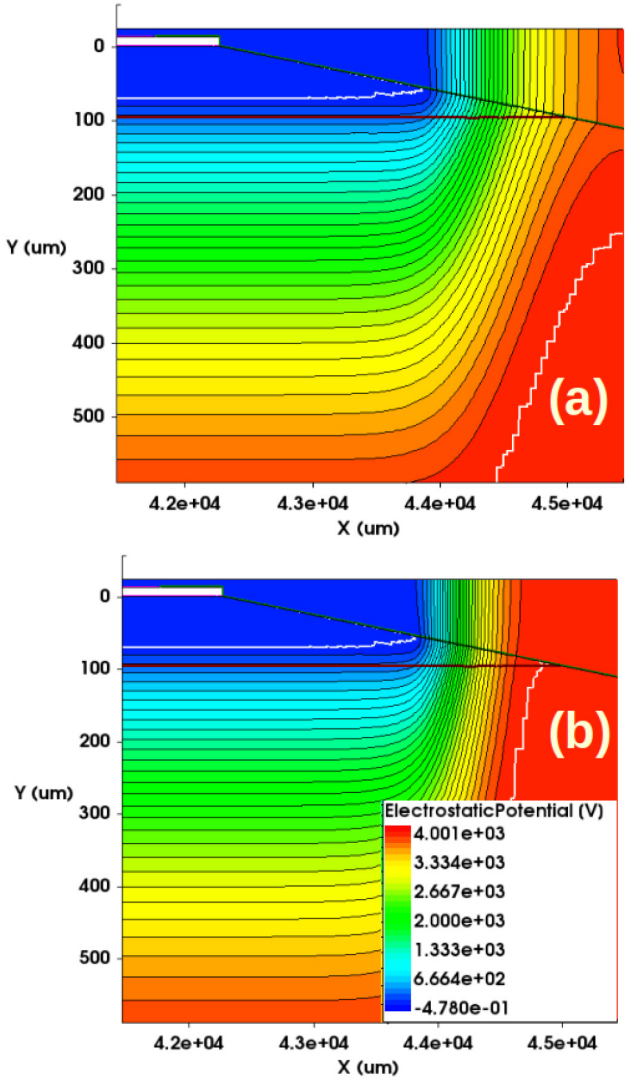


**FIGURE 22.** 2-D potential contour plots of the diode JT extracted at V = 4000V under reverse bias condition. (a) BDLC at 300K, (b) BDLC at 413K.

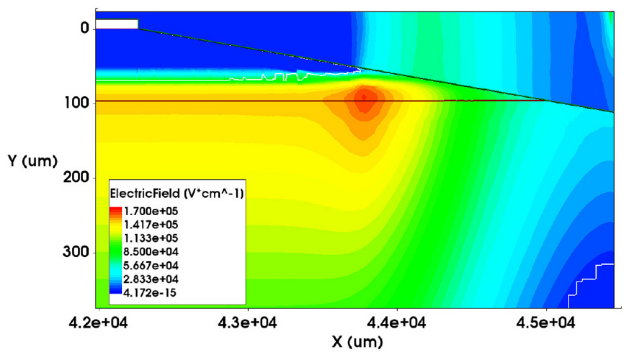


**FIGURE 23.** 2-D electric field contour plot of the diode JT extracted at V = 4000V under reverse bias condition. BDLC at 300K.

## III. CONCLUSION

Using specially designed MIS test structures with different substrate doping ad composition of the DLC layers, as well as by performing measurements on industrial 4.5kV discrete diodes in a wide range of temperatures, a detailed analysis of the DLC conduction mechanisms and electrostatic properties has been developed. The results achieved in this work give the possibility to predict the leakage current of a 4.5kV diode for differently doped DLC layers and different temperatures up to the $T_{jmax}$ of 413K. The proposed TCAD setup correctly predicts the reverse-bias SOA of the device under investigation, by accounting for the DLC-coated structure material and interface properties. Such approach is shown to be a useful tool for the design of arbitrary DLC passivation.

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