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A. N. Tallarico *et al*. " TCAD Modeling of the Dynamic Hysteresis Under Fast Sweeping Characterization in p-GaN Gate HEMTs" in *IEEE Transactions on Electron Devices,* Early Access, December 2021, DOI: 10.1109/TED.2021.3134928.

TCAD Modeling of the Dynamic V_{TH} Hysteresis under Fast Sweeping Characterization in p-GaN Gate HEMTs

A. N. Tallarico, M. Millesimo, B. Bakeroot, M. Borga, N. Posthuma, S. Decoutere, E. Sangiorgi, *Fellow, IEEE,* and C. Fiegna

***Abstract*—TCAD modeling of the dynamic threshold voltage shift (hysteresis) occurring under fast sweeping characterization in Schottky-type p-GaN gate HEMTs is reported, to the best of our knowledge, for the first time. Dynamic V_{TH} hysteresis has been first experimentally characterized under different sweeping times, temperatures, and AlGaN barrier configurations. Then, TCAD simulations have been carried out, reproducing the experimental evidences and understanding the microscopic mechanisms responsible for such effect. In particular, nonlocal tunneling models implemented in Sentaurus TCAD, defined at the gate Schottky contact and assisted by traps in the AlGaN barrier layer, have been adopted and properly tuned against experiments. Results show that the dynamic V_{TH} hysteresis is mainly caused by the time-dependent hole charging/discharging processes in the floating p-GaN layer, which are governed by the Schottky and AlGaN barrier leakage current components.**

***Index Terms*— p-GaN gate HEMT, dynamic V_{TH} hysteresis, TCAD modeling, tunneling model, gate leakage, charge trapping.**

I. Introduction

HIGH-electron-mobility transistors (HEMTs) are promising candidates for the next generation of smart, high frequency and high power density applications [1-3]. Among various GaN-based technologies, the most commercialized normally-OFF architecture features a metal/p-GaN/AlGaN/GaN gate stack grown, through a transition layer, on a low-cost and large-size silicon substrate, as it offers a good trade-off between performance, reliability and cost [4, 5]. However, the complex gate stack represents critical performance and reliability concerns because of the floating p-GaN layer with a mobile charge that is modulated by means of carrier injection, tunneling and trapping processes, causing the alteration, recoverable or permanent, of the electrical characteristics of the transistor.

In the last years, a significant effort has been devoted to the analysis of the p-GaN gate reliability by means of both static and dynamic stress/characterization tests [6-10]. In this paper, large emphasis is placed on the dynamic threshold voltage shift (ΔV_{TH}) phenomenon observed under fast transient and/or pulsed stress/characterization.

Tang et al. [11] reported about an electron injection and trapping in the gate stack under pulse forward gate bias, causing positive ΔV_{TH}, whereas the hole injection in the GaN channel results in an increase of gate leakage.

In [12] a technique has been developed to evaluate the transient V_{TH} behavior, in a time window from 10 µs to 100 s, under positive gate bias stress, proposing the occurrence of: i) electron trapping at the AlGaN/GaN interface; ii) hole accumulation at the p-GaN/AlGaN interface; iii) hole trapping in the AlGaN barrier; iv) hole depletion of the p-GaN layer.

He et al. [13] reported a positive ΔV_{TH} under fast-dynamic-forward gate stress and a monotonous frequency dependency from 10 Hz to 1 MHz, attributed to charge storage/release in/from the floating p-GaN or AlGaN barrier layer.

Similar dynamic V_{TH} drift related processes have been reported also in the case of p-GaN HEMT subjected to high pulse drain voltages [14-16], i.e. charge storage mechanisms in the floating p-GaN layer, proposing also a Spice-compatible equivalent-circuit model [17].

Finally, in [18] a dynamic V_{TH} hysteresis/instability under fast sweeping characterization has been reported. In particular, as the IdVg sweeping time decreases from 5 ms to 5 µs the fully recoverable V_{TH} hysteresis deteriorates from 22.6 mV to 1.76 V, suggesting an ionization process of the acceptor-like traps in the p-GaN depletion region.

In this paper, the microscopic mechanisms causing the dynamic V_{TH} hysteresis occurring under fast sweeping characterization

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Part of this work is funded by iRel40. iRel40 is a European co-funded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement No 876659. The funding of the project comes from the Horizon 2020 research programme and participating countries. National funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, the Netherlands, Slovakia, Spain, Sweden, and Turkey.

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TABLE I
ALGAN BARRIER PROPERTIES AND ADOPTED NONLOCAL TUNNELING MODEL PARAMETERS FOR DUTS

PROCESS	AlGaN Barrier Layer			NonLocal Trap Assisted Tunneling Model			
	Al content (%)	Thickness (nm)	Trap Conc. ($cm^{-3}eV^{-1}$)	$m_{TE} = m_{TH}$	V_T (μm^3)	S (one)	ħω (eV)
1A	25	12.5	$2.7 \cdot 10^{18}$	0.2	$4 \cdot 10^{-5}$	1	0.175
2A	25	Thicker than 1A	$2.7 \cdot 10^{18}$	0.14	$4 \cdot 10^{-5}$	1	0.175
2B	Lower than 1A/2A	Same as 2A	$2.45 \cdot 10^{18}$	0.14	$4 \cdot 10^{-5}$	1	0.175
3C	Lower than 2B	Thicker than 2A/2B	$2 \cdot 10^{18}$	0.11	$4 \cdot 10^{-5}$	1	0.175
3D	Lower than 3C	Same as 3C	$1.8 \cdot 10^{18}$	0.11	$4 \cdot 10^{-5}$	1	0.175

have been modeled, for the first time, by means of physics-based TCAD simulations, revealing the time-dependent charging/discharging processes of the floating p-GaN layer as the root cause for such effect.

II. DUT AND CHARACTERIZATION TECHNIQUE

Devices under test (DUTs) have been grown by metalorganic chemical vapor deposition (MOCVD) on 200-mm GaN-on-Si substrate by *imec*. The epi-stack consists of 200 nm AlN nucleation layer, 1.65 µm (Al)GaN superlattice layer, 1 µm C-doped GaN back barrier, 400 nm undoped GaN channel layer, different AlGaN barrier configurations in terms of thickness and Aluminum (Al) content, 80 nm Mg-doped p-GaN layer with a dopant concentration of ~ $3 \cdot 10^{19}$ cm^{-3}. Additional process details can be found in [19]. The reference device (namely process 1A) features a 12.5 nm thick AlGaN barrier with 25% of Al content. Then, moving from 1 to 3 indicates thicker AlGaN, whereas from A to D implies lower Al% (see Table I).

The fast sweeping characterization has been performed with a Keysight B1530A Waveform Generator/ Fast Measurement Unit (WGFMU). To measure the dynamic V_{TH} hysteresis, two fast gate voltage ramps, from 0 V to 6 V and back to 0 V without dead times, have been applied in sequence with 50 mV constant drain voltage, and source shorted with substrate to ground. The sweeping times of the two voltage ramps, namely t_{RISE} and t_{FALL}, are set to the same value, and range from 2 µs to 20 µs. The choice of 6 V as maximum gate voltage (V_G) has been determined by considering the results obtained in [18], where a V_G-dependency of the V_{TH} hysteresis has been observed up to 6 V, showing the maximum V_{TH} shift and a saturation for higher values. Moreover, V_G = 6 V is close to the maximum applicable gate voltage for the p-GaN gate technology currently available on the market.

III. TCAD MODELS FOR LEAKAGE CURRENTS

Sentaurus TCAD [20] has been adopted to simulate the dynamic threshold voltage hysteresis and its dependency on the sweeping time, temperature and AlGaN barrier configuration.

As reported in [21], the threshold voltage of a p-GaN gate HEMT is strongly influenced by the gate leakage, more in detail, by the balance between the metal to p-GaN Schottky diode and the p-GaN/AlGaN/GaN (PiN) diode leakage components. The dominating diode, featuring the lowest leakage current, establishes how much gate current flows and the charging state of the floating p-GaN layer, determining the V_{TH} value. Consequently, accounting for accurate gate leakage mechanisms in the simulation is of paramount importance. Therefore, in addition to thermionic emission contribution, nonlocal tunneling models [20] have been adopted and defined for both diodes.

In particular, hole tunneling from metal to p-GaN valence band is modeled at the Schottky gate contact (Fig. 1), assuming a single-band parabolic band structure, using a WKB-based model for the tunneling probability. The effective hole tunneling mass has been tuned by fitting the measured gate leakage in the V_G-range where the reverse Schottky diode is dominant, i.e. V_G > ~ 3 V in the case of our devices.

In the case of p-GaN/AlGaN/GaN diode, a nonlocal trap assisted tunneling has been modeled inside the AlGaN barrier. In particular, acceptor traps have been placed in the AlGaN barrier and coupled to nearby interfaces by tunneling. The latter, as shown in Fig. 1, is allowed for both electrons and holes coming from 2DEG (two-dimensional electron gas) and 2DHG (two-dimensional hole gas), respectively, and includes both inelastic phonon-assisted and elastic processes.

The acceptor traps, with a concentration of ~ 10^{18} $cm^{-3}eV^{-1}$ (see Table I), have been uniformly distributed in both energy and spatial domains. In particular, the energy window shown in Fig. 1 by means of dashed line has been adopted for the AlGaN barrier. It is worth noting that, such density and distribution might not be realistic, but it is needed to accurately reproduce the experimental V_{TH} hysteresis on devices featuring different AlGaN barrier variants and under different thermal and electrical conditions. One possible hypothesis is that threading dislocations are the root cause for the tunneling through the AlGaN barrier, as reported in the case of AlGaN/GaN heterostructures grown on Si-substrate by means of MOVCD [22-24]. In our case, such a possible effect is being modeled through tunneling assisted by traps, which are discretized in space and energy, hence the model parameters reported in table I might be misaligned with typical values reported in the

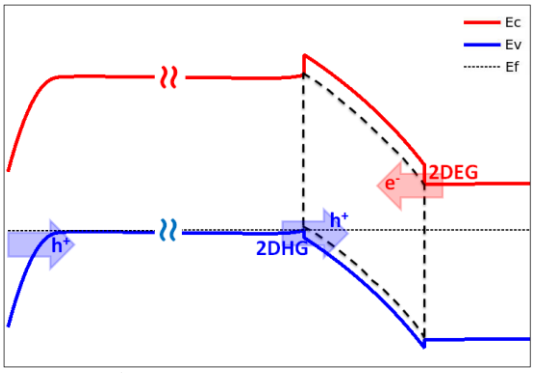

Fig. 1. Schematic of band diagram at V_G = 0 V, showing the tunneling component and the spatial and energy window of the acceptor traps placed in the AlGaN barrier layer (dashed line).

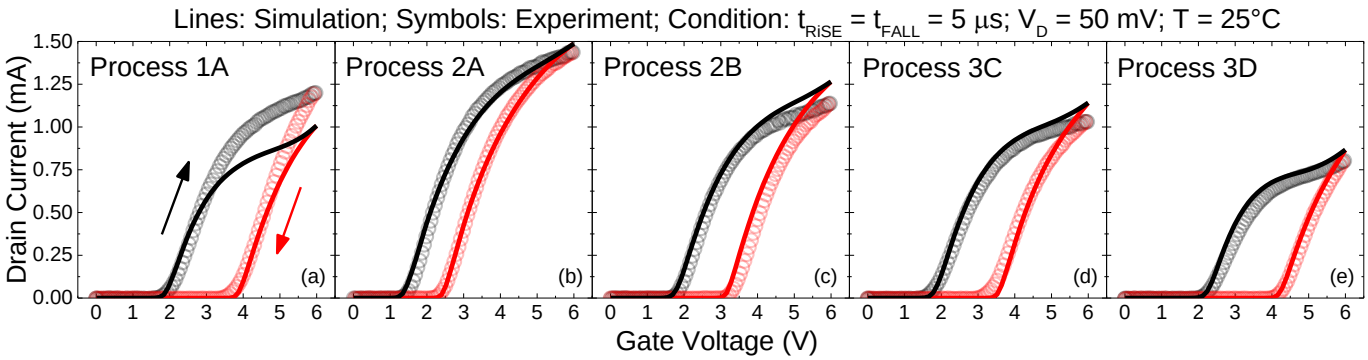

Fig. 2. Measured (symbols) and simulated (lines) IdVg transfer characteristics with related V_{TH} hysteresis under fast sweeping characterization (from 0 V to 6 V in 5 µs) on devices featuring different AlGaN barrier configurations in terms of thickness and Al content. Process 1A features a 12.5 nm thick AlGaN barrier with Al = 25%. Moving from 1 to 3 indicates thicker AlGaN, whereas from A to D implies lower Al%.

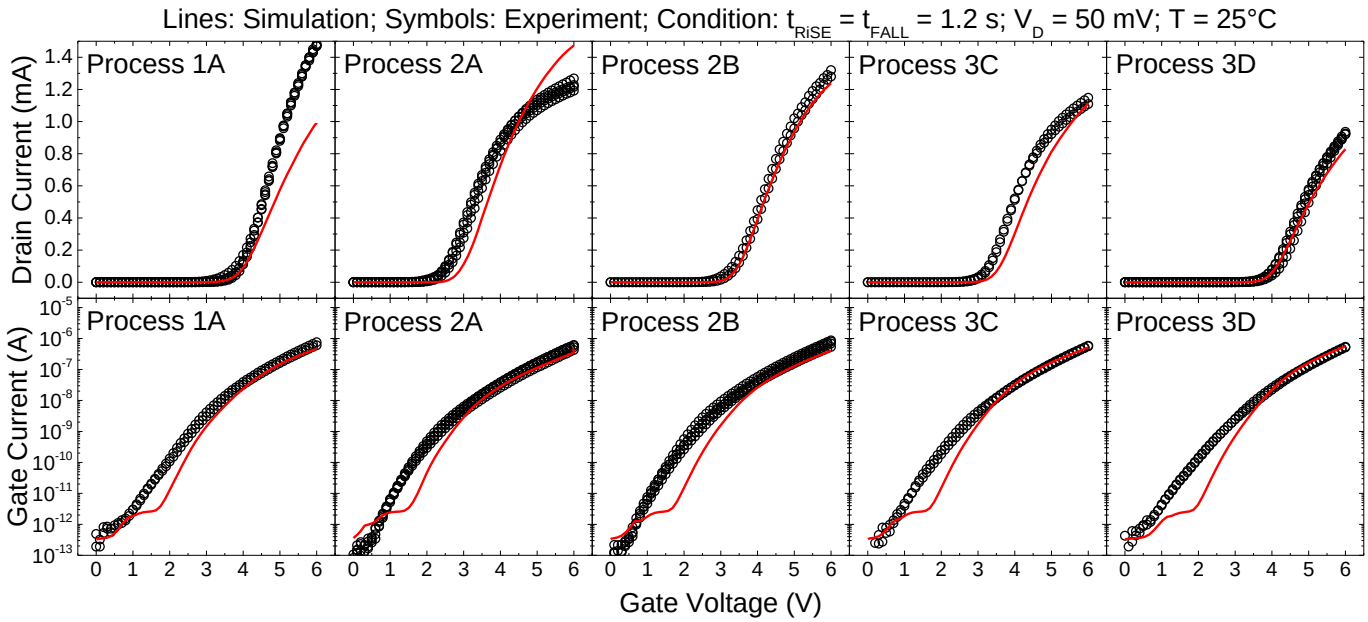

Fig. 3. Measured (symbols) and simulated (lines) IdVg transfer characteristics (top) and gate leakage characteristics (bottom) under slow sweeping characterization (from 0 V to 6 V in 1.2 s) on devices featuring different AlGaN barrier configurations in terms of thickness and Al content. Process 1A features a 12.5 nm thick AlGaN barrier with Al = 25%. Moving from 1 to 3 indicates thicker AlGaN, whereas from A to D implies lower Al%.

literature.

Finally, the effective electron (m_{te}) and hole (m_{th}) tunneling masses, the interaction volume of the trap (V_T), the Huang-Rhys factor (S), and the energy of the phonons involved in the transition ($\hbar\omega$) have been properly tuned, and summarized in Table I, to reproduce the dynamic V_{TH} hysteresis and the transfer characteristics under slow and fast transient characterization.

IV. Results and Discussion

A. *Experiments vs TCAD Simulations*

Fig. 2 shows the measured (symbols) and simulated (lines) IdVg characteristics under fast (5 µs) sweeping characterization on devices featuring different AlGaN barrier configurations. TCAD simulations accurately reproduce IdVg and related V_{TH} hysteresis on different devices. Moreover, it is observed that the amount of dynamic V_{TH} hysteresis strongly depends on the choice of the AlGaN barrier, since it plays a role in the leakage balance between the Schottky and the PiN (AlGaN barrier related) diodes. The mechanisms behind these observations will be discussed in the subsections *IV.B* and *IV.C*.

Fig. 3 shows the measured (symbols) and simulated (lines) IdVg (top) and IgVg (bottom) characteristics under slow (1.2 s) sweeping characterization on devices featuring different AlGaN barrier configurations, highlighting a good matching. The different ON-resistance values observed in the case of highest Al content (process 1A and 2A) might be ascribed to the access regions, probably due to a different concentration or energy distribution of donor traps located at the AlGaN/passivation interface. Additional calibration of the passivation related interfaces is possible, but was not considered here as it does not add to the discussion at hand.

When a relatively slow sweeping characterization is adopted no V_{TH} hysteresis is observed, as reported in [18] for sweeping times longer than 1 ms. Note, the difference between simulated and measured gate leakage characteristic, for $V_G \leq \sim 2.5$ V, is attributed to an edge leakage component observed in real devices up to $V_G \sim V_{TH}$ (i.e. up to 2DEG formation), which is not easy to account for in a 2D-simulation. In particular, by characterizing devices with different gate area, the related

leakage does not scale with the area for $V_G < 2$ V.

TCAD simulations have been performed also with different sweeping times (2, 5, 10, and 20 µs) to verify its effect on the V_{TH} hysteresis, as shown in Fig. 4 and widely reported in [18]. As noticeable, such feature is accurately reproduced by simulation. Furthermore, in addition to amount of dynamic ΔV_{TH}, also the different drain current dynamic, observed by ramping up V_G (black circles) with different sweeping times, is nicely reproduced.

Finally, the temperature dependency of the dynamic V_{TH} hysteresis has been investigated by adopting a 5 µs sweeping time from 0 to 6 V. It is worth reminding that the fast characterization is symmetric in terms of sweeping times, i.e. $t_{RISE} = t_{FALL} = 5$ µs in this case. A negligible temperature dependency is observed in Fig. 5 for both experimental and simulation analyses, although, as well known, the threshold voltage and the gate leakage are two temperature-dependent transistor parameters. However, the V_{TH} hysteresis, hence the charging/discharging state of the floating p-GaN layer (discussed in the next subsection), does not depend on the absolute value of the gate current but on the relative balance between the Schottky and PiN diode leakage components. If the temperature dependency of such two components is similar, their balance is unaffected. Overall, the dynamic V_{TH} hysteresis and its dependencies on the sweeping time, temperature and device process have been reported and reproduced by TCAD simulations, proving a quite accurate TCAD modeling.

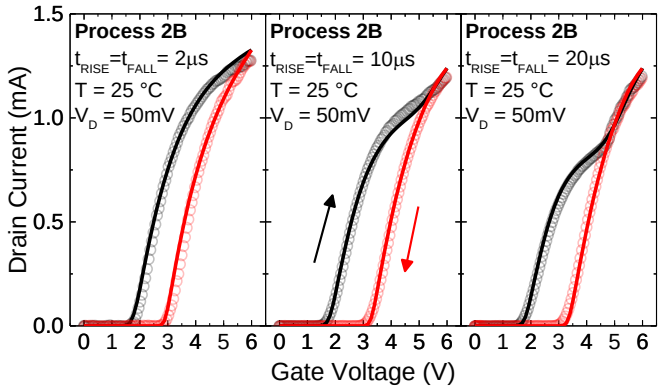

Fig. 4. Measured (symbols) and simulated (lines) IdVg transfer characteristics with related V_{TH} hysteresis under different fast sweeping characterization in the case of devices featuring Process 2B.

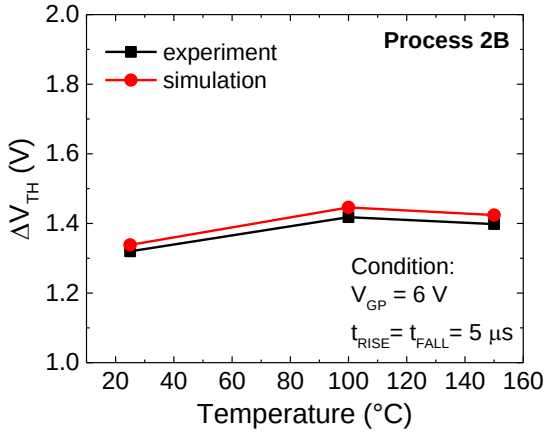

Fig. 5. Negligible experimental (squares) and simulated (circles) temperature dependency of the dynamic V_{TH} hysteresis evaluated with a sweeping time of 5 µs from 0 V to 6 V, in the case of devices featuring Process 2B.

B. Theoretical considerations

The question arises whether the measured and/or simulated V_{TH} hysteresis effects are due to charging of the p-GaN layer and/or trapping of charges. The charging (or discharging) of such layer occurs because it is a (semi-)floating node.

On the one hand, holes are provided by the metal contact, acting as a source for holes for both the (quasi-)neutral region in the p-GaN layer and for the 2DHG at the p-GaN/AlGaN interface. On the other hand, holes are lost inevitably once the gate voltage is high, since this (slightly) forward biases the p-GaN/AlGaN/2DEG "PiN" diode, whereby holes are emitted into the AlGaN and/or electrons are emitted into the p-GaN (upon which they recombine with the holes in the p-GaN and therefore also change the number of holes in this layer). Note that the necessary condition for these mechanisms is that the p-GaN layer is not completely depleted. This is the case in the DUTs as the p-GaN is highly doped and thus, the depletion region width coming from the Schottky-metal/p-GaN interface never reaches the 2DHG (even under high forward gate bias).

As thought experiment, let us assume that the Schottky contact is ideal, i.e. there is no hole supply; and that the AlGaN barrier blocks all hole loss. Then, the p-GaN gate structure should work flawlessly: the charge that is needed to modulate the 2DEG is fully provided by the accumulation of holes in the 2DHG: that is $\Delta\sigma_{2DHG} = \Delta\sigma_{2DEG}$(see also discussion in [21]). Since the holes are the majority carriers in the p-GaN, the supply to the accumulation layer is fast (in the order of the dielectric relaxation time of GaN) and the carriers originate from the depletion layer at the Schottky contact. As such, the p-GaN gate structure works as a perfect charge pump (or capacitive voltage divider): the holes are 'pumped' from the depletion layer to the 2DHG and back in a very fast manner. Yet this ideal situation is disturbed by leakage currents both through the AlGaN barrier and at the Schottky contact. As such, the voltage dividing properties will alter, and the 'internal' p-GaN electrostatic potential will depend on how fast holes are supplied, or leaking away, which is governed by particular leakage mechanisms that also change depending on the gate bias – as will be exemplified in the next subsection.

Another mechanism that might cause V_{TH} hysteresis or shifts is the trapping of charges either in the AlGaN barrier or at its interfaces. One can easily assess the value of the V_{TH} hysteresis or shift as it is given by [25]:

$$\Delta V_{TH} = -\frac{1}{C_b}\left[\frac{1}{t_b}\int_0^{t_b} x\rho(x)dx\right],$$

where t_b and C_b are the thickness and the capacitance value of the AlGaN barrier, respectively; and $\rho(x)$ is the trapped charge density in the AlGaN barrier. If one assumes, for the sake of simplicity, a constant distribution ($\rho(x) = \rho_b$) of trapped charge as a function of the depth x, then $\Delta V_{TH} = -t_b\rho_b/2C_b$. The observed V_{TH} hysteresis values would require a trapped charge density as large as ~ 9×10^{18}cm^{-3}, which is unrealistic. Note as well that the trap settings in the simulations were as such that a maximum density value of 4 to 5×10^{18}cm^{-3} was defined in the barrier, yet the hysteresis effects match well with the measurements. Hence, this is already an important indication that charge trapping alone cannot explain the (full) V_{TH} hysteresis values. Theoretically, all trapped charge could

reside at the AlGaN/GaN interface, and then the effect on the threshold voltage shift is twice as large, i.e.: $\Delta V_{TH} = \sigma_{it}/C_b$, with σ_{it} the *trapped charge* at the interface states. Again, this is considered to be an unrealistically high value for an interface between two semiconductors epitaxially grown in one process step (i.e. without air break).

These considerations let us conclude that trapped charges alone cannot explain the V_{TH} hysteresis effects as observed, and that the charging of the p-GaN layer is an important mechanism as will be illustrated in the next subsection.

C. Physical Insights based on TCAD simulations

Fig. 6 shows the simulated electrostatic potential monitored, during the V_G-sweep, in the middle of the floating p-GaN layer (at 40 nm away from gate metal and pGaN/AlGaN interface), in a region where the carrier density is constant since it is far away from the Schottky depletion region and the 2DHG layer. This p-GaN potential is a function of the applied gate voltage and of the mobile charge present in the p-GaN layer. The latter is strongly dependent on the balance between the Schottky diode and the AlGaN barrier (PiN diode) leakage. In particular, the p-GaN layer can be charged by hole injection/tunneling from gate metal, and discharged by hole tunneling/emission through the AlGaN barrier. For the DUTs, simulations revealed that hole discharging through the AlGaN barrier is dominated by tunneling and thermionic emission for V_G lower and higher than ~ 4 V, respectively.

The quasi-stationary condition (blue lines) shown in Fig. 6 represents the reference case in which all possible transients for each V_G value are completed. In fact, as expected, the p-GaN potential is the same during the V_G ramp up (solid line) and ramp down (dashed line, not observable as on top of the solid blue line). Similar behavior is observed in the case of slow transient characterization (from 0 V to 6 V in 1.2 s) except for a small difference in the subthreshold region (V_G < 1.5 V), whereas, in the case of fast transient (red), a significant difference is observed. In particular, the electrostatic potential of the p-GaN layer is lower during the V_G ramp down. The reason of such behavior is a different charging state of the floating p-GaN layer occurring during the transient sweeps, since the hole emission or tunneling through the AlGaN barrier PiN diode is time-dependent.

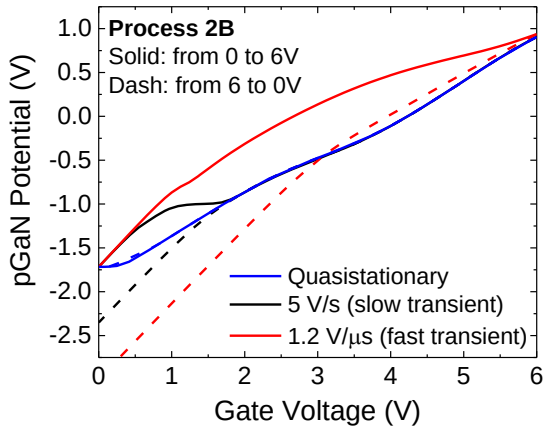

Fig. 6. Simulated electrostatic potential of the floating p-GaN layer as a function of the V_G swept with different times. Quasistationary represents the reference case, whereas fast and slow transients reproduce the experiments reported in Figs. 2 and 3 (solid lines = ramp up, dashed lines = ramp down).

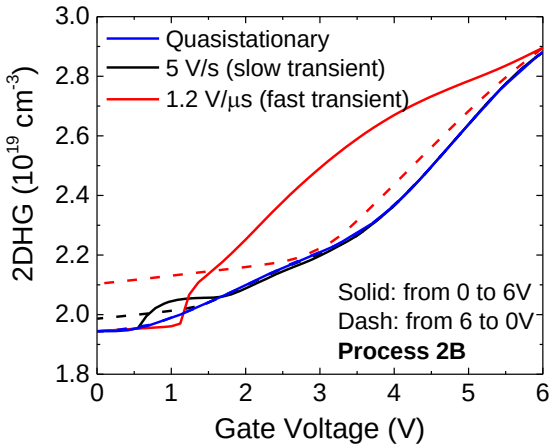

Fig. 7. Simulated two-dimensional hole gas (2DHG) volumetric charge, extrapolated at 1 nm from p-GaN/AlGaN interface as a function of the gate voltage swept with different times. As for Fig. 6, quasistationary represents the reference case, whereas fast and slow transients reproduce the experiments reported in Figs. 2 and 3.

Fig. 7 strengthens this hypothesis, showing the 2DHG volumetric charge (holes accumulated close to p-GaN/AlGaN interface), extrapolated at 1 nm from p-GaN/AlGaN interface, as a function of the gate voltage, in the same conditions as reported for Fig. 6. A difference is observed for $V_G > V_{TH}$ in the case of fast transient simulation, with a lower 2DHG during the V_G ramp down (dashed line) with respect to ramp up (solid line). The 2DHG reduction is caused by the holes tunneling/emission through the AlGaN barrier and/or by the electrons tunneling/emission from 2DEG, which in turn can recombine with holes at the p-GaN/AlGaN interface. The difference between slow and fast transient is ascribed to time-dependent charging and discharging processes.

Fig. 8 shows the electron trapping/de-trapping in the AlGaN barrier layer during the V_G ramp up and down, in the case of slow and fast transient simulation. Note that the slow transient is the same as the quasi-stationary result (not shown) except for a small difference in the subthreshold region (V_G < 1.5 V).

Fig. 8 shows that independently of the sweeping speed (fast or slow), the amount (peak) of charge trapping is similar, showing a peak at $V_G \sim V_{TH}$ (see Fig. 2c), meaning that an electron trapping saturation occurs when the 2DEG is formed.

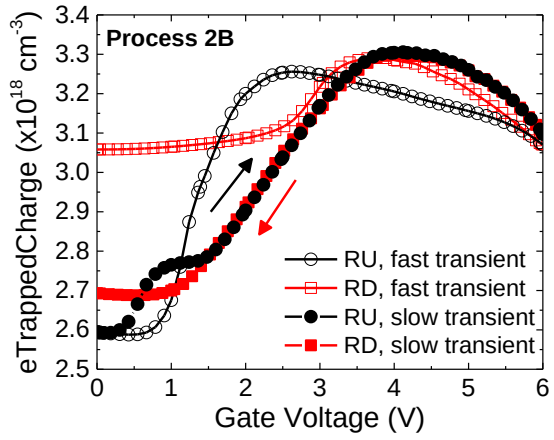

Fig. 8. Simulated electron trapped charge density in the AlGaN barrier layer as a function of the gate voltage swept with different times. Fast and slow transient represent a V_G sweeping time of 5 µs and 1.2 s from 0 V to 6 V, respectively. RU and RD stand for ramp up and ramp down.

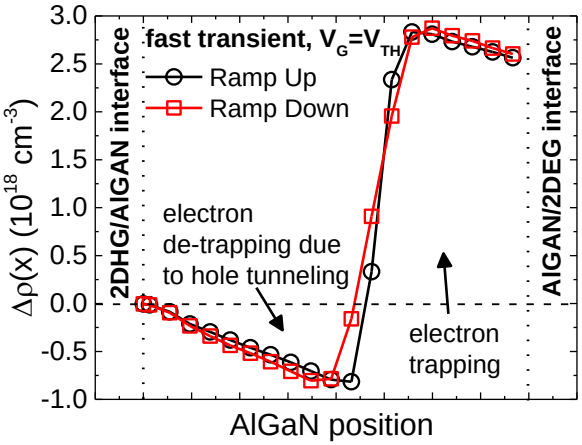

Fig. 9. Spatial distribution of the electron trapping/de-trapping charge along the AlGaN barrier layer, monitored during the fast sweeping ramp up and down at $V_G \sim V_{TH}$, i.e. the bias at which the peak of the trapped charge density occurs (see Fig. 8), and evaluated with respect to ρ(x) at V_G = 0 V

Moreover, part of such charge remains trapped only in the case of fast ramp down transient. However, the dynamics of the V_{TH} hysteresis cannot be directly ascribed to charge trapping in the AlGaN barrier. In particular, in the case of fast transient simulation, where the largest V_{TH} hysteresis is observed, the amount of trapped electron density during V_G ramp up (empty circles) and ramp down (empty squares) are similar, but they occur at different V_G, which roughly correspond to the related V_{TH} (see Fig. 2c). As a result, the device shows two different V_{TH} values (during ramp up and down) but the amount of trapped charge in the AlGaN barrier is similar, meaning that V_{TH} difference cannot be directly ascribed to the electrostatic effect of this trapped charge. This is further confirmed by the spatial distribution of the electron trapped/de-trapped charge density within the AlGaN barrier (Fig. 9), monitored at $V_G \sim V_{TH}$, i.e. the bias at which the peak of electron charge trapped density occurs (Fig. 8). In addition to amount of charge trapping, also the spatial distribution is similar. Furthermore, by looking at the 2DHG shown in Fig. 7, a similar density is shown at $V_G \sim V_{TH}$, i.e. $2.3 \cdot 10^{19}$ cm^{-3} with V_G = 2.2 V during ramp up and V_G = 3.5 V during ramp down. As a result, the charging effect of the floating p-GaN layer represents the dominant root cause of the dynamic threshold voltage hysteresis. However, it is worth noting that, the p-GaN layer charging/discharging is strongly dependent on the tunneling component through the AlGaN barrier layer, which on its turn is a function of the trapping mechanisms within the barrier. Therefore, an indirect role of the charge trapping mechanisms in the AlGaN barrier layer on the dynamic V_{TH} hysteresis should be recognized.

V. Conclusion

A combined experimental and simulation analysis, aimed at understanding the mechanisms responsible for the dynamic threshold voltage hysteresis, occurring under fast sweeping characterization in p-GaN gate HEMTs, has been reported.

Nonlocal tunneling TCAD models, implemented in Synopsys' Sentaurus simulator, have been properly tuned against experiments to reproduce the gate leakage and the related dynamic V_{TH} hysteresis. This TCAD approach has been validated on devices featuring different AlGaN barrier configurations, and considering different temperatures and sweeping times.

Simulations have revealed that the time-dependent charging/discharging processes of the floating p-GaN layer represent the root cause of the dynamic V_{TH} hysteresis, whereas the charge trapping mechanisms in the AlGaN barrier do not have a direct role. However, their role on the AlGaN barrier tunneling, which in turn contribute to discharging processes of the floating p-GaN layer, cannot be neglected.

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