Voltage Balancing of the DC-Link Capacitors in Three-Level T-Type Multiphase Inverters

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L. Vancini, M. Mengoni, *Member, IEEE*, G. Rizzoli, L. Zarri, *Senior Member, IEEE,* and A. Tani

***Abstract* - This paper illustrates an algorithm to balance the voltages across the DC-link capacitors of a three-level multiphase inverter feeding a star-connected load with an odd number of phases. The proposed strategy keeps the DC-link capacitors balanced in any operating condition and minimizes the low-frequency voltage oscillations, even during open-phase faults and with non-sinusoidal output currents. Finally, the paper identifies the operating region where the voltage oscillations of the DC-link capacitors can be canceled. The developed algorithm can maintain constant voltages even if the capacitors are unbalanced, and its performance is compared to that of other carrier-based algorithms. Experimental tests are carried out on a five-phase induction motor in healthy and faulty conditions.**

Index Terms - Pulse width modulation inverters, total harmonic distortion, variable speed drives.

I. Introduction

In the last decade, the interest in multiphase converters has grown due to the attention paid to fault tolerance and reliability of electric drives. Moreover, multiphase systems achieve high power levels by using power switches with limited current ratings. Simultaneously, multilevel converters have become a mature technology and represent the simplest way to achieve high power levels through devices with limited voltage ratings. For these reasons, multilevel multiphase converters can potentially meet the demand for high-power and reliable systems.

A traditional issue with three-phase multilevel converters is the voltage unbalance of the DC-link capacitors. This problem can be solved in a multiphase multilevel converter by exploiting the degrees of freedom of this technology.

In recent years, multiphase drives have become a viable solution in systems where reliability is a fundamental requirement, such as aerospace and naval applications [1]-[4]. Multiphase machines show some advantages compared to three-phase systems [5] in terms of torque density [6], torque quality and noise levels. The degrees of freedom of multiphase machines allow developing multi-motor systems fed by a single inverter [7]-[8]. Another feature of multiphase systems is that the current rating of the transistors of the power converter decreases as the number of phases of the machine increases. This characteristic is appreciated in high power applications where the technical limits of the commercial power switches impose a strong design constraint.

Conversely, multilevel converters improve the quality of output voltages and reduce the voltage stress of the components. This feature plays a crucial role in the design of high-power rating converters.

The advantages of multilevel inverters and multiphase drives can be considered complementary. Also, combining these technologies can lead to attractive solutions that improve the overall performance in different operating conditions.

As the number of levels increases, the complexity of the hardware and control system rises as well. Therefore, the three-level topology represents a good tradeoff between performance, cost and complexity for high-end industrial applications. The neutral-point clamped inverter and the T-type inverter are the most widespread three-level topologies due to their simple scheme, but several hardware configurations can produce the same output voltage levels [9]. However, most multilevel topologies are prone to voltage imbalance and low-frequency oscillations of the DC-link capacitors.

This voltage oscillation can reduce the maximum modulation index of the converter, affect the quality of the output voltages and currents, and even compromise the system stability. This problem has been thoroughly addressed for three-phase systems [10]-[11], whereas, for multiphase systems, there is no decisive solution.

A closed-loop balancing technique for the DC-link capacitors, based on a modulation strategy initially developed for 3-level inverters, was extended to multilevel multiphase inverters [12]. In [13] and [14], the same approach was improved through a decoupling matrix of the control commands, while the output frequency could be close to the switching frequency.

In [15]-[18], some Space Vector Modulation (SVM) strategies were developed for multilevel multiphase converters. These papers extend the concept of SVM from two levels to a higher number of levels. Also, they focus on the computational complexity and the cost of the hardware implementation. A comparison of carrier-based and Space Vector Pulse Width Modulation (SVPWM) techniques for three-level five-phase voltage source inverters was reported in [19].

Another algorithm for voltage balancing in multiphase multilevel converter was presented in [20]. This solution provides a recursive approach that can be extended to a generic number of phases while maintaining a carrier-based pulse-

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width modulation approach. The quality of the delivered power and the power losses of the converter were analyzed in [21].

The common-mode voltage, which can cause the failure of the motor bearings and electromagnetic interference problems, is another crucial problem in multiphase drives fed by multilevel converters, which is related to the balancing of the DC-link capacitors to some extent. An extensive review was presented in [21], where several aspects already published in the literature were discussed in depth. A general solution to this problem with SVPWM was presented for most multilevel topologies in [22], whereas a scalar PWM specifically developed for five-phase inverters is presented in [23].

A method consistent with the principle of the virtual space-vector PWM is presented in [24]. The proposed solution uses a switching pattern with a greater number of commutations than the traditional Carrier Based Pulse Width Modulation (CBPWM) to increase the degrees of freedom of the modulation. The main drawback of this approach is an increase in the inverter switching losses. In [25], a hybrid modulation technique is presented. This solution is based again on the multi-step approach but tries to reduce the additional switching losses with an optimized control algorithm. The voltage range of a multiphase T-type three-level inverter during an open circuit fault is analyzed in [26]. An interesting comparison between a five-phase three-level and five-phase two-level inverters is discussed in [27]. This paper demonstrates that efficiency, harmonic content, and common-mode voltage are better in multilevel converters although controlling two-level converters is simpler and requires less computational effort. The substantial equivalence between the CBPWM and the SVM is described and widely discussed in [28].

In recent years, hybrid topologies of multilevel inverters have been developed [29]-[32]. Generally, these new solutions have a boost dc-dc conversion capability, and the capacitor voltages are self-balancing. However, their hardware structure is not industrially consolidated yet and the complexity of the control system is higher.

Although the problem of voltage balancing and voltage ripple for the DC-link capacitors of multilevel multiphase inverters has already been tackled, this paper presents the following new contributions:

- a general carrier-based pulse width modulation to control the neutral point voltage of the DC-link capacitors of a three-level T-type multiphase inverter is developed. The proposed balancing technique employs only the zero-sequence component of the output voltages, while the nonzero voltage vectors can be freely used to implement advanced control algorithms of the electric machine

- the theoretical approach is based on the Vector Space Decomposition (VSD), which is very common for the analysis and the control of multiphase drives

- the method is extended to multiphase systems with an odd number of phases, fed by a three-level multiphase inverter with a single DC-link supply, and even with an unbalanced load (the only requirement is that the sum of the output currents is zero)

- the developed method is comprehensive and includes all the operating conditions, unmatched in three-phase systems, which are common in multiphase applications, such as the circulation of currents in the harmonic subspaces and the open-phase fault.

The proposed solution reduces the low-frequency voltage oscillations of the DC-link capacitors in any operating conditions, independently of the output power factor. Also, it reduces the low-frequency voltage oscillations even if the capacitances of the dc-link are unbalanced.

This paper is organized as follows. Section II describes the mathematical model of three-level multiphase inverter. This part includes the problem formulation, the analysis of the boundaries of the linear modulation for multiphase systems, and the calculation of optimal zero-sequence component of modulating signals that balance the DC-link capacitors. Section III illustrates the operating domain where the ripple of the voltage on the DC capacitors can be cancelled. Section IV addresses the implementation of the control scheme. In Section V, some experimental results, obtained with a five-phase induction motor drive fed by a three-level T-type inverter, are discussed. The tests have been carried out both in sinusoidal and unconventional conditions, such as the third harmonic current injection and an open-phase fault.

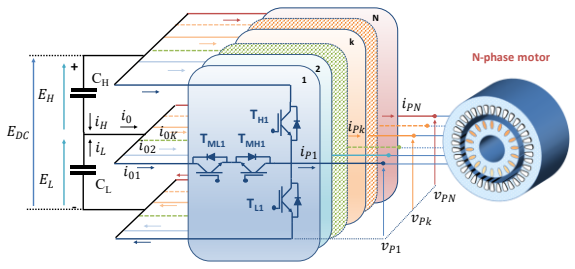


Fig. 1. Modular schematic of a three-level T-type *N*-phase inverter (*N* is odd).

II. Voltage Balance in Multiphase Inverter

A. Mathematical Model

A schematic description of a three-level Neutral Point Clamped (NPC) T-Type multiphase inverter is shown in Fig. 1. Each phase of the converter is composed by 4 power switches $(T_H, T_L, T_{MH}, T_{ML})$ with the respective freewheeling diodes. Capacitors C_H and C_L are connected to each other and play a key role to achieve the multilevel behavior. Normally, the voltages on the two capacitors should be kept equal to half the DC-link voltage. However, in general, the instantaneous ratio λ of the voltage on the lower capacitor, E_L, to the total voltage of the DC-link is different from 0.5:

$$\lambda = \frac{E_L}{E_H + E_L} \tag{1}$$

where E_H is the voltage on the upper capacitor C_H.

The derivatives of the capacitor voltages are related to the upper and lower currents i_H and i_L by the following relationships:

$$i_H = C_H \frac{dE_H}{dt} \tag{2}$$

$$i_L = -C_L \frac{dE_L}{dt} \tag{3}$$

If the capacitances C_H and C_L are equal ($C_H = C_L = C$), combining (2) and (3), one can easily verify that the difference between their voltages depends on the current i_0 [21], [24], which is defined as the sum of i_H and i_L:

$$\frac{d(E_H - E_L)}{dt} = \frac{1}{C}(i_H + i_L) = \frac{1}{C} i_0 \tag{4}$$

where

$$i_0 = i_H + i_L \tag{5}$$

Equation (4) states that, in order to keep the voltage difference $E_H - E_L$ constant, the current i_0 must be zero.

Fig. 1 shows that i_0 is the sum of the currents i_{0k} ($k = 1, \dots, N$) passing through the switches T_{MHk} and T_{MLk} of the kth leg.

$$i_0 = \sum_{k=1}^{N} i_{0k}\,. \tag{6}$$

It is straightforward to understand that i_{0k} depends not only on the output phase current i_{Pk}, ($k = 1, \dots, N$) but also on the adopted modulation strategy, which can affect the conduction time of the switches in each leg of the converter [21].

In the following sections, it is shown that the actual value of the modulating signals, the phase currents and their phase shift affect the oscillation of the voltage on the DC-bus capacitors.

B. Multiple Space Vectors and Modulation Strategies

The analysis of multiphase systems is usually based on the definitions of space vectors and zero-sequence component. For a given odd set of variables $x_1, \dots, x_N$, a new set of variables x_0 and $\bar{x}_\rho$ ($\rho = 1, 3, \dots, N-2$) can be defined through the following symmetrical linear transformations:

$$x_0 = \frac{1}{N}\sum_{k=1}^{N} x_k\,. \tag{7}$$

$$\bar{x}_\rho = \frac{2}{N}\sum_{k=1}^{N} x_k \bar{\alpha}_k^\rho \quad \rho = 1, 3, \dots, N-2 \tag{8}$$

where

$$\bar{\alpha}_k = e^{j\frac{2\pi}{N}(k-1)}. \tag{9}$$

The real quantity x_0 calculated by (7) is the zero-sequence component, whereas the variables $\bar{x}_\rho$ ($\rho = 1, 3, \dots, N-2$), usually called "multiple space vectors," are complex quantities.

In a multiphase inverter, the relationship between the modulating signals m_k ($k = 1, \dots, N$) and the zero-sequence component m_0 is given by the following equations [33]:

$$m_k = m_0 + n_k \quad k = 1,2, \dots, N \tag{10}$$

where

$$m_0 = \frac{v_0}{E_{DC}} \tag{11}$$

$$n_k = \frac{v_k}{E_{DC}}, \qquad k = 1,2, \dots, N \tag{12}$$

E_{DC} is the total DC-link voltage, v_k is the reference value of the kth load phase voltage, and v_0 is the desired zero-sequence component of the inverter pole voltages (often called common-mode voltage). The normalized voltages n_k ($k = 1, \dots, N$) can be rewritten in terms of reference voltage space vectors $\bar{v}_\rho$ ($\rho = 1, 3, \dots, N-2$) as follows [33]:

$$n_k = \frac{1}{E_{DC}}\left(\sum_{\rho=1,3,\dots,N-2} \bar{v}_\rho \cdot \bar{\alpha}_k^\rho\right), \quad k = 1,2, \dots, N \tag{13}$$

where the dot operator "·" is defined as the real part of the product of the first operand and the complex conjugate of the second operand.

The parameter m_0 does not affect the phase voltages and is a degree of freedom that can be used to improve the performance of the inverter. In the literature, several solutions to improve the operating characteristics of multiphase inverters by acting on this variable, have been analyzed [34].

The modulation strategies that will be compared in this paper are identified with the names Space Vector Pulse-Width Modulation (SVPWM), and Discontinuous Pulse-Width Modulation MIN or MAX (DPWM-MIN and DPWM-MAX), which resemble the names traditionally used for three-phase inverters [35]. The choice of the zero-sequence component for each of them is shown in Table I. The zero-sequence voltage of DPWM-MIN is selected so that the minimum modulating signal among m_1, ..., m_n becomes zero, whereas the maximum modulating signal of DPWM-MAX becomes one. Therefore, when these strategies are used, in every switching period, an inverter leg does not commutate. Since the DPWM-MIN and DPWM-MAX correspond to the boundaries of the linear modulation [36], the phase voltages can be synthesized without incurring in overmodulation only if m_0 satisfies to the following inequalities:

$$m_{0DPWM-MIN} \le m_0 \le m_{0DPWM-MAX} \tag{14}$$

Finally, the strategy called SVPWM is often referred to as "symmetric modulation." This is the generalization for N-phase inverters of the strategy commonly used in three-phase inverters.

TABLE I
ZERO-SEQUENCE OF THE MODULATING SIGNALS FOR SOME MODULATION STRATEGIES

Modulation type	m_0
DPWM-MIN	$m_{0\,DPWM-MIN} = -\min_{k=1,\dots,N} n_k$
DPWM-MAX	$m_{0\,DPW-\_MAX} = 1 - \max_{k=1,\dots,N} n_k$
SVPWM	$m_{0\,SVPWM} = \frac{m_{0\,DPWM-MIN} + m_{0\,DPWM-MAX}}{2}$

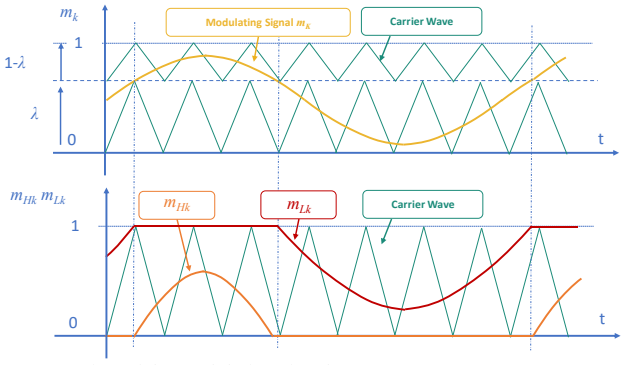


Fig. 2. Meaning of the modulating signals m_k, m_{Hk}, m_{Lk}.

C. Effect of the Zero-Sequence Component on DC-Voltage Balancing

The aim of this paper is the determination of the value of m_0 that minimizes the voltage ripple of the DC capacitors. The value of m_0 affects the modulating signals and, consequently, the value of the current i_0, which is responsible for the voltage imbalance of the capacitors.

With reference to the converter depicted in Fig. 1, to avoid the short circuit of input capacitor C_H, the switches T_{Hk} and T_{MHk} cannot be in the on state at the same time. Similarly, to avoid the short circuit of the capacitor C_L, the switches T_{MLk} and T_{Lk} cannot be in the on-state simultaneously. These constraints suggest defining two separate modulating signals, m_{Hk} and m_{Lk}, respectively for the upper switches (T_{Hk} and T_{MHk}) and the lower switches (T_{MLk} and T_{Lk}) of the *k*th leg. The gate signals of T_{MHk} and T_{Lk} are respectively the negated ones of T_{Hk} and T_{MLk}. The output pole voltage v_{pk}, defined as the voltage between the *k*th inverter pole and the negative terminal of the DC-link, can be expressed as follows:

$$v_{Pk} = m_{Hk}E_H + m_{Lk}E_L \tag{15}$$

Equation (15) can be rewritten by introducing the parameter λ:

$$v_{Pk} = E_{DC}[m_{Hk}(1-\lambda) + m_{Lk}\lambda]. \tag{16}$$

Furthermore, the modulating signals m_{Hk} and m_{Lk} can be related to the leg modulating signals m_k, introduced in (10), by means of the following relationships, whose meaning is illustrated in Fig. 2:

$$m_{Hk} = \begin{cases} \dfrac{m_k - \lambda}{1-\lambda} \; if \; m_k \geq \lambda \\ 0 \; Otherwise \end{cases} \qquad k = 1,2,\dots,N \tag{17}$$

$$m_{Lk} = \begin{cases} 1 \; if \; m_k \geq \lambda \\ \dfrac{m_k}{\lambda} \; Otherwise \end{cases} \qquad k = 1,2,\dots,N \tag{18}$$

The strategy, whose modulating signals are given by (17) and (18), is usually called single-step modulation [25].

The average value of i_{0k} over a switching period depends on the duty-cycles of the upper and lower switches:

$$i_{0k} = \begin{cases} (1-m_{Hk})i_{Pk} \; if \; m_k \geq \lambda \\ m_{Lk}i_{Pk} \; Otherwise \end{cases} \qquad k = 1,2,\dots,N \tag{19}$$

where i_{Pk} are the output phase currents. A compact formulation of (19), obtained through (17) and (18), is

$$i_{0k} = i_{Pk}\frac{1 + s_k(1-2m_k)}{1 + s_k(1-2\lambda)} \qquad k = 1,2,\dots,N \tag{20}$$

where the functions s_k $(k = 1,\dots,N)$ are defined as follows:

$$s_k = \begin{cases} +1 \; if \; m_k \geq \lambda \\ -1 \; Otherwise \end{cases} \qquad k = 1,2,\dots,N \tag{21}$$

According to (6), i_0 can be obtained by summing the contribution of all inverter legs. By replacing (20) in (6) and considering (10), it can be shown that i_0 depends on m_0.

$$i_0 = \sum_{k=1}^{N} i_{Pk}\frac{1 + s_k[1-2(m_0+n_k)]}{1 + s_k(1-2\lambda)} \tag{22}$$

As (4) states that the voltage imbalance of the input capacitors depends on i_0, (22) shows that it can be indirectly controlled though m_0. Solving (22) for m_0 leads to the following explicit expression:

$$m_0 = \frac{\sum_{k=1}^{N} i_{Pk}\frac{1 + s_k(1-2n_k)}{1 + s_k(1-2\lambda)} - i_0}{2\sum_{k=1}^{N} i_{Pk}\frac{s_k}{1 + s_k(1-2\lambda)}} \tag{23}$$

At steady state, i_0 must be equal to zero. Furthermore, when the upper and lower capacitor voltages are equal, the value of λ assumes a constant value of 0.5. In this condition, which is probably the most common one, (23) becomes:

$$m_0 = \frac{1}{2} - \frac{\sum_{k=1}^{N} i_{Pk}s_k n_k}{\sum_{k=1}^{N} i_{Pk}s_k} \tag{24}$$

Equation (24) clarifies that m_0 is the sum of $1/2$ and a fluctuating term that depends on the power exchanged by each phase, proportional to $i_{Pk}n_k$, and the coefficients s_k.

If the phase currents, i_{Pk}, and the values of voltages, E_H and E_L, are measured, and the desired value of the balancing current i_0 is calculated by the control system, (23) or (24) allow finding the zero-sequence component of the modulating signals. However, solving (23) or (24) is not straightforward because the parameters s_k $(k = 1,\dots,N)$ depend on m_0 as shown in (10) and (21). If m_0 varies from $m_{0DPWM-MIN}$ to $m_{0DPWM-MAX}$, the modulating signals m_k $(k = 1,\dots,N)$ go across the whole admissible range $[0,1]$, and the values of the functions s_k $(k = 1,\dots,N)$ change accordingly.

If all s_k are equal, the current i_0 does not depend on m_0, but only on the phase currents and voltages (25) and (26). Equation (25) gives the value of i_0 when all s_k $(k = 1,\dots,N)$ are equal to 1, while (26) calculates the value of i_0 when all s_k $(k = 1,\dots,N)$ are equal to -1.

$$i_{0+} = -\frac{1}{1-\lambda}\sum_{k=1}^{N} i_{Pk}n_k \tag{25}$$

$$i_{0-} = \frac{1}{\lambda}\sum_{k=1}^{N} i_{Pk}n_k \tag{26}$$

These two currents are opposite to each other when the capacitors are balanced ($\lambda = 0.5$). Also, the absolute value of i_0 is proportional to the power delivered to the load (divided by E_{DC}).

If the values of the functions s_k are not equal, (22) shows that current i_0 depends on m_0, the phase currents i_{Pk} and the normalized voltages n_k. Fig. 3 shows the trend of i_0 as a function of m_0 with different value of the load Power Factor (PF). This function is a piecewise line whose slope changes abruptly as soon as the configuration of the variables $s_1,\dots,s_N$ changes. It is worth noting that i_{0+} and i_{0-} have opposite signs and are always capable of increasing or reducing the unbalance of the capacitors. However, if the difference of the capacitor voltages has to be constant, i_0 must be zero. Fig. 3 shows that a value of m_0 that makes i_0 equal to zero always exists, provided it satisfies the constraints (14).

Therefore, finding the solution of (23) requires finding the admissible combinations of values $s_1,\dots,s_N$. To solve this problem, let us suppose that the signals n_k are ordered in descending order so that

$$n_1 > n_2 > \cdots > n_F > \cdots > n_N \tag{27}$$

and F is the index of the lowest modulating signal that is greater than or equal to λ:

$$m_F > \lambda \quad (28)$$

$$m_{F+1} < \lambda \quad (29)$$

It is straightforward to verify that, under the assumption that the coefficient s_k $(k = 1, \ldots, N)$ are not all equal, F must be an integer number in the range $[1, N-1]$. It results that s_k is equal to 1 for $k \leq F$ and equal to -1 for $k > F$. Consequently, if the sum of the load currents is zero, (23) can be rewritten as follows:

$$m_0 = \lambda - \frac{\lambda(1-\lambda) i_{0\,ref} - (1-\lambda)\sum_{k=1}^{N} i_{Pk} n_k + \sum_{k=1}^{F} i_{Pk} n_k}{\sum_{k=1}^{F} i_{Pk}}. \quad (30)$$

Equation (30) shows that, for each value of F in the range $[1, N-1]$, it is possible to find a value for m_0. Figs. 3 and 4 show the graphic solution of the capacitor balancing problem. Since i_0 is a piecewise linear function of m_0, to find the value of m_0 that makes i_0 equal to the reference current $i_{0\,ref}$, it is necessary to consider $N-1$ consecutive intervals.

Then, after calculating the modulating signals m_k as a sum of m_0 and n_k, it is necessary to verify that (28) and (29) are satisfied to ensure that m_0 is an acceptable solution of (23). Finally, to ensure the feasibility of the modulation strategy, m_0 must be included in the range (14). If this does not happen, m_0 can be clamped to the upper or lower boundary.

The previous algorithm can lead to three different outcomes, depending on whether there is a unique value, more values or no value of m_0 that generates the desired value of i_0 according to (22).

The first case (unique solution) is the most common. The simulation results have confirmed that it usually occurs when the power factor of the load is far from zero. The second case happens when the power factor of the load is very low. The trend of i_0 as a function of m_0 is not monotone, and (22) may have more solutions. The developed algorithm can find all of them by iterating the value of F and chooses the one nearest to $m_{0\,SVPWM}$, which is commonly recognized as a modulation strategy with good performance.

Finally, the modulation problem does not have a solution if the value of the current i_0 is too far from zero or m_0 does not comply with constraint (14). It is worth reminding that a non-zero i_0 is required by the control system when λ is different from 0.5 to balance the DC capacitors. Conversely, if i_0 is zero, the problem has always a feasible solution, provided that (14) is satisfied. If the algorithm does not provide a solution, m_0 is set to $m_{0\,DPWM-MIN}$ or $m_{0\,DPWM-MAX}$ depending on which one makes i_0 closer to the desired value.

The proposed algorithm can be easily compared with the technique illustrated in [21], which is very similar. This alternative method finds a sub-optimal solution to the problem of voltage balancing (Fig. 4) but reduces the switching losses of the converter. The corner points of the curve in Fig. 4 correspond to changes in the sign of the functions s_k. If m_0 is chosen among these values, there is a converter leg that does not commutate in the whole switching period.

The exact solution to the balancing problem is the value of m_0 that makes i_0 equal to the reference value $i_{0,ref}$. Usually, this solution is not in a corner point. Conversely, the suboptimal solution proposed in [21] is the closest corner point to the exact

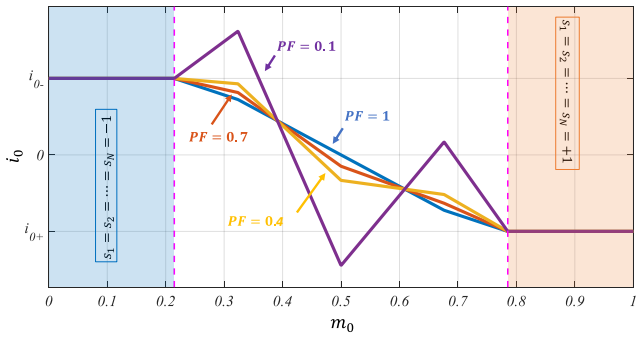


Fig. 3. Example of the trends of i_0 as a function of the zero-sequence m_0 for different values of the power factor PF in a five-phase inverter. With unity power factor, only one value of m_0 nullifies i_0. Conversely, at low power factor, three values of m_0 nullify i_0.

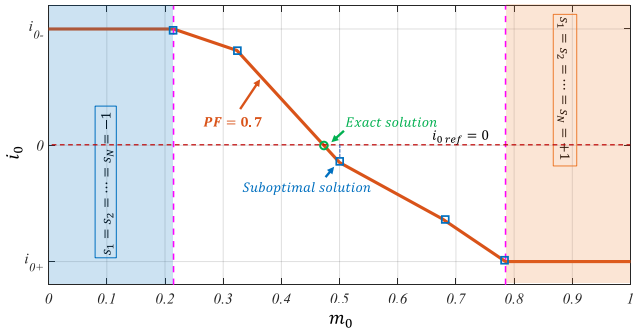


Fig. 4. Example of the exact and sub-optimal solutions when the power factor is 0.7 and $i_{0\,ref} = 0$.

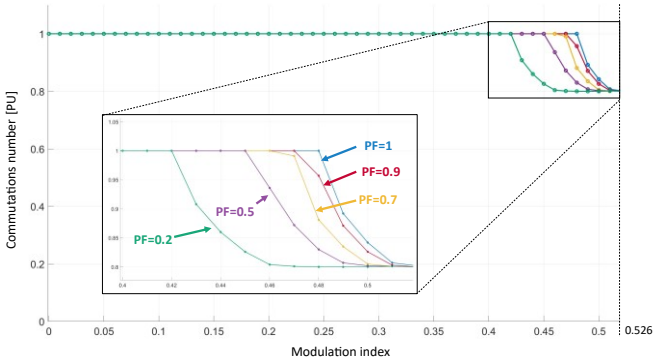


Fig. 5. Average number of commutations per second of the proposed solution for different values of the load power factor in a five-phase converter.

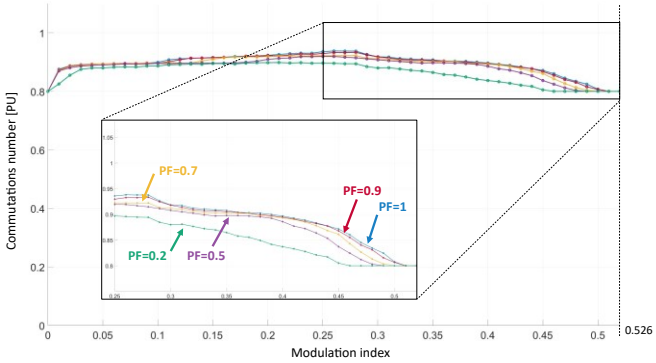


Fig. 6. Average number of commutations per second of the sub-optimal solution for different values of the load power factor in a five-phase converter.

solution. The resulting value of m_0 forces the pole voltage of an output phase to equal the voltage of the DC-link neutral point over an entire switching period, so the corresponding phase does not commutate. Therefore, the converter switching losses decrease to the detriment of an unavoidable voltage oscillation across the capacitors. Despite this shortcoming, this method provides good performance in many operating conditions.

Figs. 5 and 6 show the average number of commutations per second as a function of the modulation index for a five-phase inverter when the optimal and sub-optimal solutions are used. If the modulation index is low, the exact solution of m_0 is within the modulation limits (14), so the number of switch commutations per second and the voltage across the capacitors can be kept constant. If the modulation index increases, the calculated value of m_0 may not satisfy (14), and m_0 is set to $m_{0\,DPWM-MIN}$ or $m_{0\,DPWM-MAX}$, thus reducing the number of commutations. When the modulation index reaches the maximum value (0.526), there is always one leg of the converter that does not commutate in each switching period. In the case of a five-phase inverter, the number of commutations drops by 1/5 (20%).

Conversely, the sub-optimal solution always eliminates the commutations of a converter leg for all values of the modulation index. Theoretically, the number of commutations of an N-phase inverter should decrease by $1/N$ in percent, but some extra commutations happen due to the discontinuous waveform of m_0 (Fig 6.). The reduction in the number of commutations becomes less effective for large values of N.

The flowchart that describes the developed techniques is illustrated in Fig. 7. The algorithm can be conceptually divided into two parts. The first one finds the optimal values of m_0 that keep the capacitor voltages balanced (Fig. 7a). The second one selects the solution that respects the modulation limits (Fig. 7b).

Finally, for completeness, the diagram illustrating the selection process of m_0 in [21] is illustrated in Fig. 7c.

III. Domain Without Low-Frequency Voltage Oscillations

The voltages of the input capacitors comprise high-frequency harmonics due to the switch commutations, and low-frequency oscillations resulting from the converter operation. Whereas the former are unavoidable, the latter can be cancelled by a suitable choice of m_0, if the modulation index is lower than a threshold value that depends on the number of phases, the reference voltage vectors, the output phase currents and the load power factor in each subspace. Due to the large number of variables, it is not possible to find a simple description of this domain, but it can be plotted under the assumptions that only $\bar{v}_1$ and $\bar{\imath}_1$ are different from zero, and the input DC capacitors are balanced ($\lambda = 0.5$). The resulting boundaries of the modulation index MI have numerically been calculated and illustrated in Fig. 8 as a function of the number of phases N, and the displacement angle between $\bar{v}_1$ and $\bar{\imath}_1$. The modulation index MI shown in Fig. 8 is defined as the ratio between the magnitude of the required voltage vector $\bar{v}_1$ and the maximum voltage available in a three-phase system.

$$MI = \frac{|\bar{v}_1|}{E_{DC}/\sqrt{3}} \tag{31}$$

The higher the fundamental power factor, the higher the modulation index MI that can be reached while keeping the input capacitor voltages balanced.

As the number of phases increases, in sinusoidal steady-state operating conditions, the highest modulation index ensuring the voltage balance becomes less dependent on the fundamental power factor, but the maximum modulation index MI that guarantees the linear modulation range decreases. If the modulation index exceeds the value given by the curve of Fig. 4, for a given number of phases and a given displacement angle of the current, the developed algorithm keeps the input capacitors balanced on average, although a low-frequency voltage oscillations appears, which is the smallest possible in compliance with the voltage limits.

In order to investigate the amplitude of this low-frequency oscillations on the input capacitor voltages, it is necessary to introduce a new index, Q_0, which represents the imbalance charge of the capacitors in a fundamental period T, normalized by $T\,|\bar{\imath}_1|$:

$$Q_0 = \frac{\int_0^T |i_0|\,dt}{T|\bar{\imath}_1|}. \tag{32}$$

It is straightforward to verify that Q_0 is related to the variation of the quantity $C\ (E_H - E_L)$ over the time interval $[0, T]$.

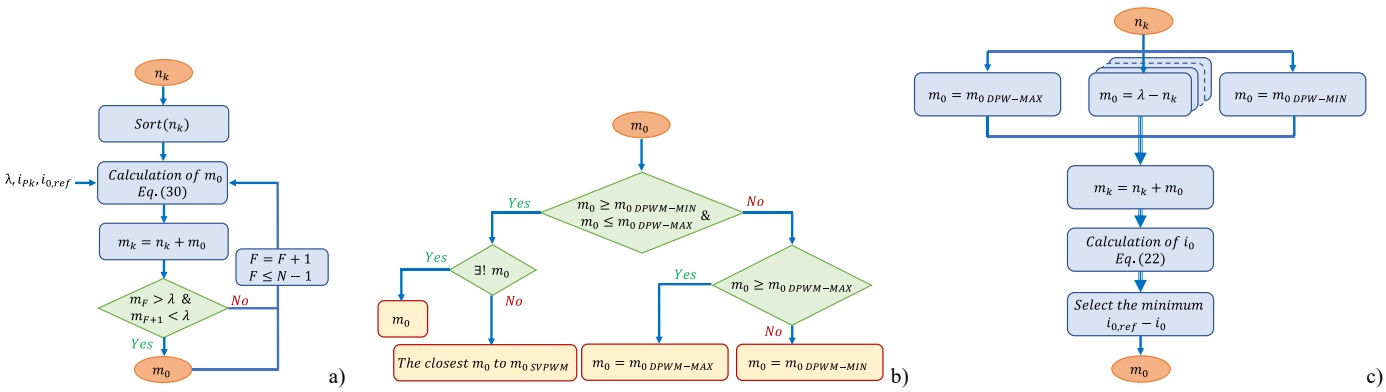


Fig. 7. Flow chart of the control algorithm. m_0 calculation (a), selection of the optimal value of m_0 (b), and sub-optimal solution (c).

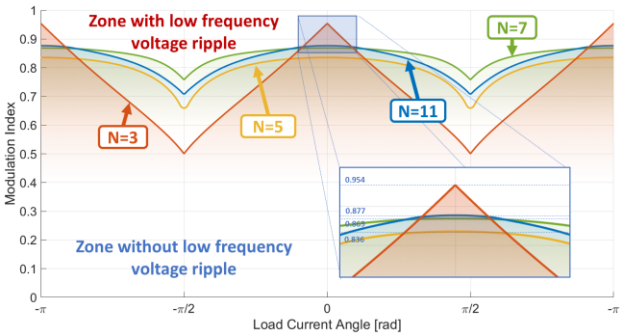


Fig. 8. Boundaries of the operating zone where the voltages of the input capacitors can be balanced without significant low-frequency voltage ripple for different number of phases.

Fig. 9a shows the amplitude of the oscillations of Q_0 as a function of the modulation index and load power factor for a five-phase inverter, under the assumption that the load currents and voltages are sinusoidal (only $\bar{v}_1$ and $\bar{\imath}_1$ are assumed to be different from zero). As can be seen, the oscillation of Q_0 is almost zero for low values of the modulation index. Fig. 9b shows the results obtained in the same operating conditions with SVPWM modulation.

In this case, a voltage oscillation is present for any modulation index other than zero, and the amplitude of the oscillation depends not only on the inverter current and the output voltage but also on the load power factor.

IV. Control Scheme for Voltage Balance

The control scheme that allows controlling the voltage of the input capacitors, through the measurement of voltages of the lower and upper capacitors, is shown in Fig. 10. The reference value of $E_H - E_L$ is equal to ΔE^*. To increase the imbalance, the current i_0 must be positive, whereas to reduce it, the current i_0 must be negative.

Finally, to maintain $E_H - E_L$ constant, the current i_0 must be zero. Therefore, the reference value for the current $i_{0,ref}$ is calculated as follows:

$$i_{0,ref} = -K_p[\,\Delta E^* - (E_H - E_L)] \qquad (33)$$

The proportional gain K_p affects the transient response of the system. Replacing (33) in (4), one finds a first order differential equation, whose time constant is C/K_p, which ensures the convergence of $E_H - E_L$ to ΔE^* with an exponential transient.

$$\frac{C}{K_P}\frac{d}{dt}(E_H - E_L) + (E_H - E_L) = \Delta E^*. \qquad (34)$$

The requested current i_0 is generated by solving (22) for m_0. The algorithm (30) that calculates m_0 requires as input signals the reference phase voltages v_k $(k = 1, \dots, N)$, the actual phase currents i_{Pk} $(k = 1, \dots, N)$, the value of λ, and the desired current i_0.

V. Experimental Results

In order to validate the developed solution, several tests have been carried out with a three-level five-phase inverter. To test the behavior of the control scheme in a practical application, the inverter was connected to a five-phase induction motor, the

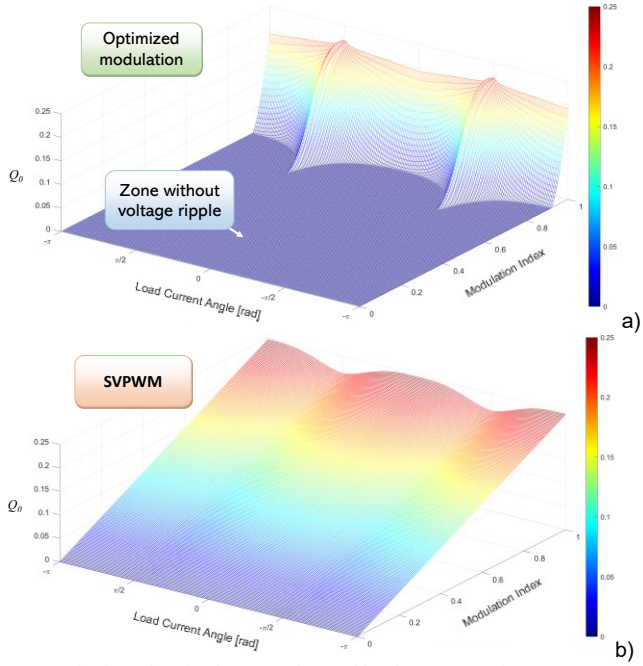


Fig. 9. Equivalent electric charge exchanged by the DC capacitors over a period of the output voltage in a five-phase inverter with the developed optimized modulation (a) and SVPWM (b).

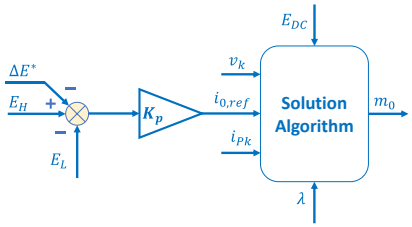


Fig. 10. Control scheme for the voltages of the DC capacitors.

control scheme is illustrated in Fig. 11. The motor parameters are shown in Table II while the inverter parameters are in Table III. The control scheme was implemented on a TMS320F28335 development board, produced by Texas Instruments. A picture of the experimental set-up is depicted in Fig. 12. A rotor field-oriented control scheme was used for the five-phase induction motor, and a closed-control loop was used to adjust the motor speed, measured by an incremental encoder. The computational time of the entire control system that adopted SVPWM to control the inverter, without balancing the voltages of the input capacitors, was 90 µs, while the control system with the balancing algorithm took 140 µs, which corresponds to an increase of about 50% in the calculation time.

Fig. 13 shows the waveforms of the capacitor voltages and a phase current in steady-state operating conditions at low speed (100 rpm), which is usually more demanding than at high speed. When the SVPWM technique is used, the voltages of the input capacitors fluctuate at five times the fundamental frequency, whereas the proposed balancing technique keeps them almost constant. The remaining small oscillations are due to the inverter dead times and nonlinearities. As can be seen, the waveform of m_0 is significantly different in the two tests, but the output phase current is sinusoidal in both cases.

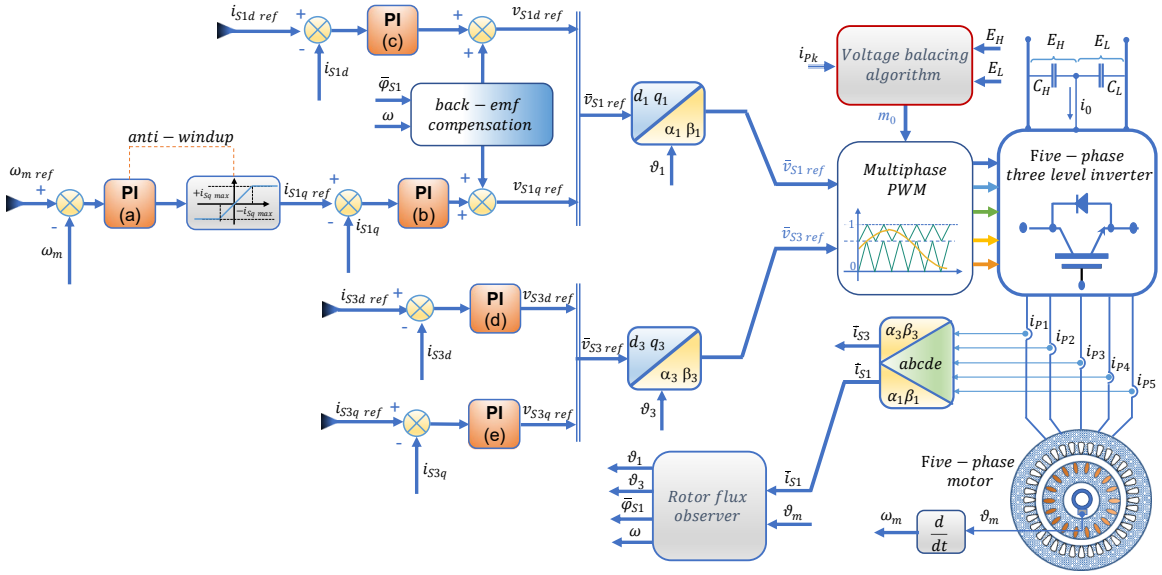


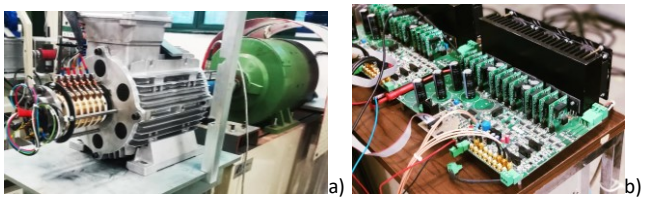
Fig. 11. Control scheme of the five-phase induction motor drive.

TABLE II
PARAMETERS OF THE FIVE-PHASE MACHINE

$\omega_{m,rated}$ = 15.7 rad/s (150 rpm)	p = 3
R_S = 1.7 Ω	R_R = 2.03 Ω
L_{S1} = 410 mH	L_{S3} = 68 mH
L_{R1} = 399 mH	L_{R3} = 65.8 mH
M_1 = 362 mH	M_3 = 35 mH

TABLE III
PARAMETERS OF THE FIVE-PHASE THREE-LEVEL INVERTER

SiC MOSFET I_{max} = 36 *A*, E_{DC} = 120 *V*
P_{rated}=3 *kVA*
Switching frequency = 5 kHz, dead time = 2.6 μs
$C_H = C_L$ = 300 μF



a) b)

Fig. 12. Experimental set-up of the electric drive composed by a five-phase wound-rotor induction machine a) and a five-phase three level inverter b).

Fig. 14 compares the results of the suboptimal solution [21] and the proposed solution in the operating conditions of the previous test. Compared to SVPWM, the suboptimal solution presents a lower fluctuation of the capacitor voltages but still higher than the proposed solution. The analysis of waveforms and the spectrum of the pole voltage, shown in Fig. 15, confirms that the sub-optimal solution reduces the number of commutations per second but the discontinuous behavior of m_0 leads to a higher voltage noise since m_0 is a highly discontinuous signal in the former case. Still, this difference is little appreciable in the waveform of the currents because of the low-pass filtering action of the load.

Fig. 16 shows the behavior of the inverter when the modulating index exceeds the threshold value that allows balancing the input capacitors. The DC-link voltage is lowered from 120V to 80V. If the modulation index is sufficiently low, the voltages of the capacitors remain constant. Conversely, if m_0 reaches the boundaries of the linear modulation (14), a voltage oscillation arises.

Fig. 17 shows the trends of the capacitor voltages during a speed transient when the inverter is controlled through the SVPWM (Fig. 17a) or the proposed algorithm (Fig. 17b). The modulation index increases as long as the speed increases. The SVPWM technique causes the oscillation of the capacitor voltages both at low and high speeds, while the developed technique is able to cancel the voltage oscillation at low speed and leads to a voltage ripple of the capacitors at high speed that is lower than that generated by the standard technique.

The developed algorithm can keep the capacitor voltages constant even if the control system involves subspaces other than the fundamental one. In Fig. 18, it is possible to observe the waveform of the inverter voltages when a current vector $\bar{\imath}_{S3}$, rotating in subspace $\alpha_3 - \beta_3$ at three times the fundamental frequency ($i_{S3d\,ref} = 2\,A$, $i_{S3q\,ref} = 0\,A$) is superimposed to current vector $\bar{\imath}_{S1}$($i_{S1d\,ref} = 2\,A$, $i_{S1q\,ref} = 2\,A$). The current vector $\bar{\imath}_{S3}$ can be intentionally injected to increase the torque density both in multiphase induction machines [6], [37] and in surface permanent magnet machines [38]-[40]. Fig. 18 also shows the spectrum of a stator current. As can be seen, regardless of the waveform of the stator current and the involved subspaces, the developed algorithm can balance the voltage across the capacitors.

Multiphase machines are well-known for their fault tolerance capabilities. Therefore, the electric drive has been tested while the control system is forced to keep the current i_{P1} equal to zero to simulate an open phase fault. For this task, the control system must control the current vectors in all subspaces.

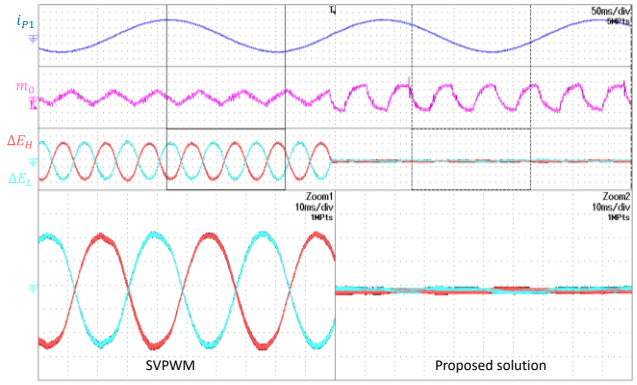


Fig. 13. Experimental results. Behavior of a three-level five-phase electric drive at 100 rpm with SVPWM and the proposed solution. Phase current i_{P1} (2 A/div), zero sequence component of modulating signals m_0 (0.1/div), variation of the DC-link capacitor voltages E_H and E_L from $E_{DC}/2$ (4 V/div).

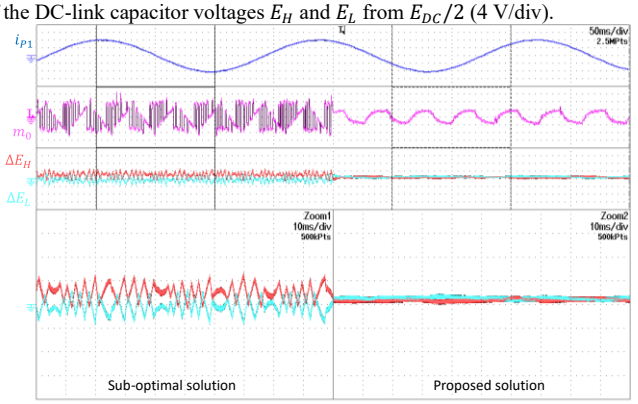


Fig. 14. Experimental results. Behavior of a three-level five-phase electric drive at 100 rpm with the suboptimal solution and the optimal solution. Phase current i_{P1} (2 A/div), zero sequence component of modulation signals m_0 (0.2/div), variation of the DC-link capacitor voltages E_H and E_L from $E_{DC}/2$ (4 V/div).

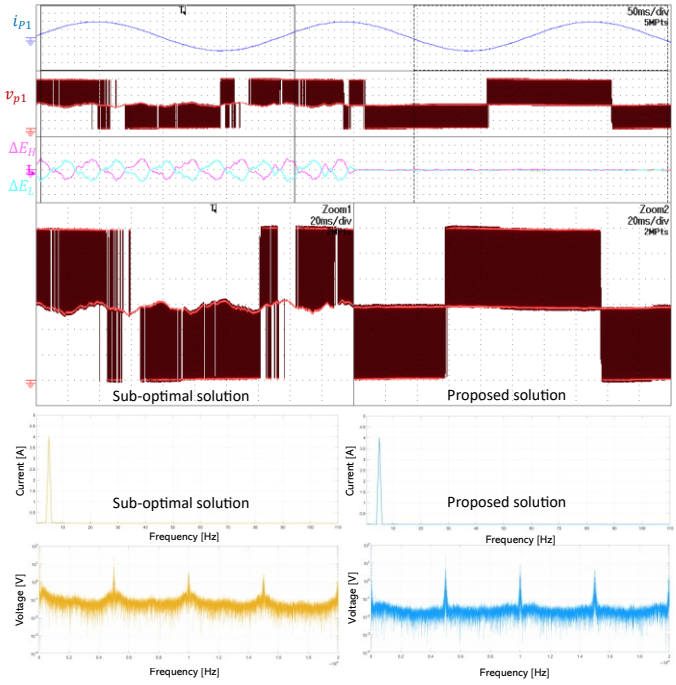


Fig. 15. Experimental results. Behavior of a three-level five-phase electric drive at 100 rpm with the suboptimal solution and the optimal solution. Phase current i_{P1} (2 A/div), pole voltage v_{p1} (20 V/div), variation of the DC-link capacitor voltages E_H and E_L from $E_{DC}/2$ (4 V/div). Phase current and pole voltage spectra.

Among the different fault-tolerant techniques, the control strategy that minimizes the stator Joule losses has been used, which has thoroughly investigated in the literature [41].

Fig. 19 shows that the voltages of the input capacitor are equal to one another, and their voltage ripple is negligible although the current of phase 1 is zero.

Fig. 20 shows different imbalance values in the voltages of the DC capacitors, obtained through a set point ΔE^*different from zero. Even in unbalanced conditions ($\lambda \neq 0.5$), the capacitor voltages do not show significant oscillations.

Finally, Fig. 21 shows the effect of an unbalance in the

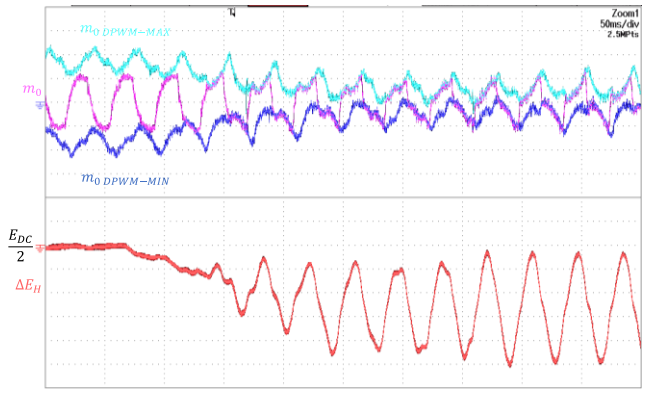


Fig. 16. Experimental results. Waveform of m_0 when the DC-link voltage of a three-level five-phase electric drive rotating at 100 rpm decreases from 120 V to 80 V. Zero-sequence component of modulation signals m_0 (0.2/div), variation of the DC-link capacitor voltages E_H from $E_{DC}/2$ (4 V/div).

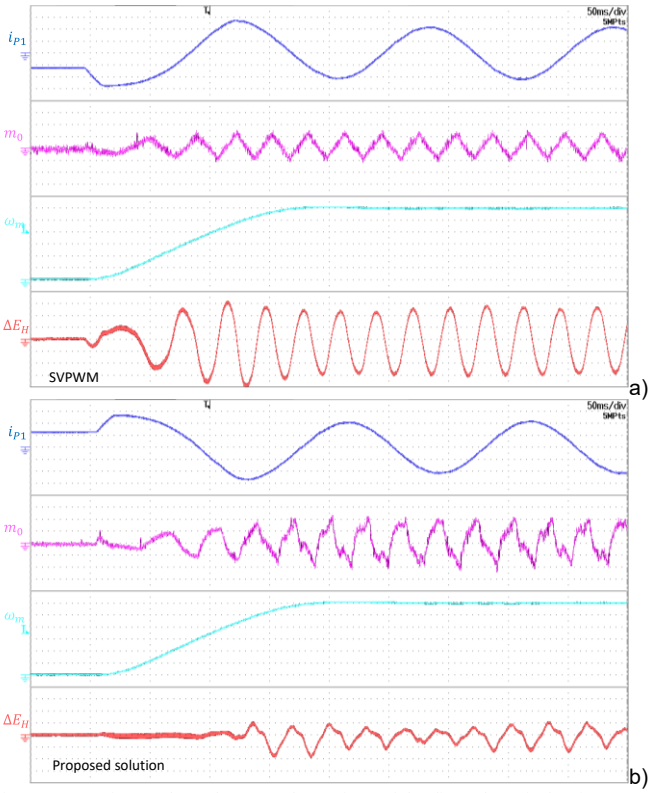


Fig. 17. Experimental results. Speed transient of the five-phase induction motor drive from 0 rpm to 120 rpm with SVPWM (a) and with the proposed modulation strategy (b). Phase currents i_{P1} (2 A/div), zero-sequence component of modulating signals m_0 (0.2/div), rotor speed (20 rpm/div), variation of the DC-link capacitor voltages E_H from $E_{DC}/2$ (4 V/div).

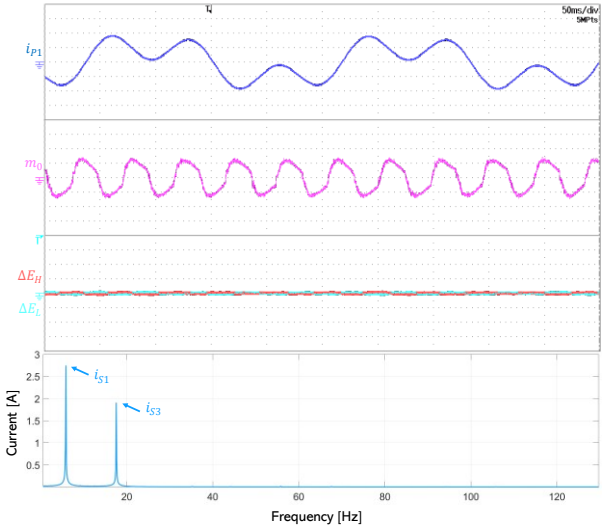


Fig. 18. Experimental results. Third harmonic injection. Phase current i_{P1} (2 A/div), zero-sequence component of modulating signals m_0 (0.1/div), variation of the DC-link capacitor voltages E_H and E_L from $E_{DC}/2$ (4 V/div). Phase current spectrum.

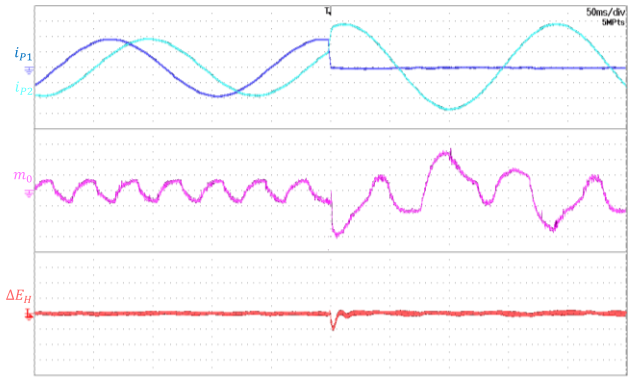


Fig. 19. Experimental results. Behaviour of the multilevel inverter when the current of phase 1 is kept equal to zero to simulate an open-phase fault. Phase currents (2 A/div), zero-sequence component of the modulating signals m_0 (0.2/div), variation of the DC-link capacitor voltages E_H from $E_{DC}/2$ (4 V/div).

capacitances of the DC-link capacitors ($C_H = 300\ \mu F, C_L = 150\ \mu F$). By cancelling the neutral point current i_0, the developed technique is not affected by the capacitor imbalance, while the SVPWM technique shows an asymmetry in the oscillations of the DC-link capacitor voltages.

VI. Conclusions

The paper presents a modulation technique that allows avoiding low-frequency voltage oscillations of the DC-link capacitors in multiphase multilevel inverters, even when the control system involves subspaces different from the fundamental one. The proposed solution can balance the capacitor voltages and control them separately.

The algorithm is valid for a generic odd number of phases, under the assumption that the load is star-connected with a single isolated neutral point. Furthermore, the operating domain ensuring the cancellation of the low-frequency oscillation of the capacitor voltages is shown when only the fundamental

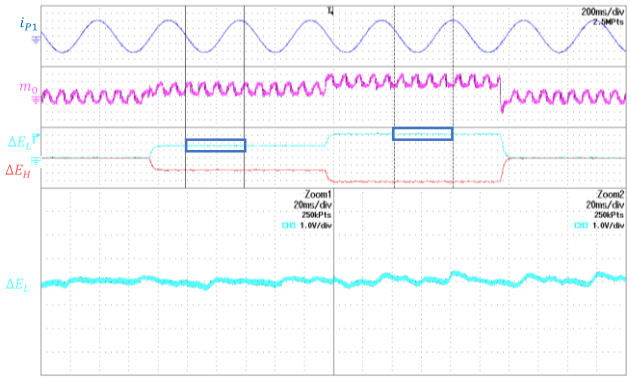


Fig. 20. Experimental results. Imbalance of the DC-link capacitor voltages. Phase current i_{P1} (1 A/div), zero-sequence component of the modulating signals m_0 (0.02/div), variation of the DC-link capacitor voltages E_H and E_L from $E_{DC}/2$ (5 V/div).

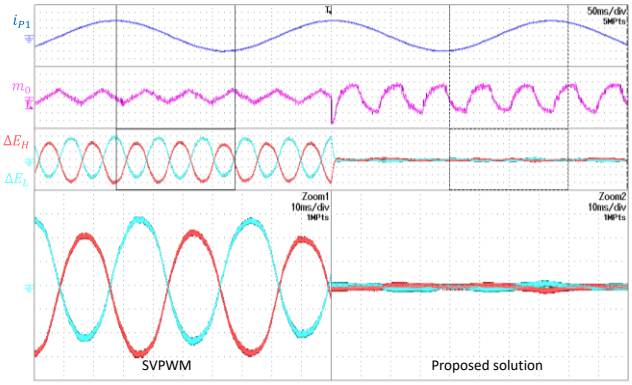


Fig. 21. Experimental results. Capacitance unbalance $C_H = 300\mu F, C_L = 150\mu F$. Phase current i_{P1} (2 A/div), zero sequence component of modulating signals m_0 (0.1/div), Variation of the DC-link capacitor voltages E_H and E_L respect to $E_{DC}/2$ (4 V/div).

subspace is used. Finally, the results of some experimental tests, carried out on a five-phase induction motor, are presented to demonstrate the feasibility of the developed algorithm, in transient and steady-state operating conditions, and in case of an open-phase fault with current harmonic injection.

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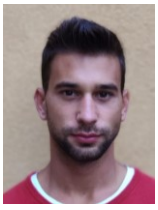

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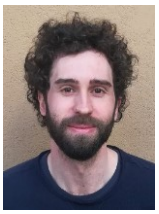

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