Reliability Risks Due to Faults Affecting Selectors of ReRAMs and Possible Solutions

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M. Omaña, S. Bardhan, C. Metra, *Fellow, IEEE*

Abstract— Resistive Random Access Memories (ReRAMs) are considered amongst the most promising candidates to replace silicon-based memories in the near future, when huge amount of data have to be stored. However, ReRAMs suffer from reliability issues associated to faults affecting both their resistive elements and their selectors. While some solutions have been presented in literature to detect, or tolerate, faults affecting the resistive element, so far no solution has been yet proposed to detect, or tolerate, faults affecting the selector, albeit these faults have been proven to be likely and possibly compromising the reliability of ReRAMs. In this paper, we analyze the effects of the most likely faults (i.e., shorts and opens) possibly affecting the selectors of ReRAM cells on the operation of the crossbar memory array. We show that a selector failing as a short can give rise to numerous errors on the ReRAM crossbar array. As an example, for the case of a crossbar array of 128x128 cells, we show that a single selector failing as a short may cause up to 64 errors in memory cells sharing the same word line of the cell containing the faulty selector. Such a large number of errors exceeds the correction capability of ECCs usually adopted for ReRAM arrays. Therefore, new solutions enabling to tolerate the large number of errors caused by selector faults in crossbar arrays are needed, to enable the use of this kind of promising memories for all applications mandating the ability to store huge amount of data, in a reliable way. We then propose a low-cost approach to detect short faults affecting selectors of ReRAMs and to identify the bitline containing the cell whose selector is faulty. Such a bitline can then be properly deactivated and replaced by a spare one, in order to guarantee the memory correct operation in the field.

Index Terms—Resistive Memory, ReRAM, Crossbar Memory Arrays, Reliability

1 Introduction

THE increasing demand for large capacity memories in modern data-intensive applications has recently motivated semiconductor manufacturers to explore the adoption of memory elements based on emerging (non-silicon) technologies, such as Phase Change Memory (PCM), Resistive Random Access Memory (ReRAM), Ferroelectric RAM (FeRAM), Magnetic RAM (MRAM) [1, 2, 3]. Among them, ReRAMs are a promising candidate to replace silicon-based memories, especially when huge amount of data has to be stored. In fact, ReRAMs enable higher density and scalability than FeRAM and MRAM, present better performance than PCM, and are also compatible with the CMOS fabrication process [5, 6, 2, 3, 4].

Each ReRAM cell is basically composed by a programmable resistive element, that is connected in series with a selector [2, 3]. The programmable resistive element enables to store information based on the value of its resistance [2], while the selector enables to perform read/write operations on the selected cell(s), minimizing the leakage current (sneak paths) through the unselected cells of the array [2]. Selectors can be implemented by any device with a high non-linearity in the I-V characteristic, such as bidirectional diodes, or transistors [2, 3].

While ReRAMs offer several benefits over alternate memories, they suffer from reliability issues associated to faults possibly affecting their resistive elements [7, 8, 9], or selectors [2]. Some solutions have been presented in the literature to detect, or tolerate, faults affecting the resistive element of ReRAMs (e.g., [7, 8, 9, 10]). Instead, so far, no solution to detect, or tolerate, faults affecting the selector of ReRAMs has yet been presented, despite such faults may constitute a serious problem for the reliability of ReRAMs [2]. In fact, preliminary analyses reported in [2] suggested that most likely faults affecting the selectors of ReRAMs (i.e., shorts and opens) may potentially induce a large number of erroneous bits [2].

Based on these preliminary results, in this paper we analyse the effects of the most likely faults (i.e., shorts and opens) affecting the selectors of ReRAM cells on the operation of the crossbar memory array. We will show that, for the case of a crossbar array of 128x128 cells, considered here as representative case study, a single selector failing as short may cause up to 64 errors in memory cells sharing the same wordline of the cell containing the faulty selector. Such a large number of errors exceeds the correction ability of ECCs usually adopted in ReRAM memory arrays. Therefore, new solutions to tolerate the large number of errors caused by selector faults in crossbar arrays are needed, in order to enable the use of this kind of promising memories for all applications mandating the ability to store huge amount of data in a reliable way.

Based on these achieved results, we then introduce a low-cost approach to detect short faults affecting selectors of ReRAMs and to identify the bitline containing the cell whose selector is faulty. Such a bitline can then be properly deactivated and replaced by a spare one present in the memory array [2], thus guaranteeing the memory correct

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operation in the field.

The rest of the paper is organized as follows. In Section 2, we recall some basic concepts on ReRAMs. In Section 3, we analyze the effects of most likely ReRAM selector faults on the operation of the crossbar memory array. In Section 4, we introduce our proposed low-cost detection approach. Finally, we draw some conclusive remarks in Section 5.

2 Preliminary Concepts on ReRAMs

As known [1, 2, 3], ReRAMs consist of a regular array of cells, each one composed by a memory element that exploits its varying resistance to store information. Such a memory element is generally implemented by a metal/insulator/metal structure (e.g., a thin film of TiO_2, or Cu_2O, placed be-tween two platinum contacts).

In order to maximize integration density, cells are usually located between two interconnect layers [1, 2, 11, 12, 14] resulting in a crossbar array, as schematically represented in Fig. 1.

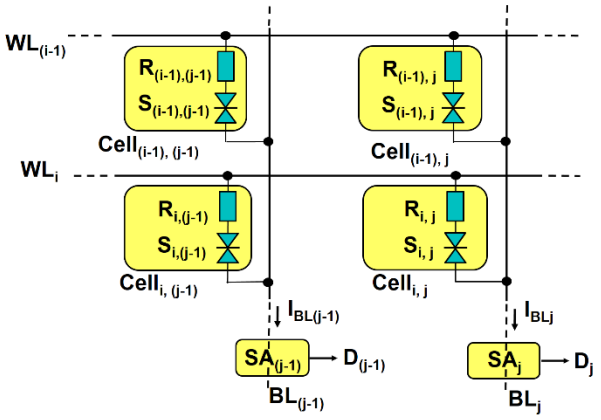

Fig. 1. Schematic representation of a portion of a ReRAM crossbar array.

In the crossbar array, the horizontal wires (WL_i) constitute wordlines, while the vertical wires (BL_j) the bitlines. The ReRAM cells connect the wordlines to the bitlines at each intersection of horizontal and vertical wires.

Stored data depend on the value of the resistance of the ReRAM cells: a low resistance state (LRS) corresponds to a logic "1", while a high resistance state (HRS) represents a logic "0" [2].

During writing operations, the resistance of the ReRAM cell can be changed from HRS to LRS (i.e., in order to write a 1) by applying an appropriate positive voltage (V_{W1}) across the cell. Similarly, the resistance can be changed from LRS to HRS (i.e., in order to write a 0) by applying a negative voltage ($-V_{W0}$) across the cell. To read the cell, a positive voltage (V_R) smaller than V_{W1} is applied across the cell. In particular, to read a given $cell_{i,j}$, a voltage equal to V_R is applied to WL_i, while a voltage equal to 0V is applied to the BL_j, so that the voltage drop across the cell equals V_R. The current flowing through the bitline BL_j (I_{BLj}) is compared to a proper reference current (I_{Ref}) by means of a current sense amplifier SA_j [13]. If $I_{BLj} > I_{Ref}$ ($I_{BLj} < I_{Ref}$) then a logic 1 (0) is given to the output D_j of SA_j.

As for the sense amplifier SA_j (Fig. 1), we considered a current sense amplifier of the kind in [13], whose implementation is schematically shown in Fig. 2.

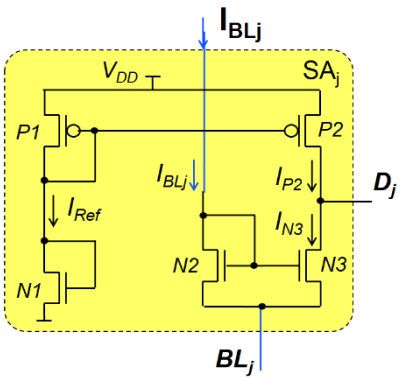

Fig. 2. Schematic representation of the implementation of a current sense amplifier SA_j of the kind in [13].

In particular, the value of reference current I_{Ref} can be chosen equal to a desired value, by properly sizing the N1 nMOS transistor and the P1 pMOS transistor in Fig. 2. Transitors P1 and P2 constitute a current mirror [13], so that, if P2 operates in the saturation region, it is $I_{P2} = I_{Ref}$. Similarly, N2 and N3 constitute another current mirror, so that, if N3 operates in the saturation region, it is $I_{N3} = I_{BLj}$. On the other hand, P2 and N3 are series transistors, which makes $I_{P2} = I_{N3}$. In order to satisfy this latter condition when $I_{Ref} \neq I_{BLj}$ (which is always the case during the memory operation), trasistors P2 and N3 cannot be in saturation simulataneously.

In particular, if it is $I_{BLj} > I_{Ref}$ ($I_{BLj} < I_{Ref}$) N3 operates in the saturation (linear) region, while and P2 is in the linear (saturation) region, so that $V_{Dj} = V_{DD}$ ($V_{Dj} = 0$). Therefore, as described above, for $I_{BLj} > I_{Ref}$ ($I_{BLj} < I_{Ref}$), SA_j produces a logic 1 (0) at its output D_j.

3 Performed Analyses and Results

By means of HSpice electrical level simulations, we have analyzed the effects of shorts and opens affecting the selector of ReRAM cells on the correct operation of a crossbar array of 128x128 cells, considered here as a representative case study.

We have implemented the ReRAMs by using the HSpice model in [14], considering two anti-parallel diodes as selectors [15]. Moreover, we have implemented the current sense amplifiers (SA_j) as shown in Fig. 2 [13], considering a 32nm standard CMOS technology, with the crossbar wire model described in [16].

For the correct memory operation, we have considered the following write voltages across a selected $cell_{i,j}$: V_{W1} = +2.5V, V_{W0} = -2.5V. Terefore, in order to write a logic 1 (0), we apply a voltage of 2.5V (0V) on the wordline WL_i and a voltage of 0V (2.5V) on the bitline BL_j. In addition, to read a $cell_{i,j}$ we have considered a reading voltage V_R = +1.1V, so that we apply a voltage of 1.1V on the wordline WL_i and a voltage of 0V on the bitline BL_j.

As for the word (bit) lines different from that of the selected $cell_{i,j}$, we have assumed them all connected to 1.25V

(0.55V) during the write (read) of $cell_{i,j}$.

In addition, we have designed the transistors of the sense amplifiles (Fig. 2) so that it results I_{Ref} = 135μA. Such a I_{Ref} value is an intermediate current value (chosen here as an example) between those that, by means of electrical level simulations, we have verified are produced when reading a 1 and a 0. Our simulations results are however independend of the considered I_{Ref} value.

As for opens and shorts affecting the selector of ReRAM cells, we have emulated them by substituting the faulty selector by a resistance with a very high (equal to 10M Ω) and a very low (equal to 0.1Ω) resistance value, respectively [9]. Morevoer, we have considered faults occurring one at a time, as usual for on-line detection in the field [17].

To analyze the effects of shorts and opens affecting the selectors of ReRAM cells, we have considered the following scenarios: 1) the cell with the faulty selector shares the same wordline as the cell selected for write/read operations; 2) the cell with the faulty selector is selected for write/read operations; 3) the cell with the faulty selector shares the same bitline as the cell selected for write/read operations; 4) the cell with the faulty selector shares neither the wordline, nor the bitline of the cell selected for write/read operations.

Let us start reporting the effects of shorts affecting the selectors of ReRAM cells for all these possible cases.

Fig. 3(a) shows the waveforms obtained when writing a 1, and then reading, $cell_{10,90}$ (i.e., the cell with WL=10 and BL=90), for the case of a fault free memory array. Instead, Fig. 3(b) reports the waveforms obtained for the same operations on the same cell as in Fig. 3(a), but in the presence of a non-selected cell (e.g., $cell_{10,70}$, with WL=10 and BL=70) affected by a short on its selector, sharing the same wordline WL_{10} as the selected cell.

From Fig. 3(a) we can notice that, in the fault free case, during the write operation of a logic 1 on $cell_{10,90}$ (V_{WL_10} = 2.5V and V_{BL_90} = 0), the resistance of the cell correctly changes from a HRS (of approx. 20KΩ) to a LRS (of approx. 1kΩ). Moreover, in the following read operation of $cell_{10,90}$ (V_{WL_10} = 1.1V and V_{BL_90} = 0), as expected, a logic 1 is given to the output of the sense amplifier (i.e., V_{D_90} = 1.1V).

Instead, Fig. 3(b) shows that, in the faulty case, during the write operation of a logic 1 on $cell_{10,90}$, the resistance of the cell does not change from a HRS to a LRS, but it maintains incorrectly a HRS. Therefore, the short affecting the non-selected $cell_{10,70}$, sharing the same WL_{10} as the selected $cell_{10,90}$, inhibits to write correctly the selected cell. This effect is confirmed by the following read operation of $cell_{10,90}$, during which an incorrect 0 is obtained at the sense amplified output (V_{D_90} =0V).

The reason of the incorrect writing of the selected $cell_{10,90}$ is the large current flowing through the faulty non-selected $cell_{10,70}$ (due to the short affecting its selector). Such a large current flowing through $cell_{10,70}$ generates an excessive voltage drop on the parasitic resistance of the wordline wire, which significantly reduces the effective voltage applied across the selected $cell_{10,90}$, which results lower than that required to change (as desired) the state of the cell resistance.

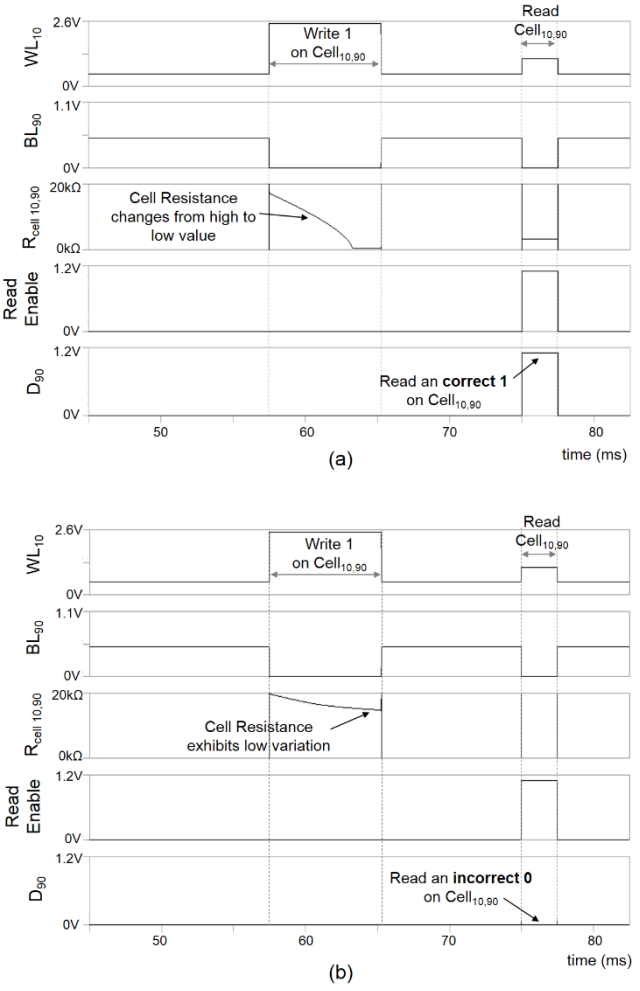

Fig. 3 Simulation results showing the waveforms obtained when first writing a 1, then reading, $cell_{10,90}$ for: a) a fault free memory array; b) a non-selected $cell_{10,70}$ with its selector affected by a short, sharing the same wordline WL_{10} as the selected $cell_{10,90}$.

More in details, Table 1 reports the values of the current (I_{BL70}) flowing through the non-selected $cell_{10,70}$ during a write (of a logic 1) and a read operation of $cell_{10,90}$, sharing the same worline as $cell_{10,70}$, as in the example reported in Fig. 3. Moreover, the table reports the values of the current (I_{BL70}) flowing through the non-selected $cell_{10,70}$, for the cases of non-selected $cell_{10,70}$ with: i) fault-free selector (second row); ii) faulty selector (third row).

TABLE 1
CURRENT FOLOWING THROUGH THE NON-SELECTED CELL10,70 DURING A WRITE AND A READ OPERATION OF A CELL10,90 SHARING THE SAME WORLD LINE, FOR THE CASE OF CELL10,70 WITH FAULT-FREE AND FAULTY SELECTOR.

	Current flowing through non-selected $cell_{10,70}$ I_{BL70}	
	Write (logic 1) of $cell_{10,90}$	Read of $cell_{10,90}$
Fault-free non-selected $cell_{10,70}$	4.8μA	≈ 2 nA
Faulty non-selected $cell_{10,70}$	430μA	80μA
Increase over the fault-free case	≈ 89.6 times	$40x10^3$ times

From Table 1 we can notice that the current flowing through the non-selected $cell_{10,70}$ (I_{BL70}) increases significantly when its selector is affected by a short. In particular, we can see that I_{BL70} increases by approximately 90 times (40.000 times) when its selector is affected by a short, and another $cell_{10,90}$ sharing the same worline is selected to write a logic 1 (for reading $cell_{10,90}$). Such an increase in the current flowing through a cell with its selector affected by a short will be exploited by our proposed detection strategy, described in the following Section.

We have also verified that the number of cells in a wordline that cannot be correctly written depends on the position of the cell whose selector is faulty within the wordline. Fig. 4(a) reports the number of cells in a given wordline that cannot be correctly written, as a function of the position of the cell whose selector is faulty in the wordline.

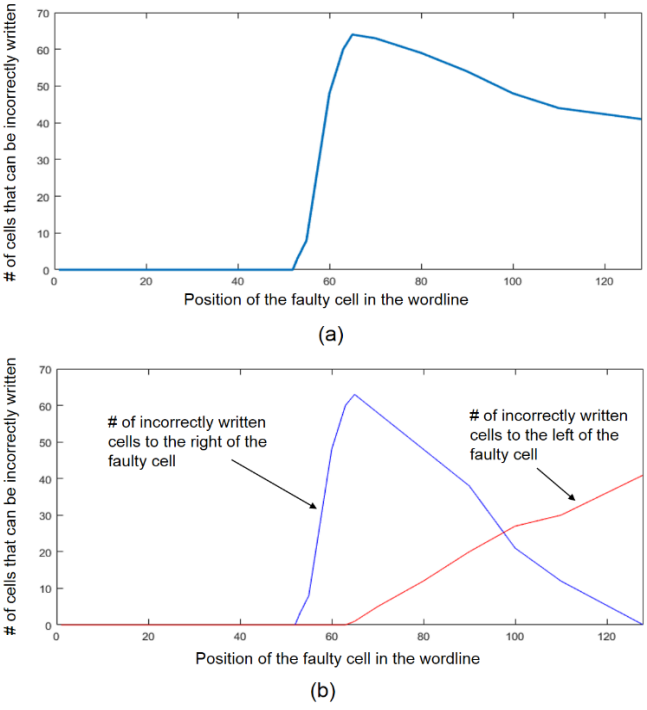

Fig. 4 a) Number of cells per wordline that can not be correctly written, as a function of the position of the cell whose selector is faulty in the wordline; b) number of cells to the right and to the left of the cell whose selector is faulty that can not be correctly written, as a function of the position of the cell whose selector is faulty in the wordline.

As we can notice, the cell can be correctly written if the faulty non-selected cell is within the first 52 cells in the wordline. This because if the cell whose selector is faulty is close to the worline drivers, the voltage drop across the wordline wire resistance is not high enough to prevent correct writes on other cells in the wordline. On the other hand, the number of cells that can not be correctly written (so the number of errors) increases significantly (with up to 64 errors) if the cell whose selector is faulty is beyond the first 52 cells in the wordline (i.e., from cell 53rd to cell 128th). More in details, Fig. 4(b) reports the number of cells to the right, and the number of cells to the left, of a cell whose selector is faulty that cannot be correctly written, as a function of the position of the cell whose selector is faulty in the wordline. As can be seen, the number of errors in cells to the right (left) of the cell whose selector is faulty tends to diminish (increase), as the position of the cell whose selector is faulty increases.

As described before, we have also analyzed the effects of shorts affecting the selectors of ReRAM cells for the case in which the cell whose selector is faulty is selected for write/read operations.

For this case, we have verified that write/read operations are performed correctly on cells, whose selectors are affected by a short. In fact, a fault-free selector of a cell selected for write/read operation is conductive, thus it presents a low on-state resistance. Thus, shorts affecting the selector (with a resistance much lower than the selector on-state resistance) of selected cells do not affect their correct write/read operations.

In addition, we have also analyzed the effects of shorts affecting the selectors of ReRAM cells that share the same bitline as the cell selected for write/read operations.

We have verified that cells sharing the same bitline with a cell whose selector is affected by a short cannot be written correctly. In fact, as discussed before, the large current flowing through the cell whose selector is faulty generates an excessive voltage drop on the parasitic resistance of the bitline wire, which significantly reduces the effective voltage applied across the selected cell, that results lower than that required to change (as desired) the state of the cell resistance.

However, in this case, the inhability to write correctly cells sharing the bitline with a cell whose selector is faulty gives rise to single errors in the ReRAM crossbar array (i.e., only one cell per wordline), which can be corrected by the ECCs usually adopted for memory arrays.

As for the case of a cell selected for write/read operations that shares neither the wordline, nor the bitline with a cell whose selector is faulty, we have verified that they can be correctly read/written.

Finally, we have also verified that a selector failing as an open can generate only single errors in the ReRAM crossbar array, which can be corrected by the ECCs usually adopted for memory arrays.

Therefore, our analyses have shown that a single selector failing as a short may cause up to 64 errors in memory cells sharing the same word line as a cell with a faulty selector. Such a large number of errors exceeds the correction capability of ECCs usually adopted for memories. Thus, new solutions to enable to tolerate the large number of errors caused by shorts affecting selectors of ReRAMs are needed.

4 Detection Scheme

In this Section, we propose a low-cost approach to detect short faults affecting selectors of ReRAMs, and to identify the bitline containing the cell with the faulty selector. Such a bitline can then be properly deactivated and replaced by a spare one, in order to guarantee the memory correct operation in the field.

The basic idea of the proposed scheme is to monitor the current flowing through each bitline (BL_j) of the crossbar

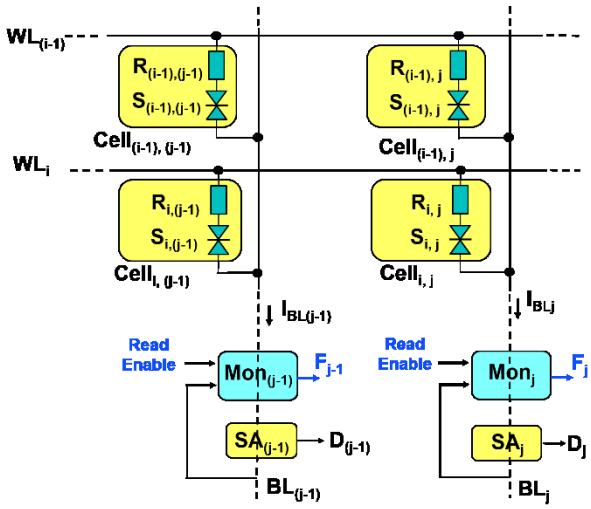

Fig. 5. Schematic representation of our proposed scheme to detect shorts affecting selectors of ReRAMs in crossbar arrays.

array during read operations, and to compare it with a proper threshold current (I_{TH}), to identify the presence of shorts affecting selectors. A schematic representation of the proposed approach is shown in Fig. 5.

It consists in adding a monitoring circuit (Mon_j) to each bitline (BLj) of the ReRAM crossbar array (Fig. 1).

In particular, during read operations (i.e., while Read Enable signal is equal to 1), the monitors connected to the bitlines of cells not selected for reading (i.e., bitlines with a BLj voltage equal to 0.55V) compare the current flowing through the bitline (I_{BLj}) with the threshold current I_{TH}.

If $I_{BLj} > I_{TH}$, the monitor generates a fault indication (Fj=1) to indicate the presence of a short affecting the selector of a (non selected) cell in the bitline BLj. As suggested in [2], after a cell whose selector is faulty is identified on a bitline BLj, all cells on that bitline can be put into a high resistance state (included the faulty one), to avoid incorrect write operations in other cells. Then bitline BLj can be properly deactivated and replaced by a spare one, in order to guarantee the memory correct operation in the field.

Otherwise, if $I_{BLj} < I_{TH}$, the monitor keeps Fj=0, indicating the absence of cells whose selectors are faulty in the monitored BLj.

As for the value of I_{TH}, it should be chosen to be an intermediate current value between those reported in Table 1, for non-selected cells during read operations (i.e., 2nA < I_{TH} < 80μA).

In order to avoid false alarms (i.e., the erroenous generation of fault indications), the monitors connected to the bitlines of cells selected for reading (i.e., bitlines with voltage applied to BLj equal to 0V) should be disabled during read operations. In fact, the current flowing though selected cells may be higher than 80μA (thus higher than I_{TH}), also when reading a cell whose selector is fault-free. However, as discussed in the previous Section, shorts affecting selectors of the cells selected for read/write operations, do not affect the correct read/write operation.

As an example, the monitoring circuits (Mon_j) of our approach could be simply implemented by properly modifying the current sense aplifiers shown in Fig. 2.

5 Conclusions

Resistive Random Access Memories (ReRAMs) are amongst the most promising candidates to replace silicon-based memories in the near future, when huge amount of data have to be stored. However, ReRAMs suffer from reliability issues associated to faults affecting both their resistive elements, and their selectors. While some solutions have been presented in literature to detect, or tolerate, faults affecting the resistive element, so far no solution has been yet proposed to detect, or tolerate, faults affecting the selector, albeit these faults have been proven to be likely and possibly compromising the reliability of ReRAMs. In this paper, we have analyzed the effects of the most likely faults (i.e., shorts and opens) possibly affecting the selectors of ReRAM cells on the operation of the crossbar memory array. We have shown that a selector failing as a short can give rise to numerous errors in the ReRAM crossbar array. As an example, for the case of a crossbar array of 128x128 cells, we showed that a single selector failing as a short may cause up to 64 errors in memory cells sharing the same word line of the cell containing the faulty selector. Such a large number of errors exceeds the correction capability of ECCs usually adopted for ReRAM arrays. Therefore, new solutions enabling to tolerate the large number of errors caused by selector faults in crossbar arrays are needed, to enable the use of this kind of promising memories for all applications mandating the ability to store huge amount of data, in a reliable way. Then, we have introduced a possible approach to detect short faults affecting selectors of ReRAMs and to identify the bitline containing the faulty cell. Such a bitline can then be properly deactivated and replaced by a spare one, in order to guarantee the memory correct operation in the field.

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