Investigation of the Impact of BTI Aging Phenomenon on Analog Amplifiers

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Marco Grossi, Martin Omaña
Department of Electrical, Electronic and Information Engineering "Guglielmo Marconi", University of Bologna, Bologna, Italy (Tel. 0039-0512093038, marco.grossi8@unibo.it, martin.omana@unibo.it)

Abstract
CMOS technology scaling allows the design of even more complex system but, at the same time, introduces some reliability problems. In particular, aggressively scaled microelectronic technologies are affected by the Bias Temperature Instability (BTI) aging phenomenon that results in an increase of the absolute value of the transistors threshold voltage with aging time and a consequent reduction for the microelectronic circuit reliability. In this paper we estimate the performance degradation caused by BTI on an operational amplifier (OPAMP) in open loop configuration as well as on three remarkable analog amplifiers based on OPAMPs. The results have shown that BTI can seriously impact the performance of the investigated circuits, and that such performance degradation worsens as operating temperature increases. We also briefly describe a possible low-cost monitoring scheme to detect the performance degradation of the OPAMPs caused by BTI. The effectiveness of our monitor has been validated by means of pre-layout electrical simulations, and the results have shown that it can be reliably used to evaluate the OPAMPs aging degradation.

Keywords BTI; Aging; Reliability; Analog Amplifiers; Operational Amplifiers.

1. INTRODUCTION

The aggressive scaling of CMOS technology has enabled significant increase of the complexity of Systems on a Chip (SoCs) and of Programmable Systems on a Chip (PSoCs) in the recent years. As a consequence, SoCs and PSoCs are being employed always in an ever large number of applications (i.e., smartphones, autonomous vehicles, etc.) [1]. Modern SoCs and PSoCs process both analog and digital signals within the same semiconductor die, making a massive use of operational amplifiers (OPAMPs) and analog amplifiers based on OPAMPs [2].

However, OPAMPs implemented within SoCs and PSoC suffers from the same reliability problems associated with the scaling of the microelectronic technology [2−5]. In particular, aggressively scaled electronics are particularly prone to aging mechanisms, such as Bias Temperature Instability (BTI), which is considered the primary parametric failure mechanism in modern ICs [6−10]. Negative BTI (NBTI) and Positive BTI (PBTI) are observed in *pMOS* and *nMOS* transistors, respectively. They cause performance degradation of MOS transistors, when they are ON. For instance, it has been proven that, due to NBTI, the absolute threshold voltage of *pMOS* transistors can increase by more than 50 mV over ten years [11]. Both NBTI and PBTI were investigated in p-channel and n-channel VDMOSFETs and the mechanisms for the degradation were analyzed [12, 13]. Accurate prediction of transistors threshold voltage shift vs time can be obtained by development of accurate physical models to estimate the interface and oxide traps generated by degradation [14]. Investigations on the BTI degradation effects have been proposed in the case of SRAMs with resistive defects [15] and gate-all-around flip-flops [16]. Different techniques to mitigate BTI that are based on power supply voltage adjustment have been also proposed in literature [17, 18]. In OPAMPs and/or analog amplifiers based on OPAMPs implemented in scaled CMOS technologies, the transistor threshold voltage increase due to BTI can result in a significant variation of important performance parameters (e.g., the amplifier gain, cutoff frequency, output offset voltage, etc.) of the amplifiers, possibly resulting in an incorrect system operation [2, 3].

In the past, some works have analyzed the effects of BTI on key performance parameters of OPAMPs (e.g., those in [3−5]). The work in [3] shows that some parameters of the OPAMPs are very prone to transistor aging. In this regard, the work in [4] presents a scheme to measure the offset voltage degradation in operational amplifiers caused by BTI. The work in [5] presents a modified OPAMP circuit, whose gain can be monitored and calibrated to compensate for NBTI degradation. However, previous works in literature analyze only the effects of BTI on OPAMPs used in open loop configuration, but these works do not analyze the effects of BTI on analog amplifiers based on OPAMPs with negative feedback networks, which are frequently employed in modern SoC and PSoC to elaborate analog signals.

Based on these considerations, in this paper we first analyze the performance degradation caused by BTI on an operational amplifier (OPAMP) in open loop configuration,

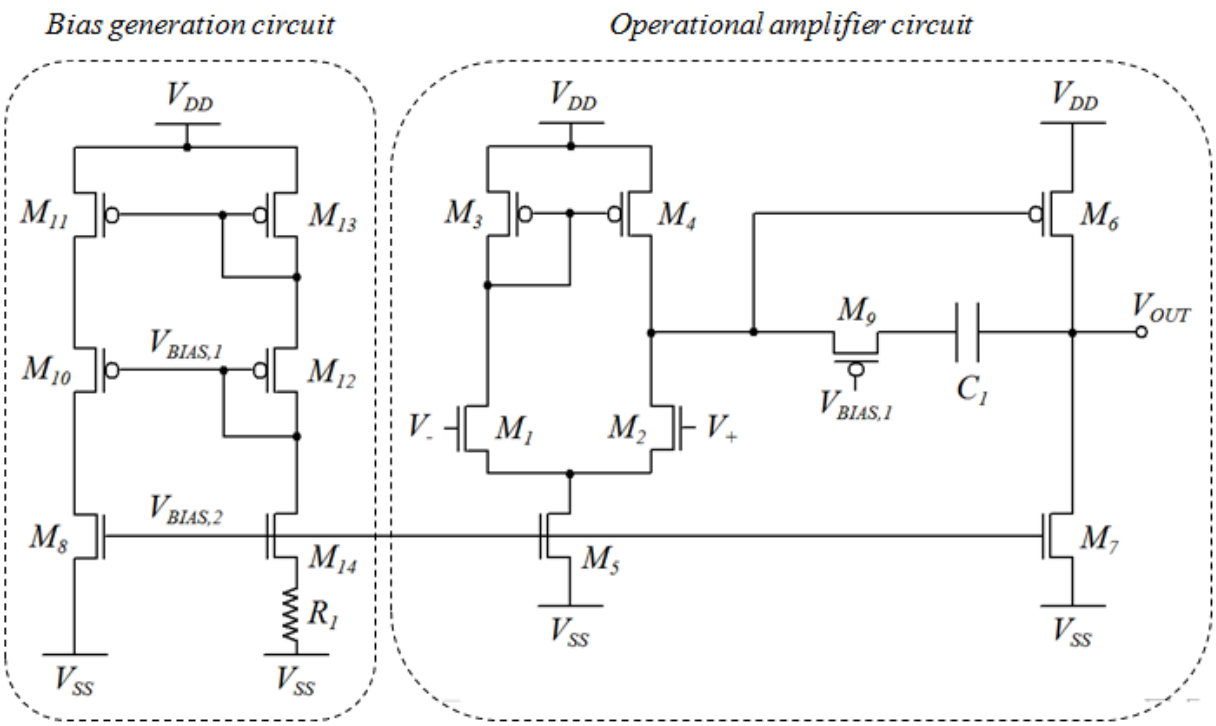

Fig. 1. Schematic of the OPAMP circuit investigated in this work. The circuit has been simulated with the parameters: V_{DD} = 1 V, V_{SS} = −1 V, R_1 = 901 Ω, C_1 = 272.77 fF, M_1 M_2 (L=320 nm W=180 nm), M_3 M_4 (L=200 nm W=1.40 µm), M_5 (L=100 nm W=126 nm), M_6 (L=70 nm w=4.6 µm), M_7 (L=70 nm W=500 nm), M_8 (L=70 nm W=650 nm), M_9 (L=70 nm W=983 nm), M_{10} M_{11} M_{12} M_{13} (L=70 nm W=2 µm), M_{14} (L=70 nm W=1.82 µm).

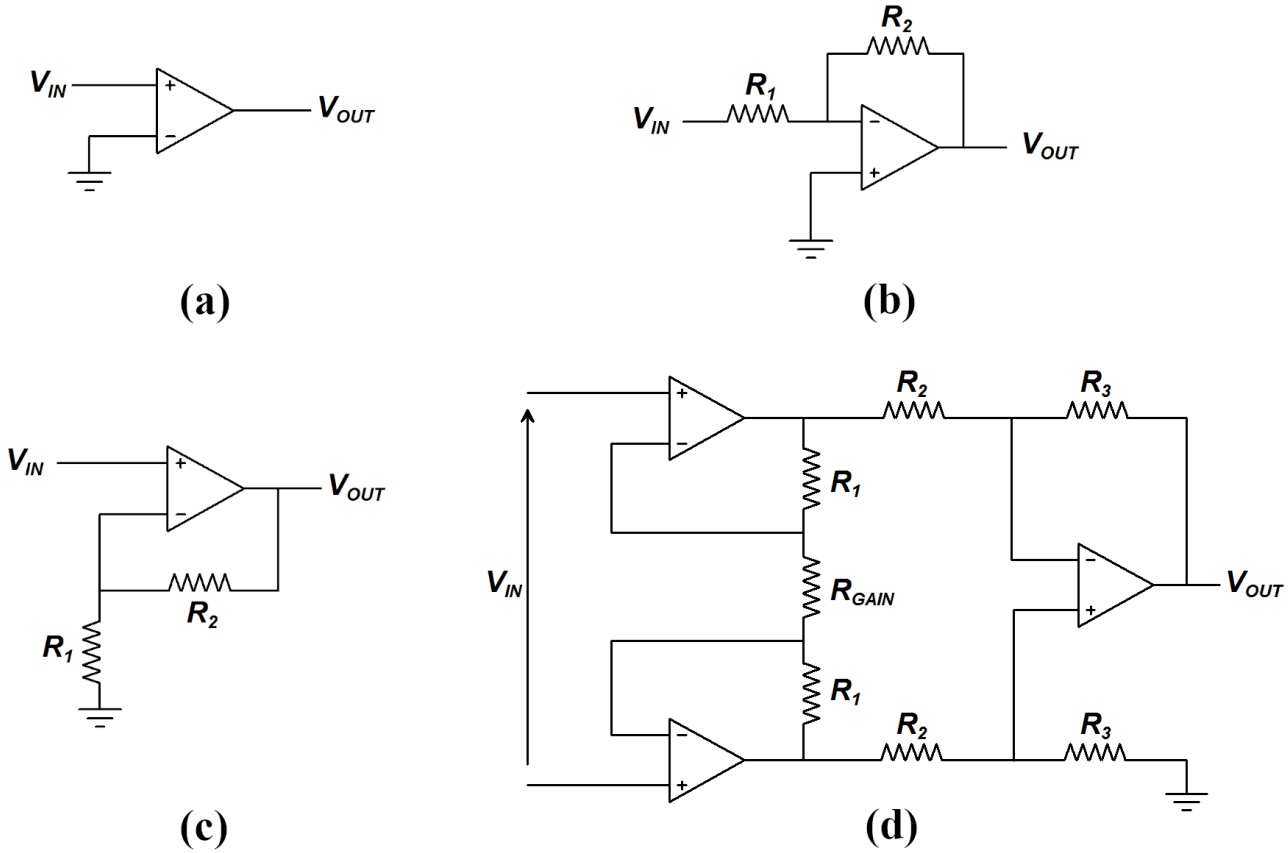

Fig. 2. Schematic representation of the amplifiers considered in our analyses: (a) the OPAMP presented in Fig. 1 in open-loop configuration, used as reference in our analysis; (b) an inverting amplifier; (c) a non-inverting amplifier; (d) a differential instrumentation amplifier.

Table 1. Threshold voltage shifts of the transistors during circuit lifetime caused by BTI degradation.

	$\Delta V_{th,p}$ (mV)			$\Delta V_{th,n}$ (mV)		
Aging time	50 °C	75 °C	100 °C	50 °C	75 °C	100 °C
1 month	30.45	37.34	44.56	15.22	18.67	22.28
3 months	36.32	44.54	53.16	18.16	22.27	26.58
6 months	40.58	49.77	59.39	20.29	24.88	29.70
1 year	45.34	55.60	66.36	22.67	27.80	33.18
3 years	54.05	66.29	79.11	27.03	33.14	39.55
5 years	58.66	71.93	85.85	29.33	35.97	42.92

as well as on three remarkable analog amplifiers based on OPAMPs with negative feedback loops. The results of our analyses have shown that for the case of OPAMPs in open-loop configuration, BTI aging induces a strong reduction (over time) of the DC gain, the cutoff frequency and the slew rate. Moreover, our analyses have shown that such reductions increases with the increase of the operating temperature. On the other hand, for the considered three analog amplifiers based on OPAMPs with negative feedback networks, our analyses have shown that BTI minimally affects their DC gain, but causes a significant degradation of their cutoff frequency and output offset voltage.

Therefore, we also discuss in this paper a possible low-cost monitoring scheme to detect the performance degradation of the OPAMPs caused by BTI.

The remainder of this paper is organized as follows. In Section 2, we describe the simulation setup we employed to evaluate the effects of aging on OPAMPs in open loop configuration and on three remarkable analog amplifiers based on OPAMPs with negative feedback networks. In Section 3, we report some of the results that we obtained by means of the simulations performed by HSPICE, considering the simulation setup discussed in Section 2. In Section 4, we discuss a low cost scheme to detect aging degradation affecting OPAMPs. In Section 5, we present some conclusive remarks.

2. SIMULATION SETUP

We assess the impact of BTI-induced MOS transistor threshold voltage shift on some key parameters of analog amplifiers based on OPAMP. Particularly, by means of HSPICE pre-layout electrical level simulations, we analyze the variations induced by BTI on the gain, the cutoff frequency (f_{-3bB}), the output offset voltage (V_{offset}), and the OPAMP slew-rate as a function of operating time, and for some different operating temperatures.

In our analysis the gain of the amplifiers has been evaluated as the ratio between the output and input voltages obtained for a frequency of the input voltage equal to 0 Hz (e.g. DC condition). The cutoff frequency (f_{-3bB}) of the amplifiers has been evaluated as the frequency of the input voltage for which the output voltage presents a reduction of 3 dB with respect to its voltage value at 0 Hz. The output offset (V_{offset}) has been evaluated as the amplitude of the output voltage obtained when a constant signal with amplitude equal to 0 V is applied to the input of the amplifier. Finally, the slew-rate of the OPAMP has been determined by evaluating the delay in the falling/rising edge of the output voltage when the OPAMP is configured in open-loop configuration, and a step voltage signal is applied to the non-inverting input of the OPAMP.

The internal structure of the OPAMP investigated in this work is schematically represented in Fig. 1, which is the OPAMP presented in [19] with some minor modifications.

The MOS transistors composing the OPAMP have been implemented by using a 32 nm High-K CMOS technology, using a level 54 SPICE model and with ±1 V power supply. The threshold voltage for non-aged transistors (fresh devices) is equal to 493 mV for *nMOS* and −491 mV for *pMOS*. The MOS oxide thickness is 1.65 nm for *nMOS* and 1.75 nm for *pMOS*. The parasitic resistance per unit width (R_{DSW}) is equal to 150 μΩ/m. The considered technology model has been obtained from the Predictive Technology Model (PTM) web site [20].

For our analysis we have considered, as significant case studies, the four analog amplifiers shown in Fig. 2. They are: 1) the OPAMP presented in Fig. 1 in open-loop configuration (Fig. 2(a)), used as reference in our analysis; 2) an inverting amplifier (Fig. 2(b)) using an OPAMP of the kind in Fig. 1; 3) a non-inverting amplifier (Fig. 2(c)) using also an OPAMP of the kind in Fig. 1 and; 4) a differential instrumentation amplifier (Fig. 2(d)) using three OPAMPs of the kind in Fig. 1.

We have implemented the OPAMPs of all considered amplifiers as the OPAMP in Fig. 1. All simulations have been carried out considering a capacitive output load of 1 pF.. The OPAMP in open-loop configuration (Fig. 2(a)) has been investigated for three different operating temperatures (50, 75 and 100 °C) while the analog amplifiers of Fig. 2 (b)-(d) have been investigated for the case of a temperature of 100 °C (worst case scenario). Moreover, for the amplifiers with negative feedback in Figs. 2(b)-(d), we have evaluated the impact of BTI for four different values of the amplifier gain (e.g., we considered a gain equal to 2, 4, 7 and 10), by connecting resistors of proper values.

In order to account for the threshold voltage shifts of the transistors during circuit lifetime caused by BTI degradation, for our analysis we have used the power-law model presented by Fukui et al. [21], based on the reaction-diffusion model [22], with the exponent modified from 0.25 to 1/6 to account for long term degradation effects [23,24]:

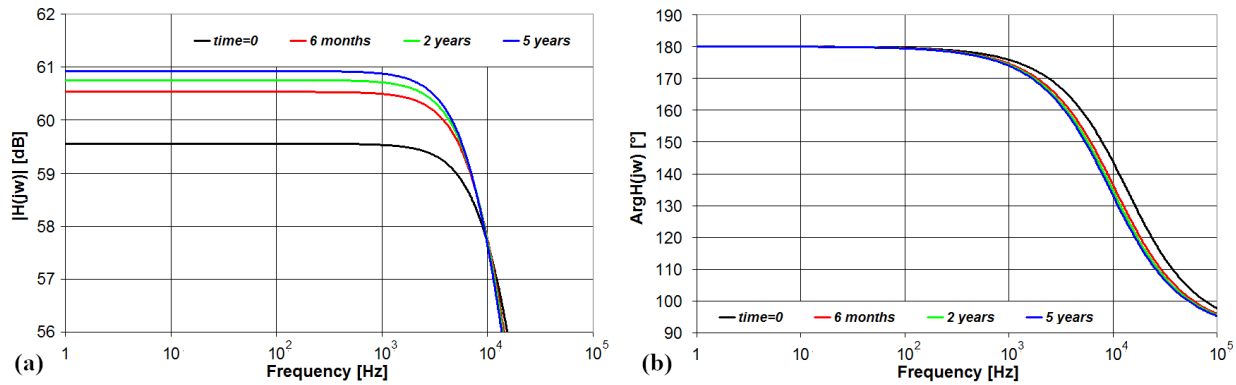

Fig. 3. Simulation results showing the Gain (a) and phase (b) *vs* frequency for the OPAMP in open-loop configuration for an operating temperature of 100 °C and four different aging times.

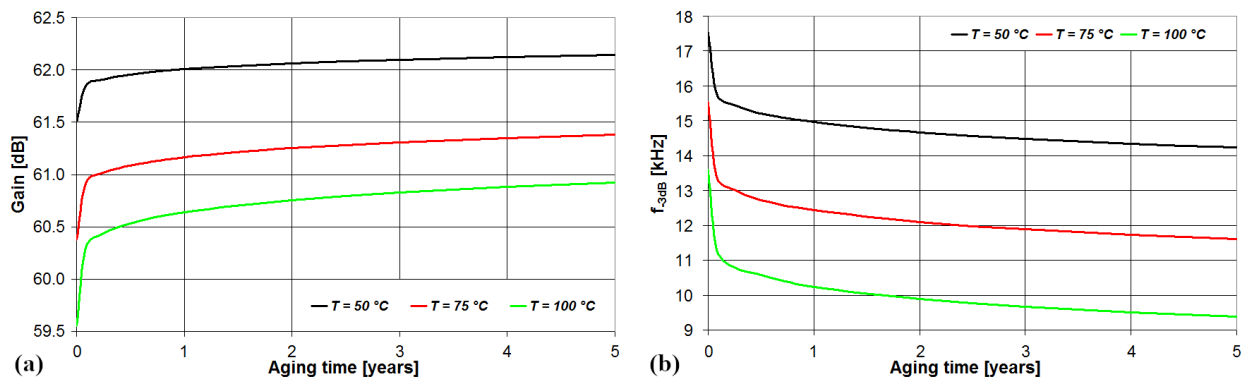

Fig. 4. Simulation results showing (a) the DC gain and (b) the cutoff frequency for the OPAMP in open-loop configuration as function of the aging time, and for three different operating temperatures.

Table 2. Relative variation of DC gain and cutoff frequency for the OPAMP in open loop configuration

	ΔGain (%)			**Δf_{-3dB} (%)**		
Aging time	50 °C	75 °C	100 °C	50 °C	75 °C	100 °C
1 month	4.03	6.42	8.97	10.05	13.74	16.91
3 months	4.81	7.65	10.68	11.90	16.13	20.59
6 months	5.37	8.54	11.92	13.24	18.06	22.29
1 year	5.99	9.53	13.29	14.72	19.93	24.76
3 years	7.13	11.32	15.78	17.43	23.43	28.92
5 years	7.72	12.26	17.09	18.82	25.19	30.98

Table 3. Relative variation of slew rate of the OPAMP in open loop configuration

	ΔSR (%) – rising edge			**ΔSR (%) – falling edge**		
Aging time	50 °C	75 °C	100 °C	50 °C	75 °C	100 °C
1 month	9.27	11.98	14.40	11.10	13.68	16.80
3 months	11.07	14.21	16.92	13.02	16.31	19.98
6 months	12.39	15.75	19.09	14.37	18.16	22.34
1 year	13.87	17.44	21.29	15.93	20.14	24.78
3 years	16.65	21.14	25.28	18.75	23.93	28.97
5 years	18.08	22.86	27.37	20.26	25.71	31.35

Table 4. Output offset for the OPAMP in open loop configuration

	Output offset (μV)		
Aging time	50 °C	75 °C	100 °C
0	14.99	-30.42	-60.81
1 month	6.49	-34.84	-61.46
3 months	4.96	-35.60	-61.50
6 months	3.89	-36.12	-61.51
1 year	2.71	-36.69	-61.50
3 years	0.61	-37.67	-61.40
5 years	-0.46	-38.15	-61.31

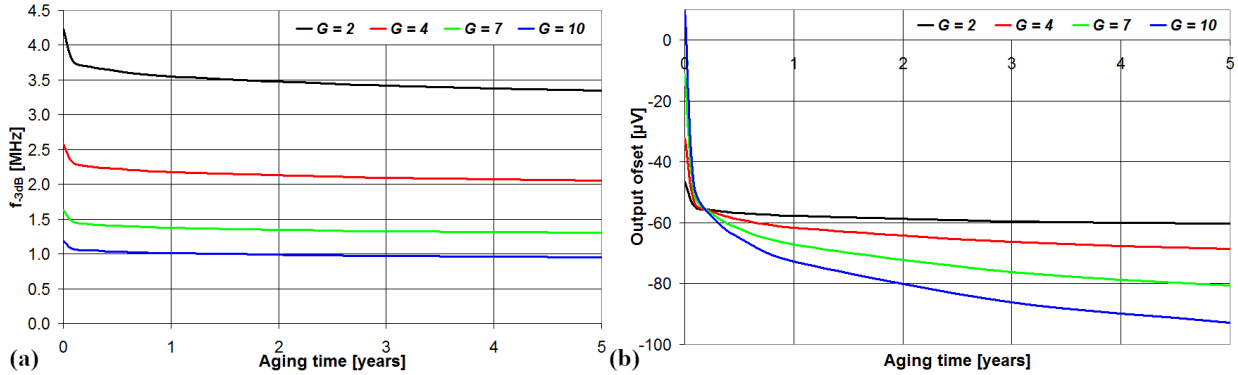

Fig. 5. Simulation results showing (a) the cutoff frequency and (b) the output offset voltage as function of the aging time for the inverting amplifier represented in Fig. 2 (b), for four different amplifier Gains (G) and an operating temperature of 100 °C.

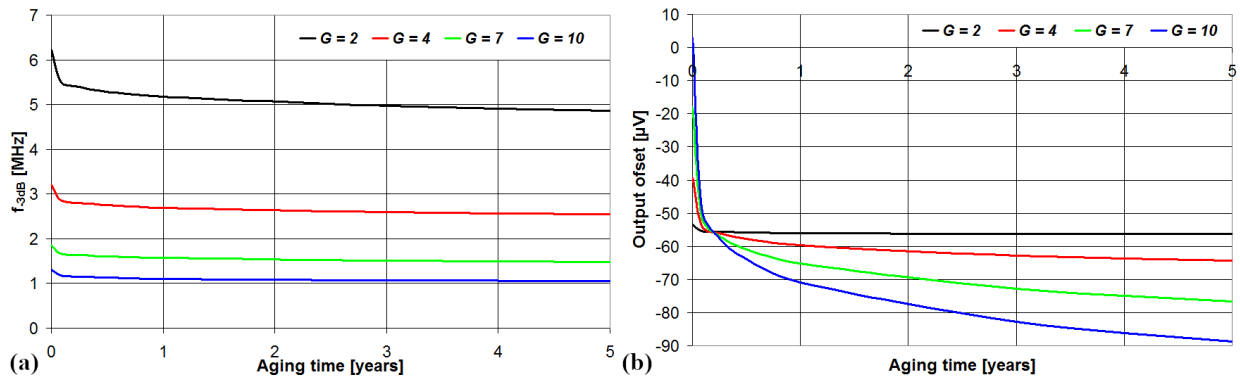

Fig. 6. Simulation results showing (a) the cutoff frequency and (b) the output offset voltage as function of the aging time for the non-inverting amplifier represented in Fig. 2 (c), for four different amplifier Gains (G) and an operating temperature of 100 °C.

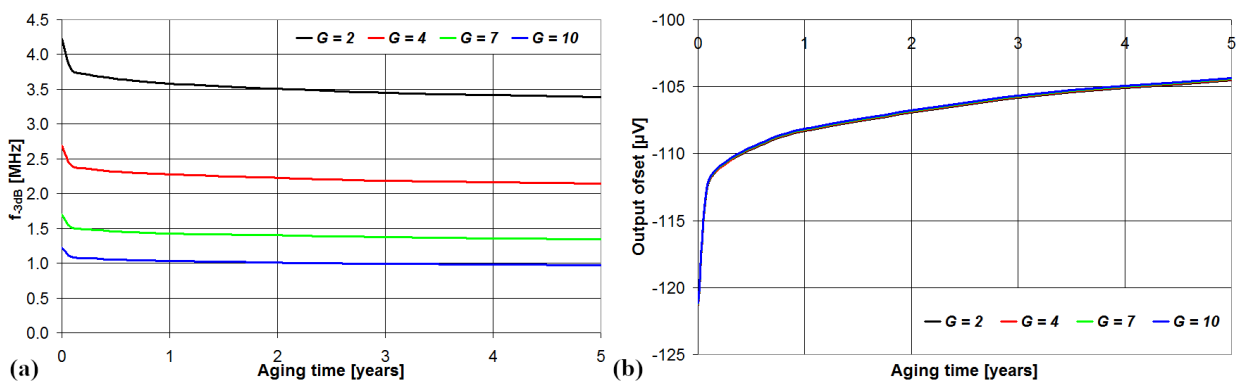

Fig. 7. Simulation results showing (a) the cutoff frequency and (b) the output offset voltage as function of the aging time for the differential instrumentation amplifier represented in Fig. 2 (d), for four different amplifier Gains (G) and an operating temperature of 100 °C.

$$\Delta V_{th} = \chi \cdot K_{lt} \cdot \sqrt{C_{ox} \cdot (V_{dd} - V_{th})} \cdot e^{-\frac{E_a}{kT}} \cdot (\alpha \cdot \Delta t)^n \quad (1)$$

where χ is 1 for pMOS transistors, and 0.5 for nMOS transistors [25-27], K_{lt} has been estimated as $2.7V^{1/2}F^{-1/2}s^{-1/6}$ for a 32nm High-K CMOS technology by fitting the model in [22] with the experimental results presented in [28], C_{ox} is the oxide capacitance, E_a is the interface traps activation energy ($E_a \approx 0.8$eV [29]), k is the Boltzmann constant, n is a fitting parameter equal to 1/6, T is the temperature (in °K), Δt is the total circuit operating time since chip initial operation and α is the fraction of time, over Δt, during which the transistor is under stress condition (i.e., conductive). Moreover, we have evaluated the effects of the increase in the absolute value of the *n/pMOS* threshold voltage (ΔV_{th}) induced by BTI degradation for an operating time Δt ranging from 0 to 5 years as a realistic scenario, and for the three different operating temperatures (50 °C, 75 °C and 100 °C). The considered threshold voltage shifts for the *n/pMOS* transistors are reported in Table 1.

3. Results and Discussion

In this Section, we report some of the results that we obtained by means of HSPICE simulations, considering the simulation setup discussed in Section 2. First, the OPAMP

in open-loop configuration has been investigated and the results presented in Subsection 3.A. Then the analog amplifiers of Fig. 2 (b)-(d) have been investigated and the results presented in Subsection 3.B.

A. Impact of BTI on OPAMPs in open-loop configuration

The operational amplifier (OPAMP) in open loop configuration in Fig. 2 (a) has been simulated for the case of a sine waveform with frequency ranging from 1 Hz to 1 GHz applied at the input V_{IN}. The obtained Bode plots are reported in Fig. 3, for the case of an operating temperature 100 °C and for four different operating times (*Δt = 0, 6 months, 2 and 5 years*). As can be seen, the DC gain increases with the increase of operating time, while the cutoff frequency f_{-3dB} (i.e. the frequency where the gain is reduced by 3 dB with respect to the DC gain) decreases with the increase of operating time.

Moreover, Figs. 4(a) and 4(b) report the gain and the cutoff frequency f_{-3dB}, respectively, of the OPAMP in open-loop and as function of the operating time *Δt*, for three different operating temperatures (50 °C, 75 °C and 100 °C). As can be noted, both the DC gain and the cutoff frequency of the open-loop amplifier present a non-negligible variation over the considered circuit lifetime, as well as with the increase of the operating temperature.

More in details, Table 2 reports the relative variation of the DC gain and the cutoff frequency with operating time and temperature. As expected, the BTI degradation increases for higher operating temperatures. In particular, after 5 years the DC gain increases by 7.72 % for a temperature of 50 °C and by 17 % for a temperature of 100 °C. Similarly, after 5 years the cutoff frequency decrease by 18.82 % and 30.98 % for an operating temperature of 50 °C and 100 °C, respectively. The increased variation of the OPAMP DC gain and cutoff frequency with temperature increase can be explained by the fact that, as shown in Table 1, the shift of the transistor's threshold voltage (due to BTI) over time increases with temperature increase. Thus, being the BTI degradation higher for higher temperatures, we consequently obtain, over time, a stronger OPAMP parameter deviations for higher temperatures.

In addition, we have also evaluated the impact of BTI on the slew rate (SR), both rising and fall edges, of the OPAMP in open-loop configuration. The simulations have been performed by applying at the input of the OPAMP a voltage step and measuring the slope of the output voltage within the range -0.6 V and 0.6 V.

The relative variations of the SR for some remarkable operating times *Δt* and three different temperatures are reported in Table 3. As can be seen, the SR increases with operating time, and the variations in both the rising and falling edges are similar. Moreover, as expected, we can see that the impact of BTI on the SR is more severe at higher temperatures.

Finally, we have also evaluated the impact of BTI on the output offset of the OPAMP in open-loop configuration. This evaluation has been performed by setting the input voltage V_{IN} to 0 V DC, and observing the voltage present at the output of the amplifier. The obtained output offset values for some remarkable operating times *Δt* and three different temperatures are presented in Table 4. As can be seen, the output offset significantly varies with the operating temperature, from approximately 15 mV for 50 °C to approximately -60 mV for 100 °C. In addition, we can observe that the output offset also varies over circuit lifetime, and that such a variation reduces as the operating temperature increases: the absolute variations of the output offset are approximately 15.4 mV (0.5 mV) after *Δt*=5 years at a temperature of 50 °C (100 °C).

B. Impact of BTI on Analog amplifiers based on OPAMPs with negative feedback

The analog amplifiers based on OPAMPs with negative feedback in Fig. 2 (i.e. inverting amplifier, non-inverting amplifier and differential instrumentation amplifier) have been simulated for an operating time between 0 and 5 years, considering an operating temperature 100 °C that represents the worst case scenario. For each amplifier we have evaluated the impact of BTI on the DC gain, the cutoff frequency and the output offset voltage. As anticipated in Section 2, we have considered as an example four different DC Gain values for the amplifiers (i.e., equal to 2, 4, 7 and 10), which have been obtained by properly designing the resistors of the feedback loop.

In particular, the DC gain of the three amplifiers with negative feedback presents a negligible variation (i.e., smaller than 0.2 %) over the whole considered circuit lifetime *Δt,* as opposed to the open loop amplifier where a worst case variation of 17.1 % was found after 5 years. This result can be somehow expected, since the gain of amplifiers with negative feedback is approximately given by the values of the resistors composing the feedback loop, which are not affected by BTI degradation.

The absolute values of the cutoff frequency and output offset of the inverting amplifier, the non-inverting amplifier and the differential instrumentation amplifier are presented in Fig. 5, Fig. 6 and Fig. 7, respectively.

As can be seen, the cutoff frequency of the three considered amplifiers with negative feedback presents a significant variation during the circuit lifetime, with a higher variation during the first months of operation. We can also observe that the variation exhibited in the cutoff frequency increases as the gain of the amplifiers reduces. This can be explained by the fact that for the case of amplifiers with negative feedback networks, the product gain-bandwidth is constant, thus lower values of DC gains result in higher values of cutoff frequencies, and also its variations.

In addition, from Fig. 5(b) and 6(b) we can see that for the inverting and non-inverting amplifiers, the offset voltage significantly varies during circuit lifetime, and that such a variation strongly depends on the DC gain value. On the other hand, from Fig. 7(b) we can observe that the offset

Table 5. Relative variation of cutoff frequency and output offset variation for the inverting amplifier.

	Δf_{-3dB} (%)		Output offset variation (µV)	
Aging time	G = 2	G = 10	G = 2	G = 10
1 month	10.82	10.23	8.12	57.75
3 months	12.97	12.23	9.50	67.89
6 months	14.47	13.75	10.46	75.00
1 year	16.22	15.41	11.47	82.69
3 years	19.42	18.45	13.18	96.08
5 years	21.09	20.01	14.01	102.78

Table 6. Relative variation of cutoff frequency and output offset variation for the non-inverting amplifier.

	Δf_{-3dB} (%)		Output offset variation (µV)	
Aging time	G = 2	G = 10	G = 2	G = 10
1 month	11.29	10.33	1.86	51.59
3 months	13.52	12.29	2.14	60.64
6 months	15.08	13.77	2.32	66.88
1 year	16.92	15.42	2.49	73.84
3 years	20.22	18.40	2.74	85.78
5 years	21.97	20.08	2.82	91.75

Table 7. Relative variation of cutoff frequency and output offset variation for the instrumentation amplifier.

	Δf_{-3dB} (%)		Output offset variation (µV)	
Aging time	G = 2	G = 10	G = 2	G = 10
1 month	10.24	10.56	-8.83	-8.82
3 months	12.29	12.63	-10.49	-10.48
6 months	13.73	14.05	-11.69	-11.68
1 year	15.35	15.79	-13.03	-13.02
3 years	18.41	18.87	-15.50	-15.49
5 years	20.04	20.50	-16.81	-16.80

voltage of the instrumentation amplifier also varies significantly during circuit lifetime, but the variation does not depend on the amplifier gain value.

This behavior can be explained by considering the equation giving the amplifier output offset ($V_{OUT,OFFSET}$) as function of the OPAMP offset voltage (v_{OS}), which is reported in equation (2) for the inverting and non-inverting amplifiers (Figs. 2 (b) and (c), respectively), and in equation (3) for the differential instrumentation amplifier (Fig. 2 (d)):

$$V_{OUT,OFFSET} = -\left(1+\frac{R_2}{R_1}\right)v_{OS} \quad (2)$$

$$V_{OUT,OFFSET} = -\frac{R_3}{R_2}\left(1+\frac{2R_1}{R_{GAIN}}\right)\left(v_{OS,2}-v_{OS,1}\right)-\left(1+\frac{R_3}{R_2}\right)v_{OS,3} \quad (3)$$

For the case of the inverting and non-inverting amplifiers, the DC gain is given by the ratio R_2/R_1. Thus, if we increases the DC gain we consequently also increase the amplifier output offset.

Instead, for the case of the differential instrumentation amplifier, the DC gain is given by the value of the resistance R_{GAIN}. As can be seen, in equation (3) R_{GAIN} appears only in the first term on the right hand side, which is theoretically equal to 0, since $V_{OS,1}$ and $V_{OS,2}$ compensate each other. Instead, R_{GAIN} is not present in the second term of equation (3). This way, the variation of the output offset of the differential instrumentation amplifier as a function of the DC gain results negligible.

More in details, Tables 5, 6 and 7 reports the relative variations of the cutoff frequency and absolute variation of the output offset voltage for some representative circuit lifetimes, and for the minimum and maximum amplifier gains considered in Figs. 5, 6, and 7 (i.e., for G=2 and G=10).

From the tables, we can observe that the cutoff frequency of the three amplifiers presents a variation of up to approximately 20% over the considered circuit lifetime. Therefore, we can conclude that BTI minimally impacts the gain of amplifiers based on OPAMPs with negative feedback, but it causes significant variation on the values of the cutoff frequency of such amplifiers.

From Tables 5, 6 and 7 we can also observe that the variations of the offset voltage during circuit operation can be of up to 100 µV (14 µV) for the inverting amplifier and up to 92 µV (3 µV) for the non-inverting amplifiers for a gain G=10 (G=2). Meanwhile, for the differential instrumentation amplifier the absolute values of the output offset are higher (> 100 µV) than the inverting and non-inverting amplifiers but its variation is smaller (about 17 µV) and independent on the amplifier gain.

4. Possible Detection Strategy

The results presented in Section 3 have shown that BTI induces a significant variation on the value of some key parameters of OPAMPs, consequently also on the value of key parameters of analog amplifiers using OPAMPs with negative feedback.

In this section, we discuss a possible simple scheme to detect BTI degradation affecting OPAMPs. Our scheme can be activated either at system start-up, or periodically during in-field operation, at time intervals while the circuit containing the OPAMP to be tested is not performing any useful operation.

Our detection strategy activates an alarm signal when the performance degradation (due to BTI) of the OPAMP being tested exceeds a predefined threshold value (T_x). Our scheme is schematically represented in Fig. 8 (a).

In particular, when our detection strategy is activated, the OPAMP under test (OP_{TEST}) is disconnected from the other components of the analog amplifier (i.e., feedback network) and connected in an open loop configuration, with the inverting input connected to GND and the non-inverting input connected to the input signal (IN) of our detection scheme. The disconnection (connection) from (to) the

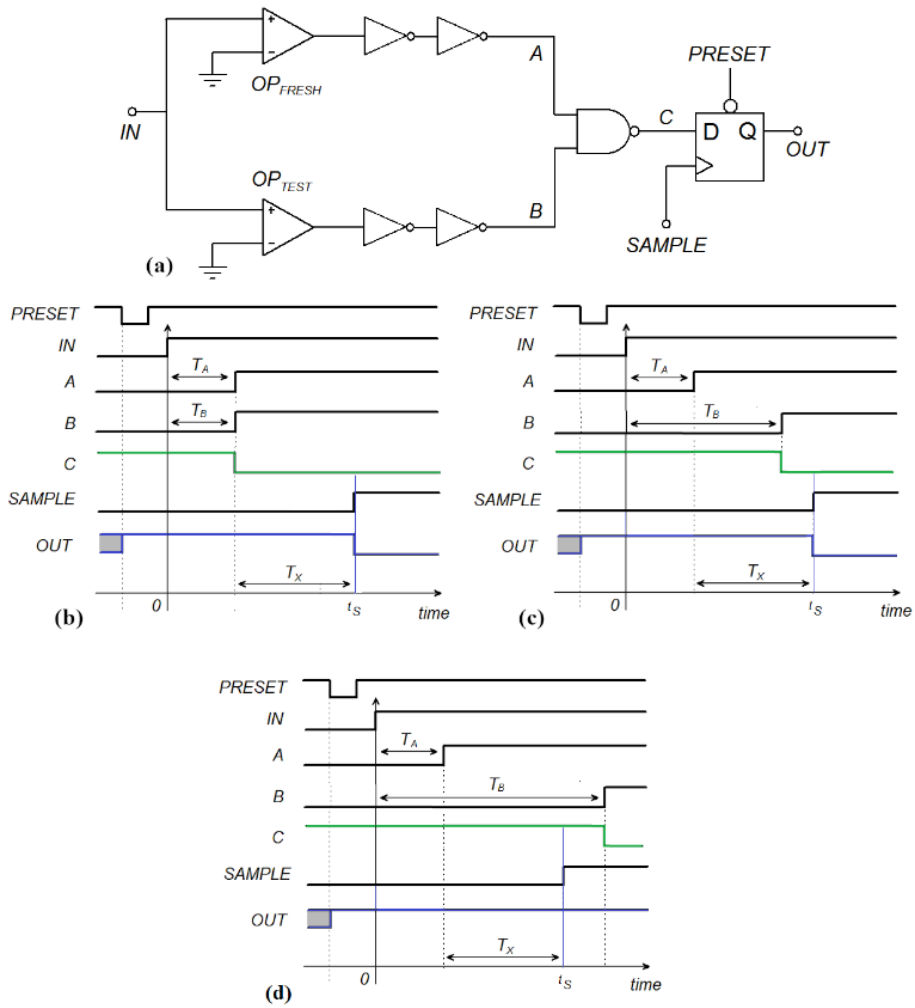

Fig. 8. Schematic representation of: (a) our proposed scheme to detect OPAMP BTI performance degradation over time; (b) the timing of our scheme for the case of OP_{TEST} without performance degradation; (c) the timing of our scheme for the case of OP_{TEST} with a performance degradation lower than the threshold T_x; (d) the timing of our scheme for the case of OP_{TEST} with a performance degradation higher than the threshold T_x.

components of the analog amplifier (our strategy) is performed by MOS transistors used as switches, which are not illustrated in Fig. 8(a) for clarity. In the simulations, the switches have been implemented with ideal characteristics (short circuit when closed/ON, open circuit when open/OFF) and not affected by aging, thus they do not impact the system performance. Our scheme uses also another OPAMP (OP_{FRESH}) that is powered on only during the time intervals when our detection scheme is activated. Thus, we can reasonably assume that OP_{FRESH} is minimally affected by BTI, since the amount of time during which OP_{FRESH} is powered on is negligible compared to the total circuit operating time.

More in details, when our scheme is activated the outputs of OP_{FRESH} and OP_{TEST} are connected to two NOT chains composed by two cascaded (min-sized) NOTs. As represented in Fig. 8(a), the output of the NOT chain (node A) at the output of OP_{FRESH} and the output of the NOT chain (node B) at the output of OP_{TEST} are given as input to a NAND gate. Finally, our scheme includes a D flip-flop that samples the output of the NAND (node C) at the rising edge of a signal SAMPLE (i.e., by generating a pulse on SAMPLE as discussed later in this section). The output of the flip-flop (OUT) is also the output of our detection scheme. It is worth noticing that, as for the NOTs in the NOT chains, also the NAND and the D flip-flop (DFF) are minimally affected by aging, since they are powered on only during the short time intervals during which our strategy is activated.

A representation of the timing of our scheme is illustrated in Fig. 8(b)-8(d). In particular, Fig. 8(b) shows the timing for the case of a fresh OP_{TEST}, Fig. 8(c) shows the timing for the case of OP_{TEST} with a performance degradation lower than the threshold T_x, and Fig. 8(d) shows the timing of our scheme for the case of OP_{TEST} with a performance degradation higher than the threshold T_x.

As can be seen, when our scheme is activated a negative pulse of short duration is applied to signal PRESET, which sets the output OUT to 1. After the application of the PRESET pulse, a transition 0 → 1 is applied at the input IN and the output of the NAND (node C) is sampled at the rising edge of signal SAMPLE (time t_S).

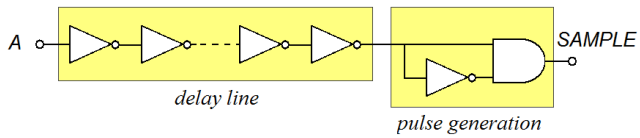

Fig. 9. Schematic representation of a possible circuit to generate the SAMPLE signal.

Table 8. Pulse width $T_B - T_A$ as function of the aging time.

Aging time	Pulse width (ns)		
	50 °C	75 °C	100 °C
0	0	0	0
1 month	4.75	7.57	11.24
3 months	5.78	9.25	13.8
6 months	6.55	10.51	15.74
1 year	7.43	11.97	18.01
3 years	9.13	14.8	22.43
5 years	10.06	16.37	24.93

For the case of a fresh OP_{TEST} (Fig. 8(b)) the propagation delays from IN to A (T_A) and IN to B (T_B) are approximately the same, since both OP_{TEST} and OP_{FRESH} are not degraded. In fact, it is:

$$T_A = T_{NOT\_CHAIN} + T_{OP\_FRESH}, \quad (4)$$

$$T_B = T_{NOT\_CHAIN} + T_{OP\_TEST}, \quad (5)$$

Therefore, the output of the NAND (node C) flips to 0 before the sampling instant t_S, and DFF samples OUT=0, thus indicating that the performance degradation of OP_{TEST} is lower than the threshold T_x.

On the other hand, Fig. 8(c) shows the case of OP_{TEST} with a performance degradation lower than the threshold T_x. As can be observed, due to the degradation on OP_{TEST} the transition 0→1 of signal B is now delayed with respect to the transition of signal A. However, the performance degradation is lower than the threshold T_x. Therefore, as in the previous case, the output of the NAND (node C) flips to 0 before the sampling instant t_S, and DFF samples OUT=0, thus indicating that the performance degradation of OP_{TEST} is lower than the threshold T_x.

Finally, Fig. 8(d) shows the case of OP_{TEST} with a performance degradation higher than the threshold T_x. In this case, due to the degradation on OP_{TEST} the transition 0→1 of signal B and consequently the transition 1→0 of signal C take place after the sampling instant t_S. Therefore, in this case the DFF samples OUT=1, thus indicating that the performance degradation of OP_{TEST} exceeds the threshold T_x.

As for the SAMPLE signal, it can be simply generated by means of a programmable delay line and a pulse generation circuit, as schematically represented in Fig. 9. The delay line should be non-inverting, and with a propagation delay equal to the desired threshold T_x.

As can be seen from Fig. 9, following a 0→1 transition on signal A, a 0→1 transition at the output of the delay line takes place after a delay T_x, and consequently a pulse is generated at the output of the pulse generation circuit (i.e., SAMPLE signal). The duration of the pulse is equal to the propagation delay of the NOT inside the pulse generation circuit. The delay T_x can be programmed to different values by changing the number of NOT gates in the circuit of Fig. 9. This enables to adapt the delay T_x to any desired level of degradation, and makes the proposed detection scheme scalable for different technologies, which are characterized by different aging degradation thresholds.

In order to evaluate the effectiveness of our approach, we have performed simulations for aging times up to 5 years and three different operating temperatures (50, 75 and 100 °C). The observed delay between the rising edges of A and B, i.e. $T_B - T_A$ (in ns), as function of the aging time and temperature is presented in Table 8.

For the detection scheme to operate correctly, the duration of $T_B - T_A$ must be characterized as function of the aging time and operating temperature. Thus, a temperature sensor must be integrated on the device and the duration of T_x must be set depending on the measured temperature value by a suitable choice of the number of NOT gates in the circuit of Fig. 9, as discussed before. According to the simulations, the delay $T_B - T_A$ is function of both the operating temperature and aging time and can be modeled with the function:

$$T_B - T_A = \alpha_T \cdot (\Delta t)^{1/6} + \beta_T, \quad (6)$$

where Δt is the aging time in years and α_T and β_T are temperature dependent parameters. By modeling α_T and β_T as a linear function of temperature ($R^2 = 0.994$) it is:

$$\alpha_T = 0.2258 \cdot T - 65.597, \quad (7)$$

$$\beta_T = 0.0104 \cdot T - 3.2302, \quad (8)$$

The corresponding error in the estimated $T_B - T_A$ has an average value lower than 1 fs, and a standard deviation of 0.519 ns. Thus, using the equations (6) - (8) the delay for the rising edge of the signal SAMPLE can be accurately determined for a given desired threshold T_x and circuit operating temperature.

The proposed detection scheme can be easily implemented on SoCs and PSoCs realized with a microcontroller or FPGA. The main advantages of these implementations are reduced costs and the presence of a temperature compensation, this later enabling to perform accurate in-situ OPAMP aging monitoring. In fact, the dependence of the delay threshold T_x *vs.* temperature can be taken in account by storing a set of values in a look-up-table (LUT) inside the microcontroller/FPGA integrated memory. The values inside the LUT can be defined at the production level thus giving the system a great flexibility to be adapted to analog circuits designed using different technologies. The possibility to change the number of NOT gates in the

pulse generation circuit of Fig. 9 allows to define a set of potential thresholds T_x to monitor the level of degradation of the device under test.

5. CONCLUSIONS

We have investigated the effect of Bias Temperature Instability (BTI) aging phenomenon on the performances of operational amplifiers (OPAMPs) as well as of OPAMPs based analog amplifiers.

The results have shown that, for the case of OPAMPs in open-loop configuration, the DC gain, cutoff frequency and slew rate are significantly degraded by BTI aging, with the degradation increasing with operating temperature increase. In case of analog amplifiers based on OPAMPs with negative feedback network, the DC gain is almost unaffected by the aging phenomenon while the cutoff frequency presents a significant degradation.

We have then presented a simple scheme that is able to detect when OPAMP degradation reaches a desired threshold value. Such detection scheme has been validated with simulations and the results have shown that OPAMP aging degradation can be accurately detected.

DATA AVAILABILITY

Data are available on request from the authors.

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