Hall-Effect Current Sensors: Principles of Operation and Implementation Techniques

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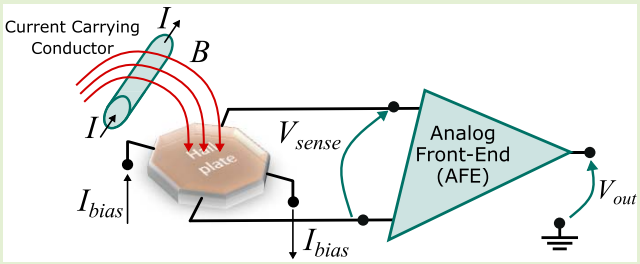
***Abstract*—Isolated current sensing is fundamental in several contexts, including power electronics, automotive, and smart buildings. In order to meet the requirements of modern applications, current sensors should feature ever larger bandwidth and dynamic range, as well as reduced power consumption and dimension. Among the available current sensing technologies, Hall-based current sensors have gained an increased popularity owing to their advantages in terms of size, economic feasibility, low power consumption, high dynamic range, and integrability with standard CMOS technologies. This tutorial aims at providing a comprehensive insight into the interdisciplinary world of Hall-effect current sensors, encompassing the fundamental principles of operation, the design of the semiconductor device, the implementation techniques, as well as the methods for sensor modeling and characterization. In particular, this manuscript focuses on Hall-effect sensors realized on standard silicon technologies, and it reviews some typical architectures for the transduction of the measurand current into a magnetic field, as well as the electronic front-end. While this tutorial is mainly addressed to students and non-expert readers, specific design aspects and dispersion effects due to temperature and other external phenomena are also discussed.**



***Index Terms*—Current sensing, Hall effect, galvanic isolation, instrumentation amplifier, analog front-end, current-to-magnetic field transduction, sensor characterization, sensor modeling.**

I. Introduction

VARIOUS applications in automotive and power electronics require accurate current sensing to estimate electrical power and energy. This demand is driven by the recent trends and policies towards energy efficiency [1], smart grids [2], [3], smart buildings [4], and hybrid electric vehicles [5]. Current sensing is of primary importance in power modules and converters [6], current leakage detection, over-current protection [7], electric vehicles [8], as well as energy production, conversion [9], and storage [10]. In several of these applications, the current sensor should satisfy many requirements, including low insertion loss, high dynamic range, robustness, high speed, low cost, and reduced physical dimensions. Therefore, it is essential to develop miniaturized and high-performance sensing devices to be possibly embedded within the power system. In this context, Hall-effect current sensors (HECSs) are promising candidates, since they are tiny devices inherently featuring galvanic isolation from the sensed current, have good linearity, large dynamic range, and are compatible with standard silicon technologies [11].

The design, development, and characterization of a HECS is challenging because of the necessary know-how in many different disciplines, from magnetometry and solid-state physics, to circuit design and metrology. This paper aims at a thorough and interdisciplinary presentation of HECSs, providing the reader with an exhaustive overview. This tutorial can be used as a basis for the design of HECSs, or to characterize and verify off-the-shelf devices using adequate Figures-of-Merit (FoMs).

The article is organized as follows. In the remainder of the Introduction, Sec. I-A presents the main metrics for a current sensor, while Sec. I-B reviews contactless current sensing technologies. Section II describes the Hall probe, from physical concepts to implementation criteria. Section III analyzes the characteristics of the electronic front-end and the transduction from current to magnetic field, discussing some typical configurations adopted for HECS. Section IV deals with typical sensor nonidealities, sensor modeling, and experimental characterization. Conclusions are drawn in Sec. V.

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A. Sensor Metrics

When analyzing a sensor, it is important to define the main FoMs for performance evaluation. From a functional perspective, current sensors can be generally described by expressing the output voltage V_{out} as a function of the measurand current I [12]:

$$V_{out} = SI + V_{os} + f_{nl}(I) + v_n; \tag{1}$$

where the following definitions are introduced:

- *Sensitivity*, indicated by S, is defined as the ratio between the increment in the output voltage over the increment in the measurand current. Sensitivity is a fundamental performance metric expressing the ability of the device in sensing small variations of the measurand current and translate them into large and robust voltage signals at the output.
- *Additive DC Offset*, indicated by V_{os}, is defined as the non-zero output voltage value at DC in the presence of a null measurand current. This quantity is intended as the result of different effects, including the electrical offset introduced by the front-end, as well as the effect of the earth magnetic field.
- *Nonlinearity*, indicated by $f_{nl}(I)$, is defined as the deviation from linearity for the relationship between the measurand current and the output voltage.
- *Noise*, indicated by v_n, corresponds to the output-referred noise density integrated over the acquisition bandwidth (in Vrms). Alternatively, it can be expressed as an input-referred noise (in Arms) by v_n/S.
- *Bandwidth* (BW), defined as the frequency interval from DC to the 3-dB attenuation point of the transfer function of the sensor.
- *Dynamic range* (DR), defined as the ratio between the maximum measurable current signal and the minimum detectable signal (MDS).

In the case of magnetic-based current sensors, another important property is the immunity to external magnetic fields, which may add up to the measurand. These are typically generated by other currents flowing nearby, or by alternative magnetic sources. In the following Secs., these FoMs and properties will be used to evaluate the performance and nonidealities of HECSs.

B. Overview of Current Sensing Technologies

A non-exhaustive review of the most popular current sensing approaches is hereafter reported by highlighting advantages and limitations, whereas Fig. 1 illustrates one of the possible classifications for the various sensing techniques, in this case based on the sensing principle [13].

While the Ohm's law could be easily applied to measure the current using the voltage drop across a current-carrying conductor with known resistance (e.g., a shunt resistor), this configuration lacks galvanic isolation, proportionally causing heat dissipation [7], [13].

Current transformers (CTs) are simple, highly sensitive, robust, cheap, and broadband devices able to measure AC currents. The output current is a function of the primary current and results from the counteracting magnetic induction

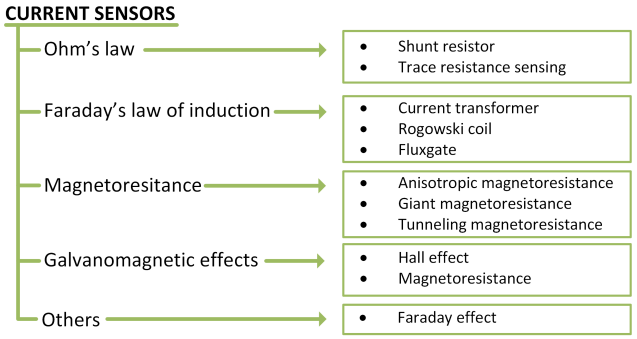

Fig. 1. Overview of current sensing techniques ordered by their operating principle.

on both the primary and the secondary sides [14]. CTs can be made very accurate by using high-permeability cores and a high number of turns. However, they cannot sense DC currents, and their magnetic core is subject to saturation, which can be avoided by increasing the core cross-sectional area. In addition, the magnetic core is typically susceptible to hysteresis and losses [13], [15], [16]. Rogowski coils, which make use of non-ferromagnetic air coil winding around a conductor [17], allow for sensors that are reliable, have large DR and high linearity. Nevertheless, they still cannot sense DC currents, and their sensitivity is comparatively lower than CTs [7], [18].

Fluxgate sensors exploit the magnetic hysteresis of ferromagnetic materials in order to sense very small magnetic fields. They can be used to realize highly accurate current sensors, yet they have limited DR and BW [19]–[21].

Optical current sensors are usually based on the Faraday effect, which takes place in polarized light within an optical fiber winded around a current conductor [22]. They are compact, broadband, and immune to electromagnetic interferences (EMI). Nevertheless, they usually find limited usage due to their high cost, complexity of implementation, and sensitivity issues [22], [23].

Magnetoresistive (MR) sensors are based on the variation of resistivity due to the presence of an external magnetic field. They can be grouped by the underlying magnetoresistance effect: anistropic magnetoresitance (AMR), giant magnetoresistance (GMR), and tunneling magnetoresistance (TMR) [19]. AMR sensors exploit the magnetic anisotropic scattering of conduction charge carriers in ferromagnetic materials [24], while GMR and TMR are based on physical effects arising in multilayer devices with magnetic materials [13], [25]. MR sensors are very good candidates for modern power applications but they all require specific back-end processes in the semiconductor technology, leading to relatively high costs.

Galvanomagnetic sensors rely on the Lorentz force acting on moving charge carriers to sense the magnetic field [7]. They can be grouped depending on the dominant galvanomagnetic effect: the geometrical magnetoresistive effect causes a change in the resistivity of the material along the main path of moving charge carriers, whereas the Hall effect generates a voltage drop orthogonal to the path of moving electrons.

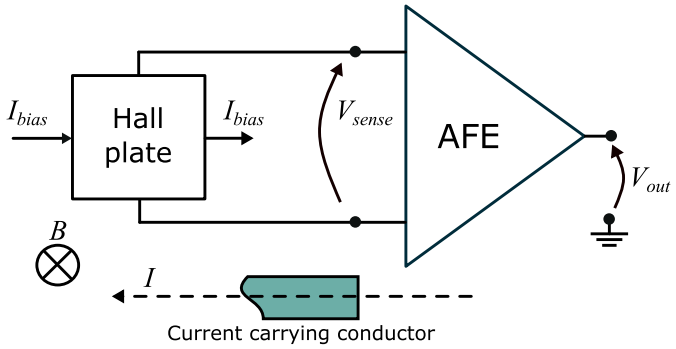

Fig. 2. Typical sensing chain of the HECS, consisting of the current-to-magnetic field transduction, the Hall plate, and the AFE.

HECSs, which are the subject of this article, are highly compatible with standard silicon technology and can be either integrated in CMOS (allowing for low-cost solutions) or might leverage on alternative compounds to achieve better performance. Generally, silicon-based HECSs have lower sensitivity with respect to GMR and TMR sensors, with resolutions usually limited to a few hundreds μT [26], [27] in standard implementations, or a few μT when using magnetic concentrators [28], [29]. A further improvement (down to less than 100 nT) can be obtained exploiting the 2D electron gas (2DEG) layer of quantum-well Hall sensors (QWHS) [30]. Despite a number of limitations including low sensitivity, limited BW, high intrinsic offset, sensitivity to external magnetic fields, and temperature dispersion of the parameters, their compact nature, low cost, low heat dissipation, high DR, good linearity, and the ability to measure DC currents, make HECSs well suited for modern power applications. Moreover, the typical limitations of HECSs can be mitigated by exploiting specific materials, devices, and tailored circuit configurations [31]–[33].

A HECS can be generally treated as a three-stage sensing chain consisting of (Fig. 2): *i)* a current-to-magnetic field transducer; *ii)* the Hall probe (i.e., the magnetic sensitive device), and *iii)* the analog front-end (AFE). The analysis of each of these stages is critical for the proper design of the current sensor, and will be discussed in the following. It should be noted that this manuscript focuses on integrated HECSs in standard CMOS technology. For aspects specific to HECSs implemented in other semiconductor technologies, the reader is referred to the specific literature, e.g., [19], [34].

II. Hall Probes

A. Galvanomagnetic Effects

This Section aims at a basic understanding of the physics behind the Hall-effect device and its main parasitic effects, while we refer the reader to [35], [36] for a more detailed and rigorous description. Let us consider a n-type rectangular semiconductor device with thickness t, width w, and length l, in which a current I_{bias} is forced to flow through the contacts C1 and C2 due to an external electric field $\mathbf{E_{bias}}$ (Fig. 3). When a magnetic field $\mathbf{B}$ is applied to the device, the Lorentz

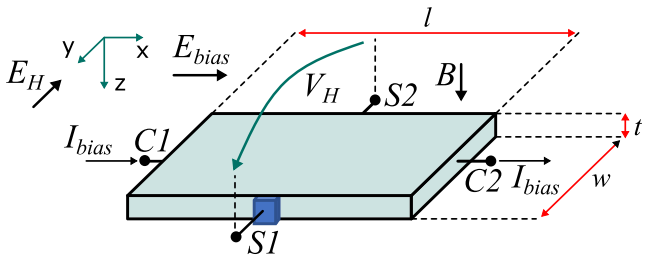

Fig. 3. Rectangular semiconductor plate highlighting the generation of a transverse electric field when an out-of-plane magnetic field is applied.

force acting on electrons can be described as

$$\mathbf{F} = -q\mathbf{E_{bias}} - q(\mathbf{v} \times \mathbf{B}); \tag{2}$$

where the first term is the electrostatic force and the second one represents the magnetic action, being $q = 1.6 \times 10^{-19}$ C the electron charge and $\mathbf{v}$ the local velocity of the carriers.

While the electrostatic part of the Lorentz force moves the charge carriers along the x-direction (see Fig. 3), the magnetic part pushes them towards one edge of the device along the y-direction, eventually leading to a non-zero space charge, and thus creating an electric field $\mathbf{E_H}$ along y. This acts on the charges with a force $\mathbf{F_H} = -q\mathbf{E_H}$ that, at steady state, counterbalances the magnetic action of the Lorentz force. Hence, $\mathbf{E_H}$ can be expressed as

$$\mathbf{E_H} \approx \mu_n(\mathbf{E_{bias}} \times \mathbf{B}), \tag{3}$$

while the total electric field in the device is given by

$$\mathbf{E_{tot}} = \mathbf{E_{bias}} + \mathbf{E_H}, \tag{4}$$

which is not collinear with the current density $\mathbf{J}$ along the device. The deflection angle between $\mathbf{E_{tot}}$ and $\mathbf{J}$ is known as the Hall angle (θ_H), for which it holds [35]:

$$\tan\theta_H = \mu_n B_z, \tag{5}$$

where B_z is the component of $\mathbf{B}$ along the z-direction. The Hall angle is a fundamental metric for Hall devices, as it directly expresses how much the Hall effect is perceivable with respect to the electrostatic bias. It also clarifies that the mobility (μ_n) of the charge carriers is a key parameter in Hall probes. Indeed, the higher the mobility, the higher the sensitivity to the magnetic field, as shown hereafter.

By accounting for (3) and referring to Fig. 3, the Hall effect in a device ultimately results in a transverse Hall voltage between contacts S1 and S2:

$$V_H = \int_{S_1}^{S_2} E_H\, dy = \frac{\mu_n}{\sigma t} I_{bias} B_z = \frac{1}{nqt} I_{bias} B_z, \tag{6}$$

being $\sigma = nq\mu_n$ the electrical conductivity. As from (6), V_H is directly proportional to the vertical magnetic field, while also depending on the bias and on the geometrical/technological parameters of the device. In order to increase the Hall voltage at the output, the device should feature low carrier concentration and be as thin as possible (indeed, Hall probes are usually referred to as Hall plates). In practice, (6) does not take into account some important physical phenomena of conduction, e.g., the thermal motion of the carriers and their velocity distribution. These effects can be considered by replacing

TABLE I
CHARACTERISTICS (AT 300 K) OF SEMICONDUCTORS USED FOR HALL-EFFECT SENSORS

Material	μ_n ($\mathrm{cm^{-2}V^{-1}s^{-1}}$)	n ($\mathrm{cm^{-3}}$)	R_H ($\mathrm{cm^3C^{-1}}$)
doped Si	1500	2.5×10^{15}	2.5×10^3
InSb	80000	9×10^{16}	70
InAs	33000	5×10^{16}	125
GaAs	8500	1.45×10^{15}	4.3×10^3

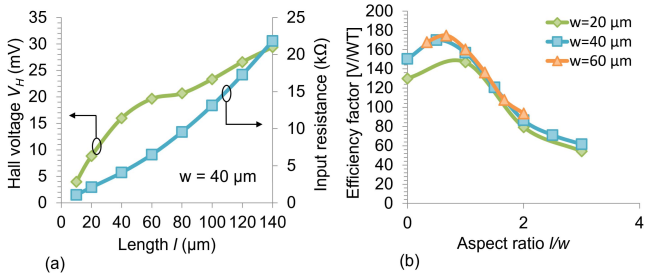

Fig. 4. (a) Variation of Hall voltage and input resistance with device length for a 40 μm wide Hall plate biased at 500 μA under 50 mT of out-of-plane field (from [12]). (b) Device efficiency as a function of its aspect ratio (from [12]).

μ_n with the Hall mobility $\mu_H = \mu_n r_H$, leading to the new expression:

$$V_H = \frac{r_H}{nqt} I_{bias} B_z = R_H \frac{I_{bias}}{t} B_z, \tag{7}$$

where r_H is the Hall factor ($r_H \approx 1$ for the majority of standard materials) and $R_H = \frac{r_H}{nq}$ is known as the Hall coefficient.

B. Materials

The choice of the material for the Hall device plays a significant role in originating the Hall effect [35]–[37]. Indeed, (6) clearly shows that the Hall voltage is directly proportional to carrier mobility, and that it is inversely proportional to conductivity and carrier concentration. Suitable candidates for HECS devices are semiconductor materials like silicon and III-V compounds (e.g., InSb, GaAs, InAs) with high mobility and relatively low conductivity. Table I reports the mobility, the average carrier concentration, and the Hall coefficient of semiconductors typically used for HECS devices ($r_H = 1$ assumed for all the materials). Nevertheless, it should be noted that low energy bandgap materials usually show high mobility but also high carrier concentration, leading to a trade-off. Moreover, when choosing the device material, the designer must consider the compatibility with the available semiconductor technologies in terms of integrability, economic feasibility, and realiability.

C. Hall Plates Technology

The Hall probe is a four-terminal solid-state device that relies on the Hall effect discussed in Sec. II-A. In this context, the fundamental expression in (7) was obtained for an ideal device characterized by $l \gg w$, negligible contacts, and unconstrained by any specific technology process. However, technological aspects are of primary importance when dealing with the implementation of the sensing device [12], [36], [38]. In this Section, the analysis will focus on CMOS technology, but similar considerations can be applied to other semiconductors.

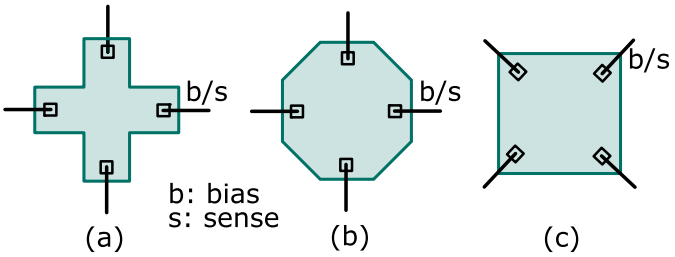

Fig. 5. Different geometries of the active area (i.e., n-type well) for Hall plates: a) cross b) octagonal c) square with contacts on the angles.

A real Hall-effect device cannot be assumed infinitely long, and at least four contacts are needed to realize a Hall probe. The effects of the implemented shape are taken into account by defining the Hall geometrical factor $G_H = \frac{V_H}{V_H^\infty}$ as the ratio between the actual Hall voltage (V_H) and the voltage generated by an infinitely long Hall device (V_H^∞). Therefore, the Hall voltage of a generic Hall plate can then be expressed as

$$V_H = \frac{G_H R_H}{t} I_{bias} B_z. \tag{8}$$

The exact value of G_H depends on the shape of the device, on the sizing and position of the contacts, and also on the Hall angle θ_H [39]. The G_H factor of a specific device shape can be analyzed by using different techniques, e.g., conformal mapping [35], boundary element methods, or finite element methods (FEMs) [12], [40]. Some general design rules are summarized in [12].

Following the definition of G_H, the longer the device, the higher the Hall voltage, up to the theoretical limit (see Fig. 4a). However, increasing the length of the device also increases the input resistance (also in Fig. 4a). In this case, a higher bias voltage is required to force the same I_{bias}, causing an overall increase in power consumption. This trade-off is well represented by the efficiency factor η (also known as power-related sensitivity):

$$\eta = \frac{V_H}{V_{bias} I_{bias} B}, \tag{9}$$

which shows a local maximum for an aspect ratio $l/w \simeq 1$ (Fig. 4b), so that symmetric shapes are preferable in this sense. Moreover, symmetric devices are easier to fabricate, and symmetry can also be exploited to improve the final performance of the sensor (see Sec. III-A).

The basic Hall device usually requires two contacts connected to a high-impedance current source for the biasing of the device with I_{bias}, and at least two contacts connected to a high-impedance AFE for sensing the Hall voltage without sinking current. While this being the standard architecture, alternative configurations can also be developed [41]–[43]. Each of these contacts creates local short circuits affecting the basic plate structure. In particular, bias contacts locally null the orthogonal electric field, while highly doped sense contacts create space charge regions that lower the measurable Hall voltage [44]. As shown by FEM analysis [12], the G_H factor for a generic shape can be maximized by using large bias contacts (as large as half the width of the device) and small sense contacts placed at half the length of the device. However, this hinders the perfect symmetry of the plate, and small sense contacts are more susceptible to misalignment

errors, giving rise to an additive offset voltage. Therefore, sense contacts are usually designed to have the same shape as bias contacts. Figure 5 reports some typical shapes for the Hall plate, while an in-depth analysis can be found in [38], [45]–[49]. The cross shape was demonstrated to achieve high values of G_H even employing large sense contacts, while the square shape displayed higher sensitivity values.

Regardless of the chosen shape, the Hall plate is meant to be a bidimensional device with negligible thickness. In standard CMOS implementations, the Hall probe is usually realized by a low-doped n-type well because of the higher mobility with respect to p-type wells. The thickness is defined by the diffusion depth set by the CMOS process, and cannot be changed by the designer [32]. The n-type active well is encapsulated in a p-type layer, which could be the epitaxial substrate or an isolation layer. In any case, the encapsulation in the p-type well originates a pn junction with its corresponding depletion layer, which lowers the effective thickness of the Hall probe and makes it non-constant along the Hall plate [12], [49], [50]. Moreover, it causes spurious dependencies on the bias and the magnetic field by means of the magnetoresistive effect and the junction field effect, leading to nonlinearity [35], [51]. The p-type layer can be reverse-biased to enlarge the depletion layer, reduce the effective thickness, and increase the sensitivity. However, the achievable improvement is negligible with respect to the increased complexity of the electronics required to properly drive the p-type layer. Alternatively, the effective thickness can be reduced by placing a shallow trench isolation on top of the active layer, or can be modulated by covering the n-well with a thin p-type implantation layer (which creates another depletion region) or a polysilicon gate inducing a field effect [49], [50]. These last two techniques also allow to protect the device from spurious electric fields by connecting the covering layer to ground. In all cases, a parasitic capacitance is associated to the depletion region, setting a fundamental BW limit for the HECS [31], [52], [53].

III. Current Sensing Chain

A. Spinning-Current Technique

The offset voltage is one of the main constraints in Hall plates, as it can be up to a few mV, leading to an input-referred magnetic field offset from a few mT to tens of mT [39], [54]. The intrinsic offset voltage of the Hall plate ($V_{os,plate}$) can be caused by both systematic and random sources, e.g., resistivity gradients, crystal defects, and mechanical stress [19], [39], [55]. Given its importance, many works in the literature [56]–[60] have dealt with its modeling and compensation. The basic model for $V_{os,plate}$ is the unbalanced resistive Wheatstone bridge (Fig. 6a), where the differential voltage between the two branches results in

$$V_{os,plate} = \frac{\Delta R}{4R} V_{bias}. \tag{10}$$

While there exist more complicated equivalent circuit models, they all derive from the basic Wheatstone bridge.

In principle, if the Hall plate is symmetric and reciprocal (i.e., the bias and sense contacts can be interchanged without any effect on the Hall voltage), it is acceptable to concentrate the unbalance of the Wheatstone bridge into a single component, as in Fig. 6a. In this case, the offset can be

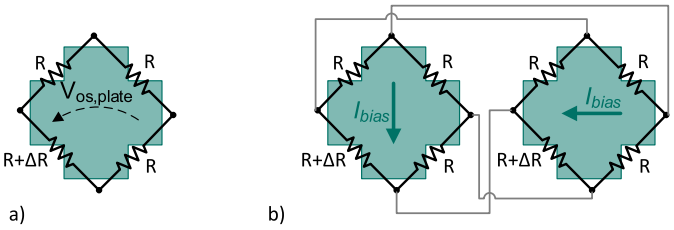

Fig. 6. (a) Wheatstone bridge model of the intrinsic offset in CMOS Hall sensors. (b) Connection of two Hall plates in the pairing technique with modeling of systematic offset, only.

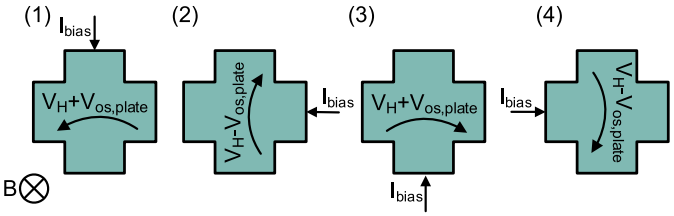

Fig. 7. Graphical representation of 4-phase spinning-current technique for the cancellation of the intrinsic offset.

theoretically nulled by applying the pairing technique [61], which consists of pairing two Hall plates and connecting them in parallel, while rotating one of the two plates by 90° (Fig. 6b). In practice, however, the offset of the two probes is never exactly the same due to the statistical nature of some of the offset sources. In addition, the offset is time- and temperature-dependent, thus requiring a periodic calibration. While providing some degree of offset reduction, the pairing technique will always leave a residual offset value and bring additional disadvantages, as it doubles the area and power consumption [39], [61]–[63].

The main advantage of Hall plates realized on silicon is the straightforward integration with standard CMOS technology, allowing to implement a series of dedicated circuits and systems addressing the nonidealities [64], [65]. Also, complex digital circuits can be integrated for the realization of smart sensors [66], [72]. A noteworthy approach dealing with the offset voltage problem in symmetric Hall plates is the spinning-current (SC) technique [68]. It involves biasing the same Hall plate in four orthogonal directions, dynamically swapping contacts between biasing and sensing every $T_{spin} = \frac{1}{f_{spin}}$, so that a full rotation takes a total time of $4T_{spin}$ (Fig. 7). Due to the symmetries of the Hall probe, a 90° spatial rotation of the bias current causes a change in the sign of $V_{os,plate}$, while its magnitude remains approximately the same [35], [68]. As a result, the offset voltage is modulated at frequency $\frac{f_{spin}}{2}$ and can be attenuated by a low-pass filter. Moreover, a proper choice of the SC phase sequence allows to suppress interferences, low-frequency noise, and pick-up noise [30].

Nevertheless, a residual ripple will typically remain present, and its removal has been the subject of research in the last years [65], [69], [70]. In addition, due to the anisotropy of the Hall plate (caused by, e.g., junction-field effect and piezoresistivity) [35], [54], [57] the value of $V_{os,plate}$ changes with the bias direction, causing a residual DC offset, yet $\times 100$ lower than the intrinsic one.

To implement the SC technique, a complex switching network is required to route the contacts of the Hall plate either to the generator of the bias current or to the readout circuit.

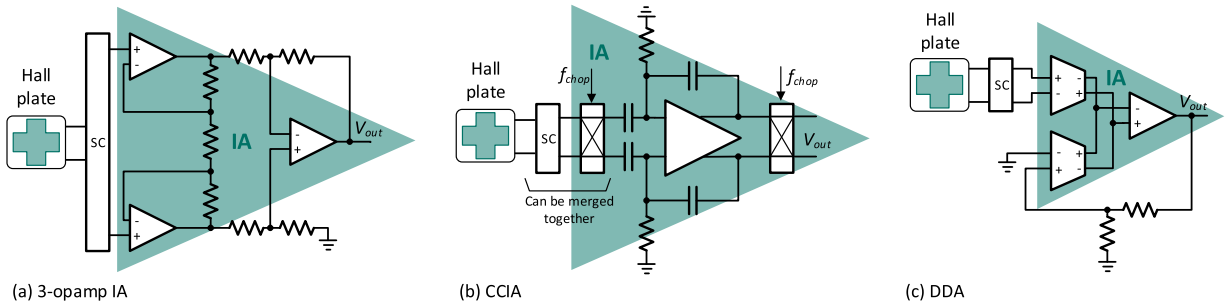

Fig. 8. Examples of instrumentation amplifiers (IAs) used as analog front-end (AFE) for Hall plates. (a) Three operational amplifiers (three-opamp) IA; (b) capacitively-coupled instrumentation amplifier (CCIA) with choppers; (c) differential-difference amplifier (DDA). All the AFEs are connected to the Hall plate by a circuit implementing the SC technique.

The implementation of the switches adds nonideal effects, like charge injection and clock feedthrough. To cope with these effects, the switches are usually made large, increasing the capacitive load seen by the Hall plate and limiting the achievable BW.

B. Analog Front-End

The AFE has a crucial role since it directly affects the sensor performance, and it must be adapted to the characteristics of the Hall plate. In general, the AFE includes the circuits required for both biasing the Hall plate and for sensing the Hall voltage. However, only the latter is discussed here, as it involves the main design challenges. The AFE must fulfill many requirements, among which [67]:

- high differential gain, usually greater than $\times 100$, depending on the application and technology;
- high input impedance, to avoid draining current from the sense contacts;
- negligible offset with respect to the inherent one displayed by the Hall plate.

The first two requirements imply the adoption of an instrumentation amplifier (IA). The IA can be implemented by using different architectures, like the three operational amplifiers (thee-opamp) topology [61] (Fig. 8a), the capacitively-coupled instrumentation amplifier (CCIA) [69], [71] (Fig. 8b), or the differential-difference amplifier (DDA) [53], [72] (Fig. 8c). The three-opamp is the standard IA architecture, but the usage of three amplifiers increases the noise level, together with a considerable power consumption. In addition, while the usage of off-chip resistors leads to high accuracy, it also increases the cost and area.

The CCIA is a non-inverting fully-differential operational amplifier using capacitors instead of resistors in the feedback loops. In this way, the circuit does not draw any DC current from the sensor, but its DC operating point must be carefully set using high-value resistors or pseudo-resistors [73], [74]. It offers very good performance in terms of noise and power consumption, since it is based on a single gain stage [74]. However, it requires an input upconversion stage to allow for DC signal sensing, which would otherwise be filtered out by the input capacitance [74]. This modulation stage can be implemented by a chopper circuit, which grants very low input-referred offset, but it also limits the input impedance $Z_{in,AFE}$, which is inversely proportional to the chopping frequency and input capacitance [75]:

$$Z_{in,AFE} = \frac{1}{2\pi f_{chop} C_{in}}. \tag{11}$$

This network can be smartly designed to concurrently work as SC for the Hall plate and as chopper for the AFE, reducing the area required by the electronic interface. The main disadvantage of the CCIA is a limited acquisition BW due to the frequency-dependent input impedance given by (11) and the high capacitive input load given by the switches of the chopper.

The DDA, formally described in [76], is an extension of the operational amplifier featuring two differential inputs, suitable for the processing of floating voltages. It can be used by means of a standard resistive feedback without sinking DC current from the input. It offers a good trade-off among noise, power consumption, and input impedance, while being intrinsically more noisy than the CCIA due to the presence of more gain stages and resistors. However, the Hall plate can be DC-coupled to a differential input pair, sinking negligible current from the sense contacts. This architecture allows to minimize the capacitive input load and to increase the BW by minimizing the size of the input transistors [53], or by adding capacitive cancellation systems based on positive feedback [77].

Finally, it is worth noting that this Section was oriented on AFEs for standard Hall plates operated in voltage mode. The current mode, in which the Hall voltage is nulled and the output of the Hall plate is a current, is indeed possible. In this case, the AFE is realized by a transimpedance amplifier (TIA) [78], [79].

C. Current-to-Magnetic Field Transduction

The transduction from current to magnetic field is based on the Ampere's circuital law. In the magnetostatic case, considering the simple example of a conductor of infinite length and negligible cross-area in free space, and traversed by a constant current I, the Ampere's law can be simplified by using the Biot-Savart formula:

$$|\mathbf{B}(r)| = \frac{\mu_0 I}{2\pi r}; \tag{12}$$

where μ_0 is the magnetic permeability of the vacuum, and r is the distance between the conductor and the point in space at which the magnetic field is sensed/evaluated.

The Ampere's law and its derivations state that it is always possible to indirectly estimate a current by sensing the associated magnetic field at a known distance r. However, magnetic interferences may corrupt (12) with an additive term, affecting the selectivity of the HECS.

The current-to-magnetic field transduction factor G_{IB} is of paramount importance in HECSs, as it can affect many sensor metrics, e.g., sensitivity, input full-scale range, and MDS. For the example above, it can be defined from (12) as

$$G_{IB} = \frac{|\Delta \mathbf{B}(r)|}{\Delta I} = \frac{\mu_0}{2\pi r}, \tag{13}$$

highlighting a direct dependence of G_{IB} to the exact distance of the sensor from the conductor by means of the parameter r. This dependence may cause many issues like increased sensitivity to mechanical noise and nonlinear effects. While (13) reports the transduction factor for a simple academic case, an accurate analysis of the magnetic circuit and geometries are required for getting the exact formulation of G_{IB} in practical cases. Usually, G_{IB} should be maximized to improve MDS and sensitivity, and should be made insensitive to thermo-mechanical effects.

Moreover, the magnetic environment should be designed to reduce the sensitivity to external EMI. In general, the use of a core allows to shunt stray magnetic fields around the sensor. Conversely, coreless architectures are susceptible to stray fields from traces carrying high currents, which may be captured by the Hall plate and eventually cause inaccurate current measurements. In this case, a differential Hall plate configuration can be employed, although any mismatch between the Hall plates, or any field disuniformity, will result in a deviation on the output signal. In the following, the most used and important arrangements employed in HECSs are summarized.

1) Yoke-Hall: An arrangement combining a Hall plate with a gapped magnetic yoke with permeability μ_r is shown in Fig. 9a [7], [80]–[82]. Specifically, the magnetic core is clamped around the current-carrying conductor (i.e., a wire or a busbar), so that all the magnetic flux generated by the current I is concentrated on the core itself and focused on the Hall plate, which is placed in the air gap of the magnetic core. This arrangement is named open-loop configuration and implies the following equation for the magnetic field on the Hall plate:

$$|\mathbf{B}(r)| = \frac{\mu_0 \mu_r I}{2\pi r - d + d\mu_r}, \tag{14}$$

where d is the thickness of the air gap, while the distance r can be usually approximated with the yoke radius. A good design satisfies $d\mu_r \gg 2\pi r$, allowing to simplify (14) in

$$|\mathbf{B}(r)| = \frac{\mu_0 I}{d}, \tag{15}$$

which is independent of the relative position of the wire. With respect to the situation in free space as from (12), the G_{IB} in the yoke-Hall open-loop configuration is increased by a factor $2\pi r/d$, and can be further increased by winding the wire around the yoke. This arrangement offers G_{IB} factors as high as 1 mT/A and it is robust against EMI. However, BW, weight, and dimension of the sensor are affected by the presence of the yoke, which also suffers from magnetization in case of large over-current events.

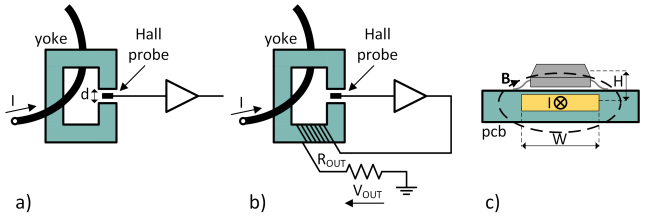

Fig. 9. a) Open-loop HECS with magnetic yoke. b) Closed-loop HECS with magnetic yoke. c) Open-loop yoke-less HECS with current-carrying trace realized at PCB level. This configuration requires an IMC to bend the magnetic field lines (see Fig. 10).

The closed-loop configuration, also known as zero-flux sensor, copes with this last issue [7], [13], [80]–[82]. In this case, the output of the Hall probe drives a secondary coil winding around the magnetic core, in order to null the magnetic flux density inside the core (Fig. 9b). This arrangement still exploits the advantages given by the core to improve the sensitivity and to reduce the dependency on the geometry, as well as the sensitivity to EMI. It should be noted that the Hall plate is placed in the feedback loop, so that the output signal of the HECS is the voltage on the output resistor. Moreover, this arrangement resembles a CT at high frequencies [82], [83], improving the BW. Nevertheless, its usage is not straightforward in modern applications given the weight and space occupation.

2) Yoke-Less Open-Loop Sensor: A more compact arrangement can be obtained by realizing a yoke-less open-loop configuration at PCB level, as shown in Fig. 9c. [7], [27], [70], [84]–[88]. The current-carrying conductor is realized as a trace on the top conductive layer of the PCB (or on a separated busbar) and the Hall probe is implemented as an integrated circuit (IC) placed on top of the trace in order to maximize G_{IB}, which in this case can be approximated as [85]:

$$G_{IB} = \frac{\mu_0}{2(W + 2H)}; \tag{16}$$

where W is the trace width and H is the trace-to-sensor distance. Nevertheless, package-to-PCB clearance as well as package and die thickness usually imply $H > 0.3$ mm [70]. Typical values for G_{IB} are in the order of 100 μT/A. Thus, multi-layer/multi-turn techniques, as well as ferromagnetic shields [85] can be used to further increase G_{IB} by concentrating the magnetic field on the Hall probe.

An important implication of the PCB approach is that the magnetic field lines on the Hall probe lie on the x-y plane, while the Hall plate is sensitive to the out-of-plane field. Thus, it is required to either rotate the Hall IC or bend the field lines. The usage of a through-hole package for the sensor allows to rotate the Hall IC and place it vertically with respect to the board plane. However, this technique increases the trace-to-probe distance above 1 mm.

Alternatively, it is possible to integrate magnetic flux concentrators (IMCs) in the same IC used for the Hall probe [28], [29], [89]–[91]. IMCs are thin layers (10 – 100 μm) of high-permeability ferromagnetic material spattered over the silicon die. The magnetic field lines converge on one edge of the magnetic material and diverge on the opposite one.

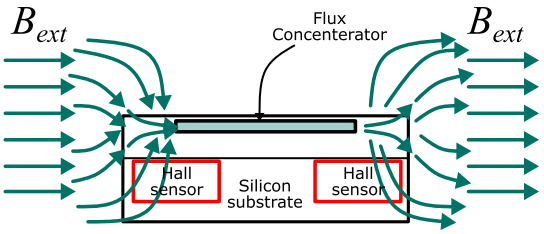

Fig. 10. 2D representation of the magnetic effects of IMCs. The flux lines due to the external magnetic field are bended and concentrated into the IMC.

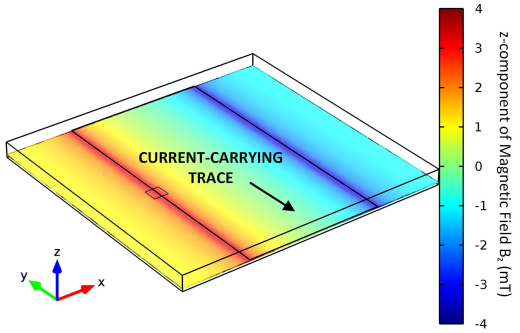

Fig. 11. Bidimensional map of the B_z field computed at the silicon-oxide interface 10 μm beneath the copper current-carrying trace. The map shows a maximum of the B_z field at the vertical projections of the edge of the trace.

Hence, the field lines bend in the proximity of the flux concentrator edge, creating a convenient positioning for the Hall plate (Fig. 10). Moreover, the concentration of the field lines leads to an amplification of the magnitude of the magnetic field (magnetic gain values from 5 to 10 are reported in the literature [28], [89]), with an amplification factor depending on the shape and thickness of the concentrator, on the relative position of the Hall device, and on other geometrical factors. It should be noted that IMCs can suffer from the saturation of the ferromagnetic material, making G_{IB} nonlinear at high-field, hence limiting the full-scale range.

3) Open-Loop Sensor With On-Chip Trace: To reduce the trace-to-probe distance down to a few μm, it is possible to integrate the current-carrying trace and the Hall probe within the same IC [53], [66], [71], [72] by exploiting thick copper layers [92], redistribution layers in wafer-level packaging, or copper frames. However, when placing the Hall plate at the minimum allowed distance, i.e., vertically beneath the trace, the out-of-plane field acting on the probe is zero. As IMCs and other magnetic techniques cannot be exploited at such a small scale, the only possible solution is moving the probe laterally away. This will increase the trace-to-probe distance and lower the magnitude of **B**, but the component of the field on the z-axis will increase, leading to a design trade-off.

Figure 11 reports the z-component of the field at the silicon-oxide interface beneath the trace, showing that the optimum position for the Hall probe is exactly below the edge of the current-carrying trace. This geometrical arrangement also implies that the magnetic field on the Hall probe is not confined to the z-direction, and a non-negligible in-plane field will arise. This could trigger spurious behavior at the probe level, like planar Hall effect [35], [93].

The integration of the trace and probe on the same IC provides a good rejection of mechanical noise, allowing to assume a noiseless $I - B$ transduction, given the precise and stable definition of the relative distance. On the other hand, the lack of magnetic circuits makes the HECS sensitive to external magnetic fields. This issue can be mitigated by placing two Hall plates below the opposite edges of the trace and combining their output voltages to eliminate any common-mode magnetic field interference, e.g., the earth magnetic field, or the one induced by noisy power circuits [96]. With this arrangement, G_{IB} factors in the order of a few mT/A can be achieved [53]. The thick copper layer presents low sheet resistance values, yet it poses a limitation on the maximum current due to electromigration and heat dissipation. Although large integrated copper traces could present a resistance lower than 10 mΩ [27], a 10-A current would already imply a few Watt of heat power to be dissipated. Dedicated package solutions with low thermal resistance are thus mandatory in this case. Moreover, specific lead and bonding techniques with low resistivity values must be implemented. At the same time, the package, leads, and bonding wires can critically reduce the operating BW, as they create spurious parasitic elements, which might couple the magnetic field generated by the sensed current into sensitive signal nodes [31] (see Sec. IV). Different packaging solutions are available on the market, which differ with respect to the maximum current on the integrated trace. The wafer-level chip-scale package (WLCSP) with the measurand current flowing on redistribution layer (RDL) copper traces [53], or a flip-chip mounted Hall plate on U-shaped copper frames, can handle up to a few tens of A [27]. Table II reports the standard full-scale ranges for different types of open-loop current sensors based on the Hall effect.

TABLE II
FULL-SCALE RANGES FOR OPEN-LOOP CURRENT SENSORS

Technical Solution	Typical Input Full-scale Range
Open-loop HECS with yoke	up to 700 A
Bus bar with magnetic shield	From 50 A to 700 A
On-board PCB trace	From 10 A to 50 A
On-board PCB trace with multi-turn	From 2 A to 10 A
open-loop sensor with trace on WLCSP	$<$ 20 A

IV. SENSOR MODELING AND CHARACTERIZATION

A. Nonidealities

Non-idealities of the Hall plate set the main performance limitations of HECSs. Therefore, we analyze the specific performance criteria starting from the Hall plate, then including considerations due to the AFE and the magnetic interface. Table III provides an overview of typical HECSs reporting the performance metrics of commercially available HECSs as well as of HECSs proposed in recent literature.

1) Sensitivity: Considering the definition in Sec. I, the sensitivity of a HECS can be expressed as:

$$S = G_{IB} S_A G_{AFE}, \tag{17}$$

where G_{IB} is the current-to-magnetic field transduction, G_{AFE} is the electronic gain of the AFE, and S_A is the absolute sensitivity of the Hall plate, which can be expressed as:

$$S_A = V_H / B_z = \frac{G_H R_H}{t} I_{bias}. \tag{18}$$

According to (17), all three stages of the sensing chain have the same importance in determining the sensor sensitivity

TABLE III
COMPARISON OF HECSs (COMMERCIAL AND FROM RECENT LITERATURE)

Metric	LEM HO-NP 0100	Allegro ACS732 -20AB	Melexis MLX 91208	TI TMCS 1100A1	[31]	[94]	[95]	[71]	[70]
Type	yoke-hall	on-chip	on-PCB	on-chip	on-chip	on-chip	on-pcb	on-chip	on-pcb
Range (A)	100	20	25 mT*	46	20	25	60	4	8 mT*
Sensitivity (mV/A)	20	100	100 mV/mT*	50	36	30	3.1	43.5	100 mV/mT*
Noise (mA rms)	1250	55	60 μT*	100	<100	64	710	150	210 μT*
DR (dB)	38	51	52	46	52	53	38	28	46
Offset (mA)	<250	300	12 μT*†	8	<280	<170	n.a.	n.a.	n.a.
Temperature dep. [Offset] (mA/K)	<3.75	1	<150 ppm/K*	0.074	5.5	n.a.	n.a.	n.a.	n.a.
Temperature dep. [Sensitivity] (ppm/K)	<200	n.a.	<40	0.4%	n.a.	n.a.	n.a.	n.a.	n.a.
Bandwidth (kHz)	350	1000	250	80	4000	1800	15000*	75000*	3000
Consumption (mA)	19	24	12	4.5	5.5	<11	n.a.	18	7.7
Size (cm^2)	8	1	0.3	0.2	chip‡	chip‡	chip‡	chip‡	chip‡

*Current-to-magnetic transduction not included (must be designed by the user).
†After correction by the user.
*Achieved by combining the Hall probe with an on-chip integrated coil (coil does not focus the field on the Hall probe).
‡As the chip package is not specified, size $<$ cm^2 is assumed.

and its long/short-term stability. The absolute sensitivity S_A cannot be used as a FoM for the Hall plate, since it depends on the applied polarization. Therefore, two other sensitivities are defined for Hall plates according to the applied bias (either current or voltage): the current-related sensitivity $S_I = S_A/I_{bias}$, expressed in V/AT, and the voltage-related sensitivity $S_V = S_A/V_{bias}$, expressed in V/VT. These are related to each other by the input resistance of the Hall plate $R_{in,plate} = V_{bias}/I_{bias}$. A maximum S_V value of 0.742 μ_H was estimated in [35], while state-of-the-art values for S_I are reported in Tab. IV for different Hall probes and materials. For silicon Hall plates, the S_I depends on temperature due to the effects of temperature on the concentration of free carriers n in the active region [35] (and, in turn, on the Hall coefficient R_H), as well as through the temperature-dependent stress effects induced by the package [97]. The temperature coefficient α_{S_I} of the current-related sensitivity can vary several hundred ppm/K from the nominal value at $T \sim 300$ K, usually ranging between 500 ppm/K and 0.1%/K on the basis of sensor and packaging technologies [27], [63], [97]. Note that package-free Hall plates (e.g., flip-chip bonded to ceramic substrates) can achieve even lower temperature coefficients at room temperature, yet with the same dispersion across the operating range [97]. Even G_{IB} and G_{AFE} may be affected by the temperature, yet their specific dispersion depends on the chosen magnetic transduction and AFE architecture. Long-term drift of HECS sensitivity can be expressed by $\Delta S/S$ (with values in the order of 10^{-4}/year [16]), or by the lifetime drift error (with values in the order of 1%, [27], [98]), representing the expected error at the end of life of the sensor (according to AEC-Q100 qualification).

Depending on the type of package, the sensitivity is also affected by humidity. For example, plastic packages are known to absorb moisture, which in turn causes a change in the mechanical stress seen by the sensor, ultimately altering the sensitivity due to the piezo-Hall effect [99].

2) Offset: The output voltage V_{sense} of the Hall probe is the differential voltage measured between the sense contacts, that can be written as

$$V_{sense} = \int_{S1}^{S2} \mathbf{E_{tot}}\, dl \tag{19}$$

TABLE IV
CURRENT-RELATED SENSITIVITY FOR DIFFERENT HALL PROBES

Reference	Semiconductor technology	S_I (V/AT)
[31]	Silicon BCD	200
[100]	GaN	130
[101]	Graphene	1000
[32]	Silicon BCD	800
[102]	Silicon CMOS	250

where $\mathbf{E_{tot}}$ is the global electric field resulting from both electrostatic and magnetic actions. As discussed in Sec. II-A and shown by (4), the expression of $\mathbf{E_{tot}}$ can be generally split into the sum of the two components, so that

$$\begin{aligned} V_{sense} &= \int_{S1}^{S2} (\mathbf{E_H} + \mathbf{E_{bias}})\, dl \\ &= \int_{S1}^{S2} \mathbf{E_H}\, dl \; + \int_{S1}^{S2} \frac{\mathbf{J_{bias}}}{\sigma_B}\, dl \; = V_H + V_{os,plate}, \end{aligned} \tag{20}$$

where $\mathbf{J_{bias}}$ is the bias current density along the device, and σ_B is the effective electrical conductivity [35]. The first term in (20) is the Hall voltage, while the second term is an additive perturbation, i.e., the offset voltage $V_{os,plate}$, which is originated by the non-ideal implementation of the Hall plate. One can see from (20) that the offset voltage is zero only if the current density lines due to the biasing electric field are perfectly orthogonal with respect to the straight line from S1 to S2. However, misalignments of the sense contacts and the finite geometrical realization of the Hall plate do not allow for perfect orthogonality. Other important sources of offset are related to imperfections in the device fabrication, non-uniformity of the semiconductor properties, and the mechanical stress due to the piezo-resistance effect [19], [39], [55].

The intrinsic offset of the Hall plate $V_{os,plate}$ is temperature-dependent, and it suffers from long-term drift, resulting in calibration procedures that are often complex yet ineffective. Indeed, the presence of a residual offset is one of the main disadvantages of HECS. Nevertheless, the SC technique can effectively reduce the offset and mitigate its temperature dispersion. Indeed, state-of-the-art Hall plates employing the SC technique can achieve a residual offset as low as 40 μT [70], [94] with a temperature coefficient of around 1 μT/°C [26], [65].

Apart from the offset voltage intrinsically created by the Hall plate, the additive DC offset in (1) also takes into consideration the offset of the AFE, as well as other magnetic interferences. The earth magnetic field is a typical example of this kind, but other spurious magnetic fields should also be considered. Eventually, the magnetic shielding configuration is a critical design step. Regarding the AFE, the usage of a chopper architecture or an auto-zero technique [103] is strongly recommended; otherwise, the offset generated by the electronic circuits may become the dominant one, impairing the usefulness of the SC. In this view, the CCIA may be a good choice since it intrinsically requires a chopper circuit and concurrently offers good noise and power performances.

3) Noise: Concerning the Hall plate, random fluctuations of the free carriers in the semiconductor active region set the ultimate limit for the HECS resolution. The noise in a Hall plate is mainly due to thermal and flicker noise. The latter can be reduced by using the buried Hall plate, so that the silicon-oxide interface is moved away from the active region by a superficial p-type layer. Being low-pass, the flicker noise is also attenuated by the SC. On the other hand, the thermal noise, which is related to the output resistance of the Hall plate, cannot be removed.

As far as the entire HECS is concerned, also the noise from the AFE has an important role and should be added (in the power domain) to the plate noise, as they are not correlated. CCIA offers the lowest possible noise because it does not rely on resistors, minimizes the number of active elements, and employs the chopping technique to reduce the flicker noise. Finally, even the current-to-magnetic field transduction adds its own noise contribution, but the analysis of this mechanism depends on the specific magnetic arrangement. For instance, in yoke-less open-loop HECS, any mechanical vibration causes random variations of the G_{IB} factor that can be modeled as an additive noise term in (1).

4) Bandwidth: The ultimate physical limit to the BW of an Hall plate is defined by the relaxation time of the free charge carriers, which typically lays above the GHz threshold. However, a more fundamental limit is set by the resistive nature of the Hall device that, combined with the parasitic capacitances generated by the depletion region at the boundary of the n-type well, determines an equivalent time constant and related frequency pole. This limit strongly depends on the practical implementation of the probe, and it can be as high as hundreds of MHz.

Nevertheless, other capacitive effects load the Hall plate, e.g., the capacitive load of the AFE and the switches used for the SC. These define a practical BW limit that may not be exceeded in a given particular sensor design. The DDA architecture can be exploited to partially alleviate the issue by moving the switches required by the SC after the AFE [53] and by minimizing the size of the input transistors of the DDA. In addition, the SC itself limits the BW to less than $\frac{1}{4T_{spin}}$. Broader BWs can be achieved by replacing SC with passive offset compensation techniques and improving the DDA with current-feedback solutions [31], [67].

Recent broadband current sensors combine low-frequency Hall-plates with high-frequency coils or current transformers on the same silicon chip, but they feature a complex configuration and suffer from suboptimal matching of the frequency response [70], [94].

B. Sensor Behavioral Modeling

In many practical cases, one deals with commercial HECSs for which the inner sensing architecture is unknown. In these cases, it is useful to define a simplified behavioral model that could describe the global operation of the sensor at the accessible ports, so to be identified from measurements.

Several models available in the literature describe the Hall voltage V_H in (6) directly as a voltage source [56], [60]. Nevertheless, as discussed in Sec. II-A, V_H is in the first place caused by the transverse local flow of charge carriers within the Hall probe, and their consequent accumulation on the probe edges. Especially when considering the dynamic behavior of HECSs [52], the Hall voltage can be more effectively represented by the voltage drop across an equivalent resistor R_{eq} due to an equivalent Hall current I_H defined as (Fig. 12):

$$I_H = K I_{bias} B_z, \tag{21}$$

where I_H is proportional to both the out-of-plane component of the magnetic field B_z (which is, in turn, proportional to the measurand current I) and the number of charge carriers flowing within the probe (set by I_{bias}) through a global constant K embedding the physical and technological parameters of the Hall plate [52].

In this representation, the additive contribution due to the various sources of offset within the Hall probe can be suitably modeled by another current source $I_{os,plate}$, placed in parallel with I_H in Fig. 12, which results in an additive voltage offset to V_{sense}. The internal parasitic effects of the Hall-probe interconnections, as well as the input load of the AFE, influence the charge carrier accumulation on the edges of the plate. These boundary conditions, which are specific to the particular Hall probe configuration, can be globally accounted for by an equivalent capacitance (C_{eq}). This representation clearly shows the dynamic operation of the probe by highlighting the main time constant $\tau_{eq} = R_{eq}C_{eq}$, where R_{eq} is the output resistance of the Hall probe [52]. Hence, the output of the intrinsic sensor can be written as

$$V_{sense} = \frac{R_{eq}\left(I_{os,plate} + I_H\right)}{1 + j2\pi f R_{eq} C_{eq}}, \tag{22}$$

where f is the frequency. As described in Sec. III-B, V_{sense} undergoes signal conditioning by the cascaded AFE circuitry. Finally, the intrinsic circuit is complemented by adding an outer shell accounting for the unavoidable presence of external parasitic effects. The bias port features the input resistance R_{bias}, while the input port is rather modeled by the input impedance Z_{in} to account for the dynamic effects.

Eventually, the extrinsic electrical model for the HECS features three external ports: 1) the input port, through which flows the measurand current I; 2) the bias port, at which applying the bias current I_{bias}; 3) the output port, at which the output voltage (V_{out}), after AFE conditioning, can be

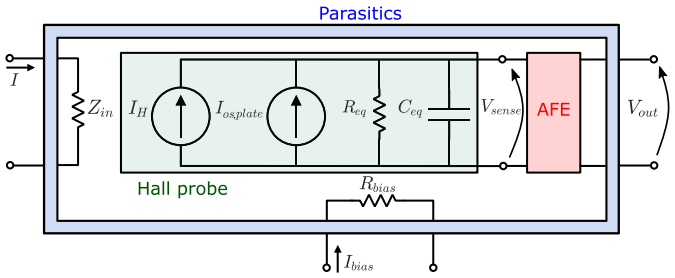

Fig. 12. Equivalent-circuit representation of the Hall-based sensor including the Hall probe.

measured. The electrical characteristics of the output port are mainly imposed by the AFE. The bias port, the AFE, and the parasitic shell could be modeled by system level descriptions or tailored equivalent circuits. Nevertheless, these will strongly depend on the actual sensor implementation, as discussed in Secs. III and IV-A.

C. Experimental Characterization

The relationship between I and V_{out} in a HECS can be described at the extrinsic reference using the generic formulation in (1). Still, the actual values of S, V_{os}, f_{nl}, and v_n account for the nonidealities of the intrinsic Hall plate and the ones due to the signal conditioning by AFE, biasing, and sensor configuration, thus they should be experimentally characterized. For each characterization, the Hall-effect sensor must be preliminarily biased at I_{bias}, while the same characterization can be repeated for different bias values.

The setup shown in Fig. 13a depicts the standard configuration for the static characterization of a HECS. The sensor is excited by a known DC current I (measurand current). For both I and I_{bias}, the applied DC current excitation should be independently measured by an amperemeter, e.g., the one embedded in a digital multimeter (DMM), to allow for an accurate calculation of the FoMs and proper FoM parametrization against the bias.

The DC current generation can be performed either by an ideal current generator, as provided by Source-Measure Units (SMUs), or by an ideal voltage source (e.g., a power supply) terminated by a resistance. In the former case, the SMU already embeds an amperemeter for current measurement. In the latter case, attention should be paid to the choice of a suitable power rating and thermal properties of the resistor, as well as to the value of the input resistance of the trace, which should be made negligible. The V_{out} is typically measured by a voltmeter, e.g., the one embedded in a high-accuracy DMM. Therefore, more than one DMM might be used in a typical setup for static characterization. Since the Hall plate is sensitive to the magnetic field, the characterization of HECSs requires an accurate magnetic setup. For yoke-based HECS, attention should be paid on the magnetic nonidealities of the yoke, like remaining magnetization, hysteresis, and perming [16]. On the other hand, yoke-less HECSs are sensitive to external fields generated by nearby currents, including the return path of the measurand current, so that they should be magnetically shielded for accurate estimation of the sensor FoMs [16]. In addition, magnetic interferences should be carefully taken into consideration for the estimation of the

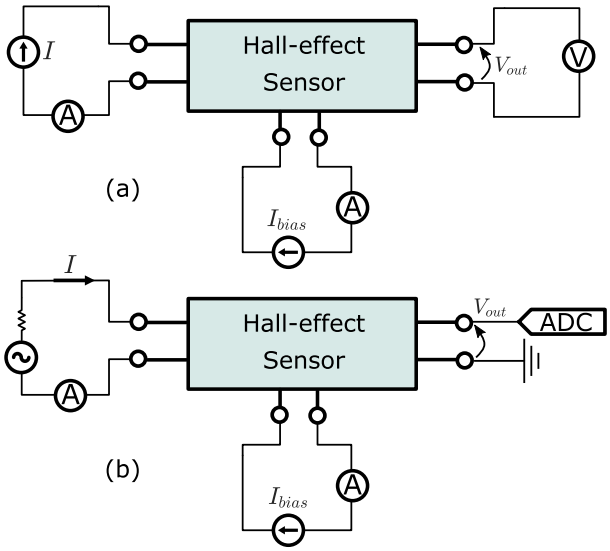

Fig. 13. Block diagram of the measurement setup for the static (a) and dynamic (b) characterization of the Hall-effect sensor.

performance in real-case scenarios. In this context, it should be mentioned that HECS with an on-chip trace imply a considerably higher distance from the sensor, thus are less sensitive to the return path, which is usually realized out of the chip.

Among the introduced FoMs, the setup in Fig. 13a can be used to extract the static value for the sensitivity S, the additive offset V_{os}, and the nonlinearity contribution f_{nl}. To characterize the static sensitivity, a set of different amplitudes for I should be applied, concurrently measuring V_{out}. Then, the sensitivity is obtained by applying a linear regression to the measured set of (I, V_{out}) pairs. Indeed, the linear regression also allows to roughly estimate the additive DC offset (V_{os}), while the deviation between the estimated linear I-V_{out} relationship and the actual measured data allows to quantify the nonlinearity contribution f_{nl}. For offset measurement, the DMM at the output port should either be a high resolution or low-input range voltmeter. To improve the estimation of the static sensitivity, as well as for providing detailed information on the nonlinearity behavior, the set of measured (I, V_{out}) pairs should be as large as possible and well distributed across the expected range.

The typical nonlinearity deviation for properly designed sensors is expected to be small (e.g., a few percent over the entire temperature range [27]). Often, the amplitude of the deviation due to nonlinearity becomes incrementally larger for larger I, allowing to define the maximum value of I corresponding to the maximum acceptable distortion due to nonlinearity. Considering on-chip Hall-effect sensors, this maximum value can be defined by physical/technological limitations (e.g., maximum current allowed on the trace or saturation of the AFE), or might be due to the self-heating of the probe at high input current levels, as shown in Fig. 14a for an Hall-effect sensor based on the four-phase SC technique [53]. Even though the input trace is characterized by very low resistance, high values of I can lead to very high power dissipation, in the order of several Watt. Therefore, temperature monitoring or control is important for the accurate characterization of the static

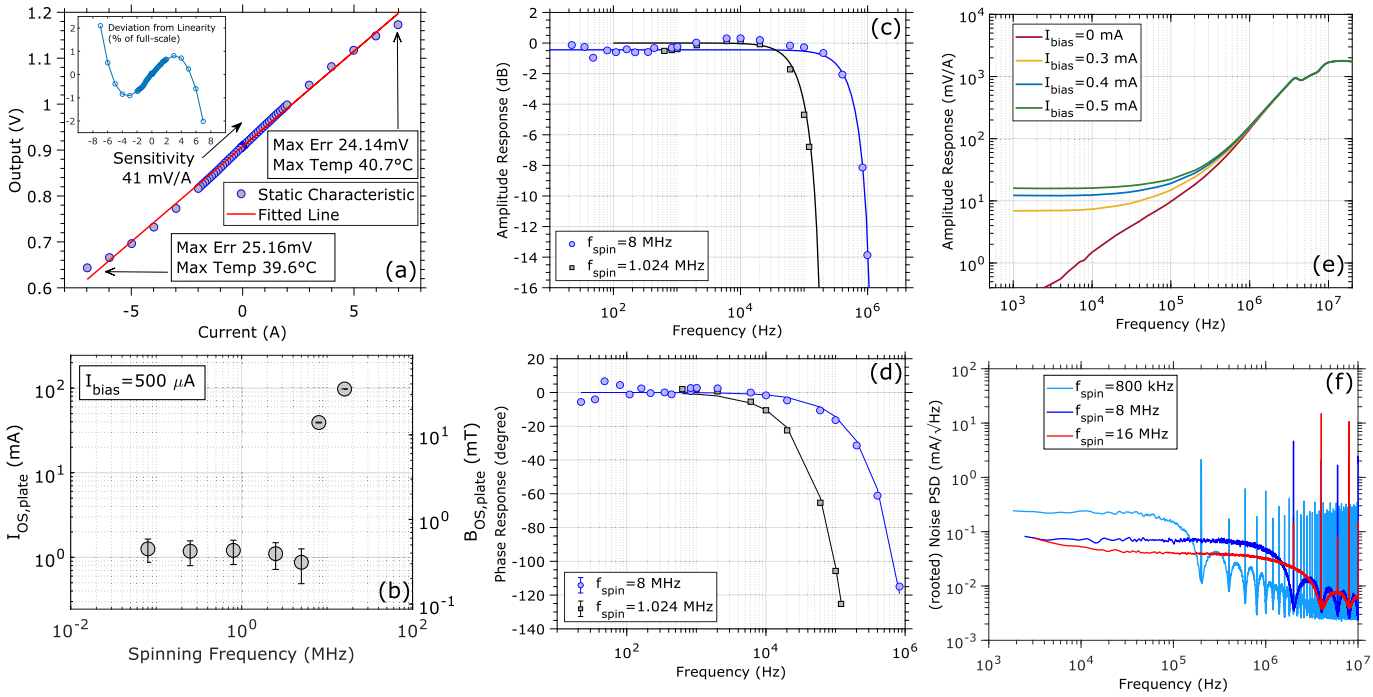

Fig. 14. Examples of characterization for HECSs highlighting the presence of nonidealities. (a) Static characteristic displaying thermal effects inducing nonlinearity (edited from [53]). The inset reports the deviation from linearity in % of the full-scale. (b) Degradation of the SC technique at high spinning frequency (edited from [53]). (c) Typical amplitude and (d) phase frequency response at two different spinning frequencies. (e) Effects of inductive parasitic on the amplitude transfer function (from [31] (© [2021] IEEE)). (f) Input-referred (rooted) noise PSD estimated at different spinning frequencies with $I = 0$ A (from [53] (© [2018] IEEE)).

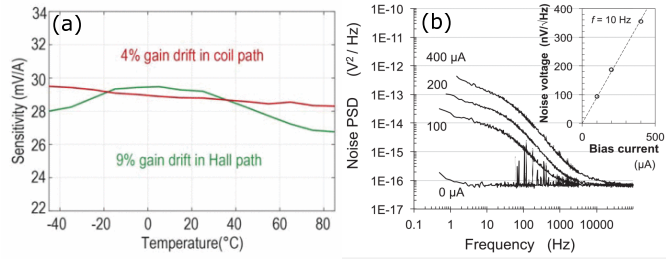

Fig. 15. (a) Temperature dispersion of the sensitivity for coil (red) and Hall (green) current sensors (from [94] (© [2021] IEEE)). (b) PSD of the LF noise of a small AlGaAs/InGaAs/GaAs-based QWHS without SC technique at different I_{bias}. The small PSD increase at $I = 0$ μA is due to the differential amplifier in the AFE. Inset: noise voltage at $f = 10$ Hz showing a linear dependence on the bias current (from [30] (© [2017] IEEE)).

parameters and their dispersion with temperature. Possibly, pulsed characterization is useful to separate the nonidealities due to self-heating only, and it is directly usable in specific applications, e.g., overcurrent protection. Nevertheless, this requires a suitable choice of the pulse timings and pulsed current generation/measurement capabilities. Figure 14b shows the absolute intrinsic DC offset of the Hall plate characterized for the sensor in [53]. It clearly demonstrates that the effectiveness of the SC technique decreases at high spinning-current frequencies, meaning that there exists a maximum operating BW limit set by the SC. Additional sources of DC offset uncertainty are the dependency on temperature as well as other long-term drifts [31].

To characterize the frequency behavior of the sensor, let us consider the setup in Fig. 13b. While the bias can be applied and measured in the same way as in Fig. 13a, the input port should be excited with an AC current. To do so, a broadband current generator can be considered. Nevertheless, since these are not common as off-the-shelf instruments, nor they are suitable for an excitation of hundreds of MHz, a power source (i.e., a voltage source with an output resistance greater than zero, typically 50 Ω) can be considered, as shown in Fig. 13b. The generated I at the input port should be characterized independently from the sensor, but DMM or SMU amperemeter functionalities are not useful in this case, as they are limited to DC or very low frequencies. Instead, another current sensor with higher accuracy w.r.t. the HECS under test should be considered, e.g., resistive-shunt current sensors or CTs. The AC output voltage must be acquired with a broadband receiver based on an Analog-to-Digital Converter (ADC), e.g., an oscilloscope channel.

The frequency response is characterized by measuring the linear transfer function of the HECS. In practice, this involves applying a swept-frequency sinusoidal current at the input, and measuring the sinusoidal voltage at the output. The applied sinusoidal current should feature a reasonably small amplitude, yet sufficiently high to obtain a satisfactory signal-to-noise ratio at the receiver. Figures 14c-d show the frequency response of the sensor in [53] for amplitude and phase, respectively. The amplitude response is normalized to the estimated DC sensitivity (see Fig. 14a). The characterization is reported at two spinning frequencies. At low frequencies, the response is flat and independent of the value of the spinning frequency, while it shows a typical roll-off at high frequencies, with 3-dB frequencies at 600 kHz and 1 MHz, respectively. Figure 14e shows the transfer function for a different HECS topology that avoids the frequency limitation

due to SC [31]. While this topology can provide broader BWs, it highlights the presence of inductive parasitics at the package level introducing a gain expansion for frequencies above the MHz range. This represents a typical example of parasitic effect that should be added in the outer shell of the black-box model of Fig. 12. In [31], it is shown that such a behavior can be compensated by low-pass filtering in post-processing. In Fig. 15a, the temperature dispersion of the sensitivity S of the QWHS HECS in [94] is reported (green line).

Finally, the setup in Fig. 13b also allows to characterize the noise power spectral density (PSD) of the sensor by applying a null I at the input. Figure 15b reports a detail on the low-frequency noise of the QWHS sensor in [30] without SC, demonstrating that the low-frequency noise in HECS is a flicker noise dependent on the bias current. Conversely, Fig. 14f shows the input-referred PSD for the sensor in [53]. In this case, it can be seen that SC cancels out the flicker noise, so that the measured noise PSD is flat for a large operating BW, from very low frequencies up to the spinning frequencies. The spikes at high frequencies are due to the up-conversion of the intrinsic offset originated by the SC.

V. Conclusion

Miniaturized and galvanic-isolated current sensing is an ever important requirement for many power electronic systems, from industrial to automotive applications. HECSs can play a major role in this context, given their reduced dimensions, low cost, and compatibility with silicon technology. However, a good HECS design encompasses many disciplines, from magnetometry to silicon device physics and analog circuit design.

This article described the principles of operation and the main implementation techniques by following the typical design flow, from the Hall plate to the mechanical/magnetic arrangement of the sensor. Particular attention was paid to the Hall plate, which is the fundamental part of the HECS, defining the major performance and nonidealities. Physical principles of the Hall effect in silicon plates were reviewed, as well as their main practical implementation challenges.

At the same time, a careful design of the AFE is essential to fully exploit the capabilities of the electronic circuits in order to compensate for the intrinsic nonidealities of the Hall plate. For example, advantages and limitations of the SC technique for offset compensation were presented and discussed. In addition, the standard arrangements exploiting a magnetic yoke, both in open-loop and closed-loop configurations, as well as yoke-less architectures with on-PCB or on-chip traces, were described and compared in terms of the transduction factor and robustness against external magnetic interferences.

Finally, this tutorial examined the modeling and characterization of HECSs. The principal nonideality effects were analyzed, with a focus on the Hall plate, but also treating aspects related to the AFE and magnetic techniques. The influence of environmental parameters, like temperature, humidity, or stress induced by the package on the sensor metrics were also discussed, reporting state-of-the-art values.

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