Variable Switching Frequency PWM for Three-Phase Four-Wire Split-Capacitor Inverter Performance Enhancement

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Variable Switching Frequency PWM for Three-Phase Four-Wire Split-Capacitor Inverter Performance Enhancement

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***Abstract*—Three-phase, four-wire, split-capacitor inverters, thanks to their capability to deal with unbalanced systems, are currently employed in photovoltaic installations, electric vehicles battery chargers, active power filters, and many other grid-tied applications. The minimization of ac output current ripple and switching losses positively impacts the inverter's efficiency, volume, weight, and cost optimization. For this reason, a novel variable switching frequency driving strategy independently tunable on each phase is proposed in this paper. Taking advantage of phase current ripple prediction, a proper variable switching frequency strategy is applied for obtaining a flat current ripple profile. Having tuned the driving strategy parameters, it is possible to optimize and compare individual metrics such as the maximum peak-to-peak value of the current ripple, current ripple rms, average switching frequency, and switching losses. By applying the proposed modulation method, a significant inverter performance enhancement has been obtained. Converter efficiency is improved without introducing detrimental effects on the current harmonic quality. Analytical derivations are expressed as a modulating index function and the power factor for balanced and unbalanced systems. All the theoretical developments are verified throughout numerical simulations and experimental tests.**

I. Introduction

Three-phase four-wire, voltage-source inverters (VSIs) with the inherent capability of handling homopolar current has become popular in power applications such as grid-forming inverters, active rectifiers, active filters, renewable energy sources, electric drives, and electric vehicle ancillary services [1]–[7]. Among the multiple neutral forming topologies, split-capacitor and four-leg are collecting most of the nowadays' interest. In both cases, extending standard three-phase inverter flexibility and control simplicity by increasing the independency grade across phases is possible. Setting the dc-link midpoint voltage, split-capacitor three-phase four-wire VSIs behave as three parallel half-bridge inverters having decoupled phases (without neutral inductor) [1]–[4]. On the other hand, the four-leg solution shifts the operations towards a topology made out of three parallel H-bridge inverters sharing the neutral leg (without neutral inductor) [5]–[7]. Since four-leg topology presents the possibility to inject common-mode signals, typical three-wire pulse-width modulation (PWM) schemes like space vector modulation (SVM) and discontinuous PWM (DPWM) can be employed as well. In this way, modulation effectiveness and VSI global efficiency can be increased [7], [8]. Differently from the four-leg inverter, a split-capacitor solution, here analyzed, can independently tune legs switching frequency following specific criteria.

Even though carrier-based schemes, which employ constant switching frequency PWM (CSF-PWM), can be effortlessly realized, they introduce a set of drawbacks such as high switching losses, narrowband harmonic clusters, unevenly distributed switching current, and torque ripple within the fundamental period, and acoustic noise [9]. For this reason, solutions as DPWM, random PWM (RPWM), random DPWM (RDPWM), variable switching frequency PWM (VSF-PWM), and DPWM-based variable switching frequency (VSF-DPWM) have been employed to mitigate those detrimental effects [7], [9]–[16]. Although in [7] four-leg inverters' switching losses and current ripple amplitude performances have been enhanced thanks to proper usage of DPWM, the harmonic spectrum preserves a narrowband cluster distribution. In [11], [12], RPWM is obtained by acting on the pulse disposition and switching frequency distribution, respectively. Thanks to the relevant harmonic spreading effect over the entire spectrum, it is possible to mitigate acoustic pollution [13] significantly. However, real-time switching losses control results to be particularly complex [9]. As shown in [14], RDPWM joins the strengths of DPWM and RPWM, ensuring a broadband spectrum and significant switching losses reduction. On the other hand, VSF-PWM has been used in [17]–[20] with the primary aim of reducing current and voltage switching ripple, improve electromagnetic compatibility (EMC), or ensuring

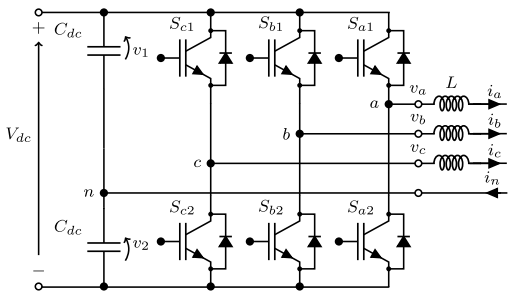

Fig. 1. Circuit scheme of a three-phase, four-wire, split-capacitor VSI.

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soft-switching conditions, respectively. Thanks to VSF-PWM, the switching frequency can be varied according to the current ripple prediction/measurement, the ripple envelope shaping, and filtering stage requirements [17], [21], [22]. In [23], a multipurpose family of switching frequency driving profiles is presented. The VSF-PWM range of applications has been extended considering magnetics saturation through virtual inductance identification procedure [24]. Authors in [16] have improved hybrid Si/SiC half-bridge converter efficiency using two different switching frequency patterns for different fundamental current values. A similar technique is carried out in [25] for both unipolar and bipolar PWM. In [15], the benefits guaranteed by DPWM and VSF-PWM are joined together to optimize switching losses, and harmonic performances of two parallel interleaved three-phase inverters operated in VSF-DPWM. Since RDPWM cannot be implemented on split-capacitor VSIs, because of the lacking common-mode injection possibility, VSF-PWM that can be independently tuned for each leg is the most promising solution in contrast to CSF-PWM drawbacks described above.

Concerning three-phase, four-wire, split-capacitor inverter (Fig. 1), voltage switching ripple formulations for balanced and unbalanced systems have been introduced in [3]. On the other hand, split-capacitor inverter complete phase current ripple peak-to-peak and rms analysis has been proposed in [4]. Furthermore, an interleaved approach capable of mitigating neutral current ripple in the split-capacitor inverter is available in [2]. It effectively relays on the current ripple cancellation effect granted by the unsynchronized pulse disposition. However, all these studies are available for CSF-PWM only. Most VSF-PWM contributions are applied to the standard three-phase, three-wire VSIs [24], [26], [27]. Even though the VSF-PWM strategy of [17] could be applied to four-wire, split-capacitor inverter, phase independency degree of freedom is not employed, leading to an only marginally optimized inverter design and control.

The primary aim is to introduce a variable switching frequency PWM strategy for three-phase, four-wire, split-capacitor inverters that allows adjusting switching pattern in each phase independently. The resulting VSF-PWM guarantees performance improvements in terms of ac current ripple and switching losses. Taking advantage of phase independence, it is possible to tune a switching frequency profile, ensuring a considerable reduction of ac current harmonic pollution in balanced and unbalanced systems. Moreover, switching losses can be minimized regardless of the system power factor, equally valid in grid-connected or load-driving applications ensuring notable efficiency improvement.

To formalize the proposed VSF-PWM scheme, the following methodology has been applied. Firstly, the phase current ripple envelope in the CSF-PWM regime is predicted within one fundamental cycle. Secondly, based on this information, a VSF-PWM strategy capable of forcing the current ripple to have a flat profile within a fundamental period is introduced. Finally, the designed VSF-PWM technique has been configurated for obtaining multiple performance optimizations. In detail, metrics such as average switching frequency, current ripple maximum peak-to-peak, current ripple rms, and switching losses are equalized to their counterparts given by CSF-PWM, enabling fair comparison with the proposed strategy.

Generic analytical formulations defined as a function of the modulation index and the power factor permit precise knowledge of the inverter performances. Together with the rigorous analysis of phase current ripple peak-to-peak, current ripple rms, and switching losses, qualitative considerations on the neutral current ripple performances are proposed here as well. Relevant characteristics have been compared with their correspondences from the standard three-phase, three-wire inverter. It can be pointed out that, under certain conditions, the selected topology can achieve performance similar or even better than the three-wire counterpart in both balanced and unbalanced systems. Moreover, harmonic spectrum and efficiency curves comparing the proposed VSF-PWM and the CSF-PWM are provided.

Section II introduces practical assumptions and definitions. Section III provides a current ripple prediction in CSF-PWM. The proposed VSF-PWM strategy is described in Section IV. Findings are numerically validated and discussed in Section V. Section VI introduces experimental results. Finally, Section VII concludes the paper.

II. Basic Assumptions and Definitions

The considered circuit scheme, presented in Fig. 1, consists of a three-phase, four-wire, split-capacitor inverter. Similar to the standard three-phase three-wire VSI, phases are connected to three identical legs by three magnetically independent ac-link filter inductors L (assumed to be constant at this stage). The additional neutral wire is directly connected to the midpoint of the dc-link (split) capacitors.

Since the neutral point is directly connected to the split-capacitor midpoint, no common-mode injection might be considered, and therefore only sinusoidal pulse-width modulation (SPWM) can be implemented. This means that the only modulation scheme capable of enhancing inverter performances is the VSF-PWM because it can work on the carrier level rather than the modulating signal one. The generic modulating signal u_x employed in carrier-based PWM inverters is given by:

$$u_x(\vartheta_x) = m_x \cos(\vartheta + \varphi_x) = m_x \cos(\vartheta_x) \qquad (1)$$

with x the phase index (a, b, c), φ_x and ϑ_x phase angles, $\vartheta = 2\pi ft$ with f the fundamental (grid) frequency, and m_x the

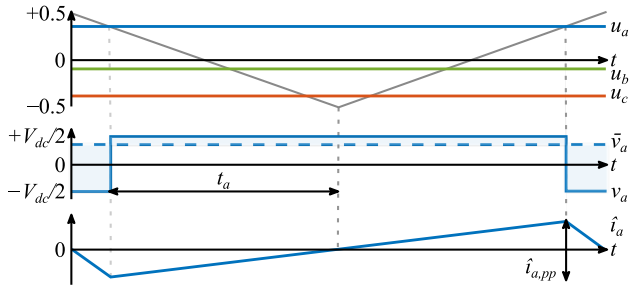

Fig. 2. Carrier and modulating signals (top), phase a voltage with its averaged value (middle) and phase a current ripple (bottom) in the switching period T_{sw}.

modulation index defined as the ratio between the reference phase voltage amplitude and the dc-link voltage V_{dc}. The carrier ranges from −0.5 to +0.5, and the corresponding linear modulation range is limited to m_x = [0, 0.5]. The main PWM signals are summarized in Fig. 2 (top).

The ac current ripple is the integral of the instantaneous difference between the inverter output voltage v_x and the sinusoidal reference voltage $\bar{v}_x$ (filled area in Fig. 2). By neglecting the voltage drop on the resistance R, the current ripple $\hat{\imath}_x$ can be computed as:

$$\hat{\imath}_x(\vartheta_x) \cong \frac{1}{L}\int [v_x(\vartheta_x) - V_{dc}u_x(\vartheta_x)]d\vartheta_x \tag{2}$$

The peak-to-peak current ripple over switching period T_{sw} can be defined as:

$$\hat{\imath}_{x,pp}(m_x,\vartheta_x) = \max\left[\hat{\imath}_x(t)|_{T_{sw}}\right] - \min\left[\hat{\imath}_x(t)|_{T_{sw}}\right] \tag{3}$$

All the analytical findings are normalized through the normalization base $V_{dc}/(2\,L\,f_{sw})$. In this way, the final equations are independent of circuit parameters.

III. Phase Current Ripple Prediction in CSF-PWM

In this Section, the current ripple in the case of CSF-PWM is predicted. As will be discussed later, the current ripple represents the joining ring between harmonic pollution and converter efficiency. This implies that the current ripple prediction and control is the starting point for obtaining optimizations in terms of converter, size, weight, and cost.

$$t_x(\vartheta_x) = \frac{1}{2f_{sw}}\left[\frac{1}{2} + u_x(\vartheta_x)\right] \tag{4}$$

Based on Fig. 2, and considering the modulating signals introduced in (1), the time intervals t_x are expressed as (4).

Similar to what has been done in [4], having in mind (2) and (3), peak-to-peak current ripple can be determined by equation (5). The latter can be normalized by giving equation (6).

$$\begin{aligned}\hat{\imath}_{x,pp}(m_x,\vartheta_x)\big|_{CSF} &= \frac{V_{dc}}{L}[1-2u_x(\vartheta_x)]t_x(\vartheta_x)\\ &= \frac{V_{dc}}{2Lf_{sw}}\left[\frac{1}{2} - m_x^2 - m_x^2\cos(2\vartheta_x)\right]\end{aligned} \tag{5}$$

$$\hat{r}_{x,pp}(m_x,\vartheta_x)\big|_{CSF} = \frac{1}{2} - m_x^2 - m_x^2\cos(2\vartheta_x) \tag{6}$$

The normalized value of maximum peak-to-peak current ripple, shown in (7), always occurs when (6) is evaluated at $\vartheta_x = \pm\pi/2$, while the variation of the modulation index does not affect.

$$\hat{r}_{x,pp}^{max}(m_x)\big|_{CSF} = \hat{r}_{x,pp}\left(m_x, \pm\frac{\pi}{2}\right)\Big|_{CSF} = \frac{1}{2} \tag{7}$$

Based on previous analysis, the instantaneous phase current ripple always presents as a triangular waveform having a peak-to-peak magnitude given by (5). Therefore, the normalized current ripple rms can be calculated as:

$$\begin{aligned}\hat{R}_x(m_x)\big|_{CSF} &= \frac{1}{2\sqrt{3}}\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\hat{r}_{x,pp}(m_x,\vartheta_x)\big|_{CSF}\right]^2 d\vartheta_x}\\ &= \frac{\sqrt{1-4m_x^2+6m_x^4}}{4\sqrt{3}}\end{aligned} \tag{8}$$

Switching losses accumulated by a generic leg over one fundamental cycle can be approximated as in:

$$\begin{aligned}&P_{x,sw}(m_x,\varphi_x)\big|_{CSF}\\ &= \frac{k_s f_{sw} V_{dc} t_c}{2\pi}\int_0^{2\pi} |I_x\cos(\vartheta_x+\varphi_x)|d\vartheta_x\end{aligned} \tag{9}$$

where t_c represents the total commutation time (t_{on}+t_{off}), k_s is a shape factor usually ranging from 1/6 to 1/2, and I_x is the maximum phase current value [28], [29]. By normalizing (9) with the base ($2\,k_s f_{sw}\,V_{dc}\,t_c\,I_x$) /π, it is possible to obtain:

$$S_{x,sw}(m_x,\varphi_x)\big|_{CSF} = \frac{1}{4}\int_0^{2\pi}|\cos(\vartheta_x+\varphi_x)|d\vartheta_x = 1 \tag{10}$$

As expected, switching losses are phase angle φ_x independent in the case of CSF-PWM.

Following the approach of [24], replacing L with the concept of 'virtual inductor', current ripple envelope deformation caused by magnetics saturation can be considered. This procedure could be particularly beneficial in powder core inductors and ac drive applications [30]–[32]. Therefore, the VSF-PWM technique proposed in the next Section can be employed whether the converter is operating in saturation or not (typically avoided in rated conditions).

IV. Variable Switching Frequency PWM (VSF-PWM)

Taking advantage of the phase independence guaranteed by split-capacitor topology, a novel variable switching frequency PWM strategy exclusively tunable in each phase leg is proposed here. Differently from [17], the new modulation method restricts in each phase a particular value of the current ripple peak-to-peak $\hat{\imath}_{x,ref}$ utilizing a switching frequency profile f_x that is defined for each phase as:

$$f_x(m_x,\vartheta_x)|_{VSF} = f_{sw}\frac{\hat{\imath}_{x,pp}(m_x,\vartheta_x)\big|_{CSF}}{\hat{\imath}_{x,ref}(m_x)} \tag{11}$$

The normalized switching frequency ρ_x is introduced as:

$$\rho_x(m_x,\vartheta_x)|_{VSF} = \frac{f_x(m_x,\vartheta_x)|_{VSF}}{f_{sw}} = \frac{\hat{\imath}_{x,pp}(m_x,\vartheta_x)\big|_{CSF}}{\hat{\imath}_{x,ref}(m_x)} \tag{12}$$

Setting the current ripple reference value $\hat{\imath}_{x,ref}$ (that is time-independent), the current ripple profile resulting from the proposed VSF-PWM is forced to be completely flat over the whole fundamental cycle. It can be demonstrated that, based on the ripple prediction shown in (6), the only function capable of producing a flat current ripple profile is:

$$\begin{aligned}\rho_x(m_x,\vartheta_x)|_{VSF} &= k(m_x)[1-\delta_x(m_x)\cos(2\vartheta_x)]\\ &= k(m_x)\left[1 - \frac{2m_x^2}{1-2m_x^2}\cos(2\vartheta_x)\right]\end{aligned} \tag{13}$$

where δ_x is the maximum relative frequency deviation, and k is a gain parameter.

In the following Subsection, to have a fair evaluation of benefits of the new VSF-PWM, this modulation strategy (13) is updated, amending the gain k to equalize metrics such as average switching frequency, switching losses, current ripple rms, and maximum peak-to-peak current ripple with the ones shown by CSF-PWM in Section III. In this way, as will be later illustrated in Section V, findings are discussed and validated, demonstrating the proposed VSF-PWM technique's performance in contrast with standard CSF-PWM and already available VSF-PWM basic implementation.

A. Effects of VSF-PWM

Since the normalized current ripple peak-to-peak of (6) is inversely proportional to the switching frequency f_{sw}, the VSF-PWM impact on the latter can be measured by dividing (6) by (13) observing:

$$\hat{r}_{x,pp}(m_x)\big|_{\mathrm{VSF}} = \frac{\hat{r}_{x,pp}(m_x,\vartheta_x)\big|_{CSF}}{\rho_x(m_x,\vartheta_x)|_{VSF}} = \frac{1-2m_x^2}{2k(m_x)} \tag{14}$$

which, being the current ripple profile flat, always coincide in each instant of the fundamental period with the maximum peak-to-peak. Comparing (14) with (7), it appears that VSF-PWM maximum peak-to-peak can be sensibly lower if compared with CSF-PWM one.

The rms can be directly derived from (14) as:

$$\hat{R}_x(m_x)\big|_{\mathrm{VSF}} = \frac{\hat{r}_{x,pp}(m_x)\big|_{\mathrm{VSF}}}{2\sqrt{3}} = \frac{1-2m_x^2}{4\sqrt{3}k(m_x)} \tag{15}$$

which, similarly to (14), by proper tuning of VSF-PWM parameters can lead to current ripple rms reduction compared to CSF-PWM value.

$$\begin{aligned} &S_{x,sw}(m_x,\varphi_x)\big|_{VSF} \\ &= \frac{1}{4}\int_0^{2\pi} \rho_x(m_x,\vartheta_x)|_{VSF}|\cos(\vartheta_x+\varphi_x)|d\vartheta_x \\ &= k(m_x)\left[1-\frac{2m_x^2\cos(2\varphi_x)}{3-6m_x^2}\right] \end{aligned} \tag{16}$$

By substituting (13) in (10), the normalized switching losses can be computed by (16). Since the switching frequency profile is linked with the modulating signal rather than the current fundamental, different power factors provide different switching losses.

From formulations (13)-(16), one can derive the value which the gain k should assume for obtaining the metrics equalization introduced above. From (13), it can be directly seen that replacing $k|_\rho = 1$ ensures a unity normalized average switching frequency, enabling a fair comparison with the CSF-PWM method. Furthermore, reversing (14) and replacing $\vartheta_x = \pm\pi/2$, the equalization gain for obtaining the same maximum peak-to-peak values of current ripple can be defined as:

$$k(m_x)|_{pp} = \frac{1-2m_x^2}{2\,\hat{r}_{x,pp}^{max}(m_x)\big|_{CSF}} = 1-2m_x^2 \tag{17}$$

Following a similar procedure, the current ripple rms equalization can be obtained employing (18).

$$k(m_x)|_{rms} = \frac{1-2m_x^2}{4\sqrt{3}\,\hat{R}_x(m_x)\big|_{CSF}} = \frac{1-2m_x^2}{\sqrt{1-4m_x^2+6m_x^4}} \tag{18}$$

$$\begin{aligned} k(m_x,\varphi_x)|_l &= \frac{S_{x,sw}(m_x,\varphi_x)\big|_{CSF}\,(3-6m_x^2)}{3-[6+2\cos(2\varphi_x)]m_x^2} \\ &= \frac{3-6m_x^2}{3-[6+2\cos(2\varphi_x)]m_x^2} \end{aligned} \tag{19}$$

Finally, for obtaining identical normalized switching losses concerning CSFPM, k in (16) should be replaced by (19). It is worth mentioning that in the case of $\varphi_x = \pm\pi/4$, the gain k becomes equal to one. In other terms, assuming the same switching losses (when $\varphi_x = \pm\pi/4$) is equivalent to the instance with the identical average switching frequency, as already has been discussed above.

All the gains k proposed above are considered in Section V enabling fair comparison with CSF-PWM for all the metrics analyzed above.

B. Limited Switching Frequency Span Operations

From (13), it can be readily noticed that when $m_x = 0.5$, δ_x becomes equal to one, ideally leading the normalized switching frequency ρ_x to able to range from 0 to $2k$. Therefore, for high values of modulating index m_x, frequency deviation δ_x should be restricted to confine the switching frequency above a preset limit value f_{lim} (indicated as ρ_{lim} in its normalized form). In the physical meaning, this limitation sets upper and lower boundaries of switching frequency variation span. Moreover, standards like IEC 61000-3-2 and IEEE Std 519-2014 suggest limiting the VSF-PWM operations above 2 kHz and 2.5 kHz, respectively. This effect can be seen from Fig. 3 to Fig. 6 for modulation index higher than m_t. The maximum frequency deviation, from a specific value of modulation index m_t, becomes:

$$\delta'_x(m_x) = 1-\frac{\rho_{\mathrm{lim}}}{k'(m_x)} = 1-\frac{1}{k'(m_x)}\frac{f_{\mathrm{lim}}}{f_{sw}} \tag{20}$$

During limited operation, the flat current ripple profile guaranteed by (13) cannot be preserved. For maintaining equalization of switching losses and maximum peak-to-peak values of current ripple, the gain k should be respectively updated to (21) and (22).

$$k'(m_x)|_l = \frac{3-\rho_{\mathrm{lim}}\cos(2\varphi_x)}{3-\cos(2\varphi_x)} \tag{21}$$

$$k'(m_x)|_{pp} = \frac{1+\rho_{lim}}{2} \tag{22}$$

Conversely, the gain $k|_\rho = 1$ ensures the same average switching frequency in limited operations as well. On the other hand, gain for obtaining the same rms of current ripple given by CSF-PWM has not be presented here because it would result in a notably bulky formulation. For this reason, all the findings are obtained considering the same gain $k|_{\mathrm{rms}}$ presented in (18). The switching frequency span is limited in the range $k'(1 \pm \delta')$. The effects on normalized switching frequency attributes are visible from Fig. 3 to Fig. 6 at $m_x > m_t$.

The maximum peak-to-peak value of the current ripple, switching losses, and rms of the current ripple can be calculated by employing (23), (24), and (25), respectively.

$$\hat{r}_{x,pp}^{max}(m_x)\big|_{VSF} = \frac{1}{2k(m_x)[1+\delta_x(m_x)]} \tag{23}$$

$$S_{x,sw}(m_x,\varphi_x)\big|_{VSF} = \frac{k(m_x,\varphi_x)}{3}[3-\delta_x(m_x)\cos(2\varphi_x)] \tag{24}$$

It is worth noticing that (23)-(25) are expressed considering completely generic notation, and can be freely employed in the whole modulation index m_x span [0, 0.5].

$$\hat{R}_x(m_x)\big|_{\mathrm{VSF}} = \frac{1}{4\sqrt{3}}\frac{1}{k(m_x)}\frac{\sqrt{\delta_x(m_x)^2-4m_x^2[1+\delta_x(m_x)]\left\{\delta_x(m_x)^2[1-2m_x^2]+m_x^2[1-\delta_x(m_x)]\left[1-\sqrt{1-\delta_x(m_x)^2}\right]\right\}}}{\delta_x(m_x)\sqrt[4]{[1-\delta_x(m_x)^2]^3}} \tag{25}$$

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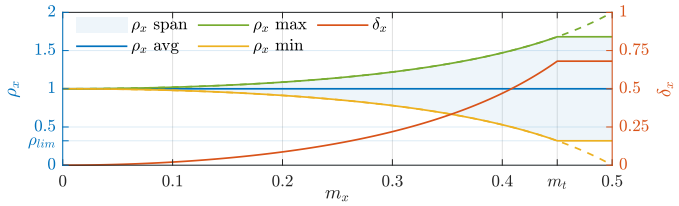

Fig. 3. Normalized switching frequency ρ_x attributes in case of VSF-PWM in average switching frequency equalization.

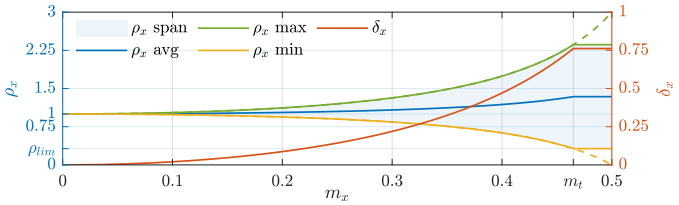

Fig. 4. Normalized switching frequency ρ_x attributes in case of VSF-PWM in switching losses equalization at PF = 1.

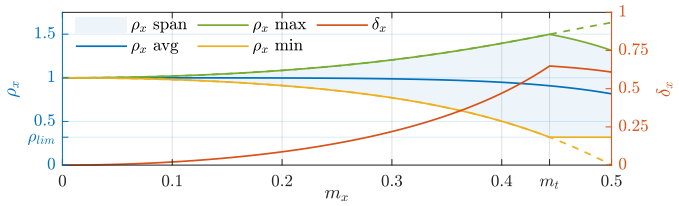

Fig. 5. Normalized switching frequency ρ_x attributes in case of VSF-PWM in current ripple rms equalization.

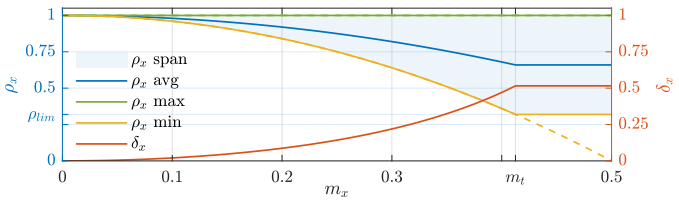

Fig. 6. Normalized switching frequency ρ_x attributes in case of VSF-PWM in maximum current ripple peak-to-peak equalization.

C. Switching Frequency Span in VSF-PWM

From Fig. 3 to Fig. 6, the variable switching frequency attributes are depicted for average switching frequency, switching losses, current ripple rms, and current ripple maximum peak-to-peak equalizations, respectively. The frequency span that each strategy ranges every fundamental cycle is indicated as 'ρ_x span'. The latter is bounded by maximum ('ρ_x max') and minimum ('ρ_x min') normalized switching frequency traces. During the whole modulation index m_x interval, the maximum and minimum normalized value of switching frequency can be obtained using $k\,(1 \pm \delta)$. As visible and explained in the previous Subsection, to confine the switching frequency above a preset limit value ρ_{lim}, the maximum normalized frequency deviation δ_x is limited for $m_x > m_t$. Theoretical traces are depicted with dashed lines. Current Subsection's plots always show the variable switching frequency's average value as 'ρ_x avg'. It can be demonstrated that the normalized average switching frequency numerically coincides with the gain k employed in each strategy.

Fig. 3 displays the normalized switching frequency profile's main attributes in average switching frequency equalization. As demonstrated, for high values of m_x, 'ρ_x span' approaches the theoretically limit ±100% of its average value. For small values of modulation index m_x, maximum ('ρ_x max') and minimum ('ρ_x min') normalized switching frequency traces remain close to the average value ('ρ_x avg'). Fig. 4 shows the main characteristics of normalized switching frequency profile in case of switching losses equalization. Differently from the previous instance, normalized switching frequency maximum value ('ρ_x max') could theoretically triplicate (+200%) the average value ('ρ_x avg') at $\varphi_x = 0$. Fig. 5 depicts the main features of normalized switching frequency profile setting rms of ac current ripple equal among the compared modulation methods. As soon as the modulation index m_x increases, the average switching frequency decreases. Fig. 6 shows the main attributes of normalized switching frequency profile in the current ripple maximum peak-to-peak equalization. In this regard, the switching frequency span remains confined to values always smaller or equal to the switching frequency f_{sw} employed in CSF-PWM. Overall, drawings of Fig. 3-Fig. 6 might be used as a reference for setting VSF-PWM operation boundaries. Even though there is no mathematical limitation in the maximum switching frequency (differently from the minimum one discussed in Section IV.B.), the technological limit of the switches, microcontroller clock frequency, and electromagnetic compatibility (EMC) restriction (especially above 150 kHz) might introduce the operation upper boundary.

D. VSF-PWM Digital Implementation

The above presented PWM strategy is synthesized in Fig. 7. The algorithm is generic and can be employed for generating PWM patterns in both CSF-PWM and VSF-PWM. Once the working mode is selected, parameters like k and δ_x are set according to the targeted metric optimization (maximum peak-to-peak, rms, average switching frequency, and switching losses equalization). As visible, the proposed VSF-PWM technique should be seen as a logical layer executed together with PWM pattern generation. Part of the technique inputs come from the inverter controller (regardless of the type) without influencing it. In this way, both open- and close-loop operations are enabled. Being each leg independent, no computation effort should be dedicated in the three carrier's synchronization as it usually happens in CSF-PWM. Although most of the high-level code deployment, numerical simulation, and hardware in the loop (HIL) environments support by default the real-time setting of the switching period/switching frequency, a slightly higher level of implementation complexity of the VSF-PWM compared to CSF-PWM is undeniable.

For the experimental results of Section VI, the block 'ePWM'

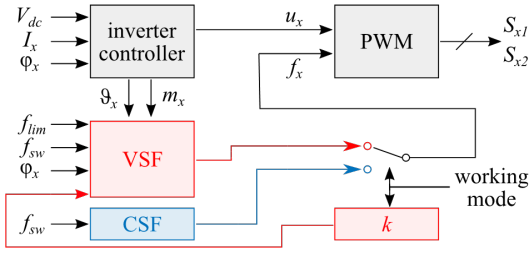

Fig. 7. Digital implementation algorithm in case of CSF-PWM and VSF-PWM.

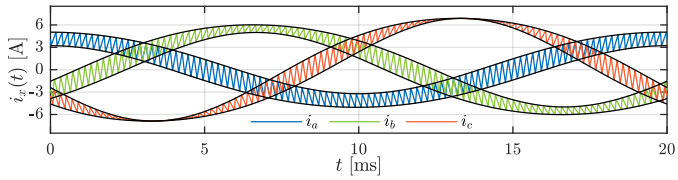

Fig. 8. Phase currents of the three phases in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ with calculated envelopes in case of CSF-PWM modulation technique.

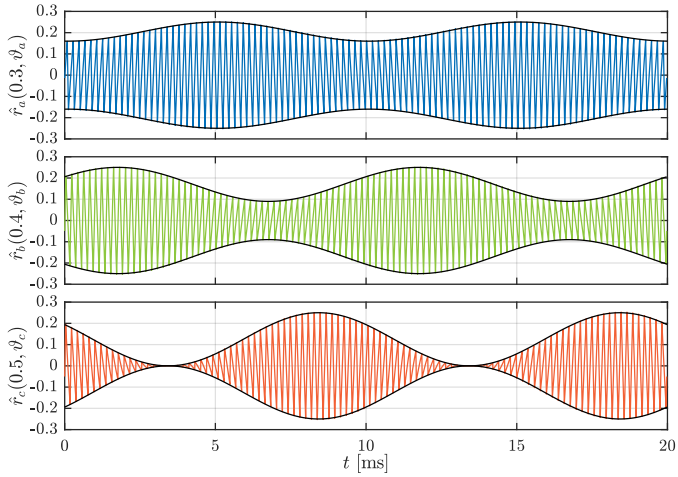

Fig. 9. Normalized current ripple profiles for the three phases in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ with calculated envelopes in case of CSF-PWM modulation technique.

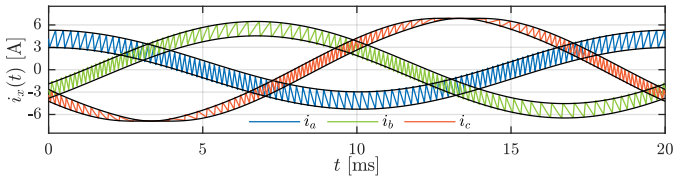

Fig. 10. Phase currents for the three phases in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ with calculated envelopes in case of VSF-PWM average switching frequency equalization modulation technique.

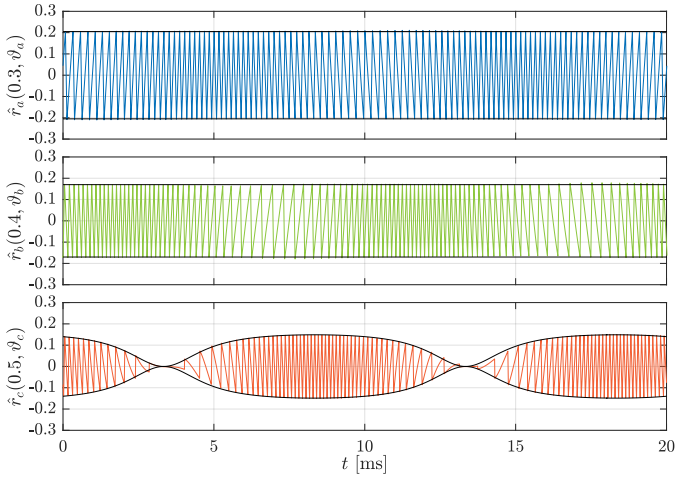

Fig. 11. Normalized profiles of current ripple for the three phases in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ with calculated envelopes in case of VSF-PWM average switching frequency equalization modulation technique.

available in the 'Embedded Coder Support Package for Texas Instruments C2000 Processors' block set for Simulink (MathWorks) has been used.

V. Findings Validation and Discussion

To verify the theoretical developments and the proposed VSF-PWM technique presented in the previous sections, numerical simulations are carried out in MATLAB/Simulink (MathWorks) environment. The circuit model (Fig. 1) has been built considering the same unity power factor *RLC* three-phase load of [7] to emulate a typical grid-connected working condition. The circuit model has been set with the actual setup parameters given in Table II.

The simulation results presented in Fig. 8 and Fig. 9 show the three-phase currents and the three-phase normalized current ripples in the case of CSF-PWM, respectively. Similarly, Fig. 10 and Fig. 11 illustrate the three-phase currents and the three-phase normalized current ripples in the case of VSF-PWM average switching frequency equalization, respectively. These plots are obtained by setting $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ under CSF-PWM and VSF-PWM modulation schemes. In this way, multiple meaningful cases at different values of m are validated. However, it should be noted that in actual applications (especially grid-connected), uneven phase power allocation can be achieved with less severe modulation indexes unbalances. Therefore, the extreme case here depicted should be intended for the sole sake of representation in mind to show three meaningful cases. Upper and lower envelopes correspond to half of the peak-to-peak values given in (6) and (14). As expected, the simulation results demonstrate an excellent match between the derived equations and simulation results for both CSF-PWM and VSF-PWM. As Fig. 10 displays, low-frequency components in VSF-PWM are precisely the same as for CSF-PWM (Fig. 8), although each leg uses a different variable switching frequency function f_x. Differently from the CSF-PWM case (Fig. 9), phase *a* and *b* current ripple framings seen in Fig. 11 convincingly demonstrate the expected flat profile. On the other hand, phase *c* ($m_c = 0.5$) is in a limited variable switching frequency operation. Consequently, the flat current ripple profile is lost, although a relevant ripple reduction is still introduced. In Fig. 12, VSF-PWM effects can be evaluated on the harmonic spectra of phase voltage and current. As expected, in both cases, the harmonic clusters for VSF-PWM result to be smoother than the one of CSF-PWM. Although the minimum frequency (in the specific case depicted in Fig. 12) is lower than the one of CSF-PWM, VSF-PWM

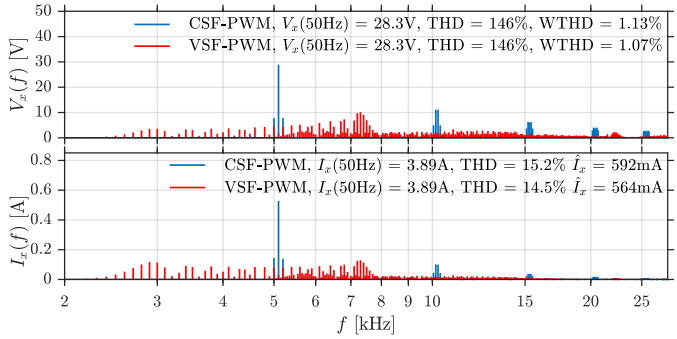

Fig. 12. Harmonic spectra of phase voltage (top) and current (bottom) in case of CSF-PWM and VSF-PWM (same average switching frequency), $m_x = 0.4$.

ensures a voltage spectrum having density shifted towards higher frequencies. This feature is reflected in a lower weighted THD (WTHD), although the voltage THD is unchanged, being a two-level topology [33]. Thus, the current ripple appears to be mitigated, as visible in both rms and THD reductions. Even though no harmonized standard regulates the frequency span ranging from 2 kHz to 150 kHz (supraharmonics [29] usually employed for switching operations), it can be seen that the VSF-PWM spectrum has harmonics with lower magnitude in comparison to the case of CSF-PWM. As mentioned in Subsection IV.C, harmonic magnitude diminishing, density shifting, and clusters broadening can be freely tuned by acting on the maximum frequency deviation δ (defined in (20)). In this way, a spectrum closer to the one experienced by CSF-PWM can be obtained, opening to a precise trade-off between specific EMI filter specification and VSF-PWM effectiveness.

Performance comparison between the proposed VSF-PWM and standard CSF-PWM can be seen in Fig. 13. The normalized maximum peak-to-peak value of the current ripple (top plot) and its rms (bottom plot) are depicted for all the cases examined in Sections III and IV. Numerical results (labeled as 'sim.') verify the analytical computations in both flat and limited switching frequency regions. The ideal profile that there would be without limiting the switching frequency is displayed with dashed lines. Each metric equalization is indicated using the same notation introduced in Section IV. Therefore, in each frame, there is one trace referring to CSF-PWM ('CSF') and a set of traces depicting the proposed VSF-PWM implemented using multiple values of k ('*pp*', '*rms*', 'ρ', and '*l*1').

In detail, the dotted trace in Fig. 13 (top plot) demonstrates that strategy (labeled as '*pp*') provides the same maximum peak-to-peak current ripple performance of the CSF-PWM (Section III). Conventional three-phase, three-leg (SPWM) structure ('3*leg*') outperforms the four-wire, split-capacitor topology in most points of the modulation index range. However, starting from about $m = 0.45$, the presented family of VSF-PWM strategy starts to have better, or at least comparable, performance in relation to the classical three-leg inverter. Split-capacitor converter working in CSF-PWM ('CSF') is outperformed by VSF-PWM techniques with a reduction of the maximum peak-to-peak magnitude of current ripple (at $m = 0.5$) theoretically reaching −67% in case of switching losses equalization for unity power factor. When average switching frequency ('ρ') and rms of current ripple ('rms') equalizations are applied, the reduction is about −50% and −39%, respectively. Limiting switching frequency operational span (Subsection IV.B) introduces detrimental effects on the maximum peak-to-peak current ripple reduction capability compared to the values stated above. However, as (23) suggests, a power switch technology that can guarantee a wide switching frequency excursion (for instance, GaN- and SiC-based) can shift the limited operations towards higher values of modulation index m_x, providing results close to ideal (dashed traces).

Concerning Fig. 13 (bottom plot), the dotted trace represents the approach of current ripple rms equalization with the CSF-PWM trace ('CSF') in the flat profile region. As explained in Subsection IV.B, once the limited switching frequency operation occurs, the tracking is lost. However, differently from Fig. 13 (top plot), this kind of operation does not introduce detrimental effects. Indeed, the ripple profile at $m_c = 0.5$ (Fig. 11) ensures the lower rms of current ripple (compared with non-limited operation) because the restricted VSF-PWM can smooth down the envelope to the values closer to the zero-magnitude level. Non-restricted traces (dashed) closely follow the actual ones (solid lines). This kind of behavior also enables narrow switching frequency span technologies (like Si-based) to provide relevant improvements in terms of rms of the current ripple. The only strategy that can reach the three-leg inverter's performance is the switching losses equalization with unity power factor operation ('*l*1'). The current ripple rms evaluations here presented can be readily used for calculating total demand distortion (TDD), total harmonic distortion (THD), weighted THD (WTHD), and distortion index (DIN).

Normalized switching losses $S_{x,sw}$ are depicted in Fig. 14 for power factors equal to 1 (top plot), 0.8 (middle plot), and 0.6

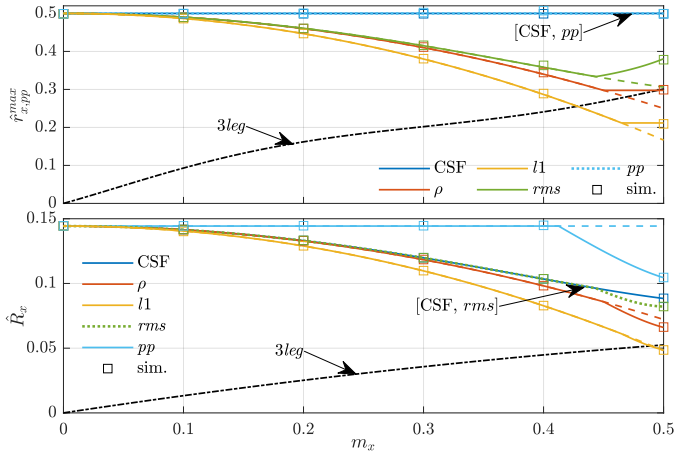

Fig. 13. Normalized maximum peak-to-peak of current ripple (top) and its rms (bottom) as a function of modulation index in case of CSF-PWM ('CSF') and VSF-PWM in case of maximum peak-to-peak ('*pp*'), average switching frequency ('ρ'), rms ('*rms*'), and switching losses ('*l*1', PF = 1) equalizations.

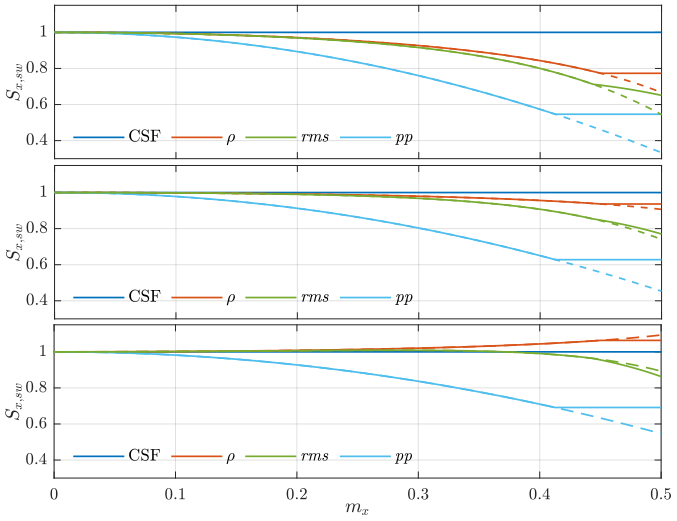

Fig. 14. Normalized switching losses as a function of modulation index in case of PF = 1 (top), PF = 0.8 (middle), and PF = 0.6 (bottom) for CSF-PWM ('CSF') and VSF-PWM during maximum peak-to-peak ('*pp*'), average switching frequency ('ρ'), and rms ('*rms*') equalization.

(bottom plot). The referring strategies are labeled with the same notation of Fig. 13. In all the cases, the identical peak-to-peak values of the current ripple ('*pp*') always ensure a relevant reduction in switching losses, thanks to the switching frequency span oriented towards low values of frequency (Fig. 6). In the best case (PF = 1), at $m = 0.5$, switching losses come to one third of the CSF-PWM one. As visible in the bottom plot of Fig. 14, rms of current ripple or average switching frequency equalizations may lead to higher losses for particularly low power factor values.

From this discussion, it stands out that it is possible to strongly reduce switching losses (therefore improving converter efficiency) by selecting the proper value of k in such a way that the current ripple maximum peak-to-peak or rms do not exceed what you would experience in case of CSFPWM. This means that, although the average switching frequency has been reduced, there is no need to increase the size, volume, and weight of the coupling inductors for achieving the same value of THD/TDD. On the other hand, one can try to achieve a higher level of integration (for instance, on-board chargers OBCs), taking advantage of a higher average switching frequency without higher switching losses (compared with CSFPWM) and the, therefore, bulkier heatsink.

Formulations related to VSF-PWM current ripple RMS, maximum current ripple peak-to-peak, and switching losses presented in the paper will not present the same grade of accuracy if employed in the case of magnetics saturation (although VSF-PWM definition (11) can be still used). A dedicated study, outside the scope of this paper, utilizing a virtual inductor could be carried out. However, it is reasonable to expect that VSF-PWM can guarantee similar improvements in harmonic pollution and converter efficiency with respect to CSF-PWM also in case of inductor saturation.

A. VSF-PWM Effects on the Inverter Efficiency

As argued in the previous Section and displayed in Fig. 14, switching losses optimization is perhaps one of the most interesting outcomes of the proposed VSF-PWM technique. In this regard, the efficiency plot of Fig. 15 depicts the switching loss reduction weight over the total power losses experienced by the converter. Fig. 15 represents a grid-connected application ($m = 0.4$; PF = 1, 0.8, and 0.6) in case of CSF-PWM and VSF-PWM under maximum peak-to-peak equalization. As visible, the switching losses reduction of about 43%, 35%, and 30% in the case of power factor 1, 0.8, and 0.6, respectively, depicted in Fig. 14 (*pp*) leads to a maximum efficiency η_{max} improvement of about 0.5% for all the cases (reduction of the global losses ranging from 20% to 30%). Similar improvement can be noticed in the European η_{EU} and Californian η_{CAL} efficiencies [34].

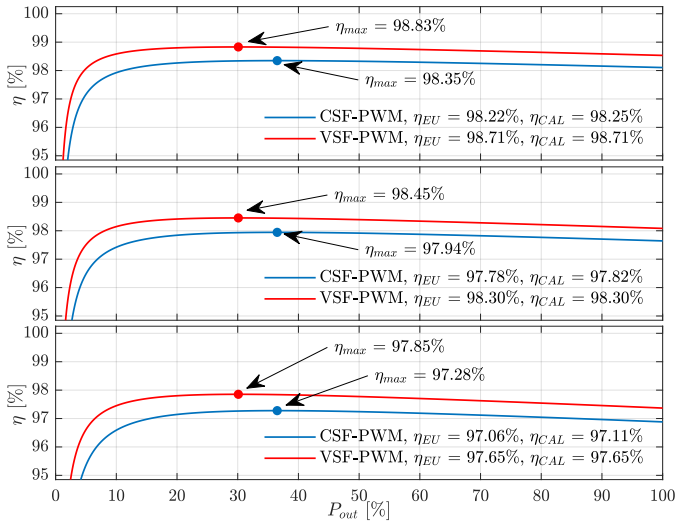

Fig. 15. Inverter efficiency in case of PF = 1 (top), PF = 0.8 (middle), and PF = 0.6 (bottom) for CSF-PWM and VSF-PWM (maximum peak-to-peak), at $m_a = m_b = m_c = 0.4$.

TABLE I
COMPARISON AMONG CSF-PWM, PROPOSED VSF-PWM, AND BASIC VSF-PWM OF [17].

η_{max}		PF = 1	PF = 0.8	PF = 0.6
CSF-PWM		98.35%	97.94%	97.28%
VSF-PWM	ρ	98.50%	98.00%	97.21%
	rms	98.55%	98.07%	97.31%
	pp	98.83%	98.45%	97.85%
	[17]	98.38%	97.98%	97.33%

As discussed above, classical DPWM techniques can not be implemented in the four-wire split-capacitor inverter. Therefore, the sole technique (remaining in the hard-switching domain) capable of reducing switching losses is VSF-PWM. However, to the best of the author's knowledge, no technique capable of independently tune each leg switching frequency is available yet. For this reason, the proposed VSF-PWM has been compared with [17] basic VSF-PWM implementation set having the same maximum current ripple peak-to-peak of CSF-PWM. In all the cases, the proposed VSF-PWM (especially '*pp*') ensures better performance than the basic VSF-PWM, which barely improves CSF-PWM efficiency. This is due to the missing degree of freedom that does not permit the strategy to be precisely tuned over each leg. Results depicted in Fig. 15 and Table I refers to the real power converter employed in the experimental validation of Section VI.

B. VSF-PWM effects on the neutral current ripple

Although driving each leg with independent switching frequency functions provides multiple benefits in terms of phase current quality and switching losses, it is particularly challenging to tackle the neutral current ripple study. For this reason, this Subsection presents qualitative considerations only.

It is reasonable to assume that the neutral current ripple is the algebraic summation of the phase current ripples. Since the current ripple continually ranges between positive and negative

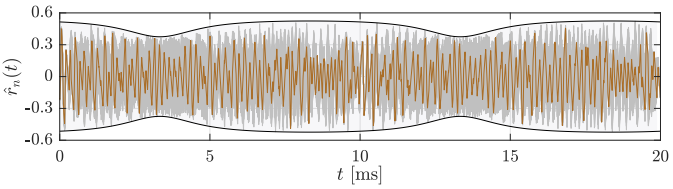

Fig. 16. Neutral current ripple in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ (front trace) and a set of neutral current ripples sharing the same boundary profile (background traces). Calculated boundary in case of VSF-PWM average switching frequency equalization.

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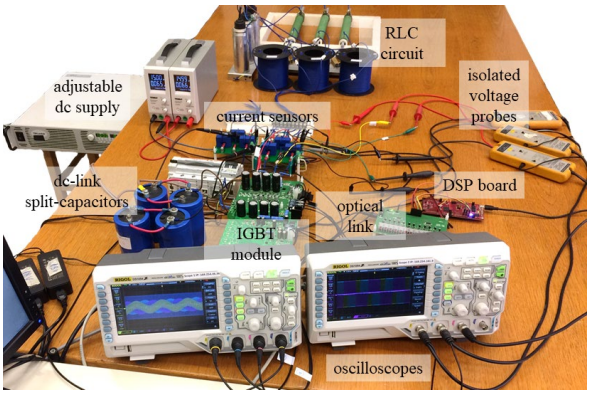

Fig. 17. View of the laboratory experimental working bench.

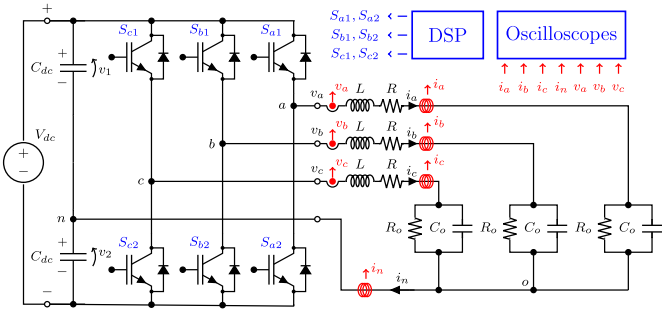

Fig. 18. Circuit scheme of the laboratory experimental working bench.

TABLE II
MAIN SYSTEM PARAMETERS.

Description	Labels	Parameters
dc voltage supply	V_{dc}	100 V
dc-link split capacitance (2×)	C_{dc}	2 mF
series *RL* circuit	R, L	727 mΩ, 1.73 mH
parallel *RC* circuit	R_o, C_o	6.6 Ω, 45 μF
fundamental frequency	f	50 Hz
switching frequency (CSF-PWM)	f_{sw}	5.1 kHz
minimum switching frequency limit	f_{lim}	1.6 kHz

values, cancellation effects may occur. A similar effect was obtained in [2] employing the carrier interleaving technique. However, since each leg is driven independently from the others, the neutral current ripple magnitude may be equal to the straight summation of the phase current ripple magnitudes. For this reason, thanks to (26), it is possible to define a boundary region in which the neutral current ripple can be enclosed.

$$\hat{r}_{n,pp}(t) \leq \hat{r}_{a,pp}(m_a,t) + \hat{r}_{b,pp}(m_b,t) + \hat{r}_{c,pp}(m_c,t) \quad (26)$$

Since a rigorous description of the neutral current ripple waveform is missing, the true-rms formulation cannot be derived easily. The neutral current ripple is reported in Fig. 16 (front trace) concerning the same case depicted in Fig. 10 (m_a = 0.3, m_b = 0.4, and m_c = 0.5). Moreover, multiple combinations of modulation indexes producing the same boundary profile are displayed in the background. As visible, traces remain confined within the region described by (26), representing the theoretical 'worst case'.

VI. EXPERIMENTAL RESULTS

In this Section, the analytical developments of Sections III and IV have been verified through experimental assessments on the test bench depicted in Fig. 17. The converter circuit from Fig. 1 has been coupled to a Y-connected three-phase, unity power factor *RLC* load (with common neutral point), where impedances are made as a sequence of series *RL* circuit and parallel *RC* circuit. The setup scheme is illustrated in Fig. 18.

The setup consists of an adjustable dc supply (GEN100-33, TDK-Lambda), a three-phase insulated gate bipolar transistor (IGBT) power module (PS 22A76, Mitsubishi Electric), and two dc-link split capacitors in between. The three RL circuits are created by utilizing air-core inductors. Measures of phase

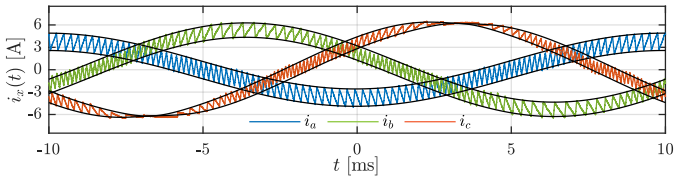

Fig. 19. Experimental phase currents of the three phases in case of m_a = 0.3, m_b = 0.4, and m_c = 0.5 with calculated envelopes in case of VSF-PWM average switching frequency equalization.

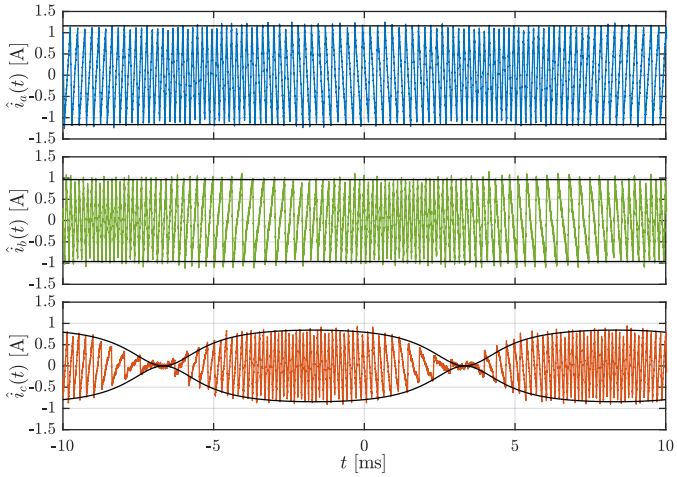

Fig. 20. Current ripples of the three phases in case of m_a = 0.3, m_b = 0.4, and m_c = 0.5 with calculated envelopes in case of VSF-PWM average switching frequency equalization.

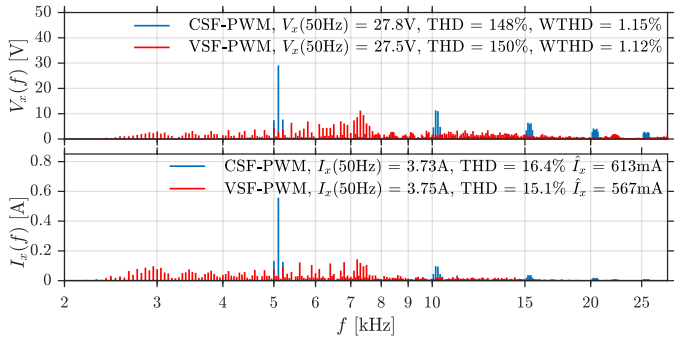

Fig. 21. Harmonic spectra of phase voltage (top) and current (bottom) in case of CSF-PWM and VSF-PWM (same average switching frequency), m_x = 0.4.

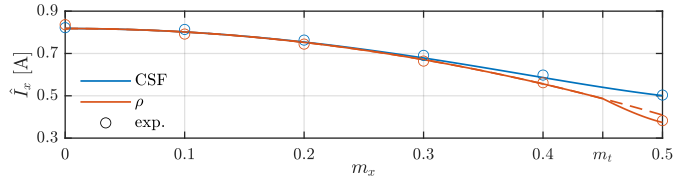

Fig. 22. Current ripple rms as a function of the modulation index in case of VSF-PWM average switching frequency equalization.

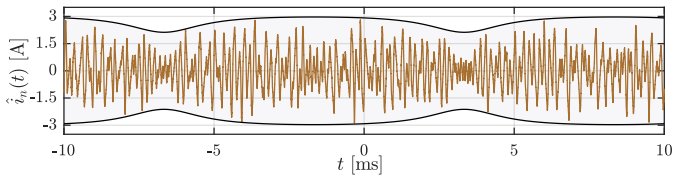

Fig. 23. Neutral current ripple in case of $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$ with the calculated boundaries and span (filled area) for VSF-PWM average switching frequency equalization.

currents are acquired by employing Hall-effect-based sensors (LA 55-P, LEM Europe) and sampled at 5 MS/s by digital oscilloscopes (DS1054Z, Rigol Technologies). The corresponded plots are created through MATLAB (MathWorks) using the acquired data points. The modulation is implemented by a digital signal processor (DSP) board (TMS-320F28379D, Texas Instruments). Setup parameters are listed in Table II.

Fig. 19 and Fig. 20 display measured phase currents and phase current ripple, respectively, in VSF-PWM average switching frequency equalization at $m_a = 0.3$, $m_b = 0.4$, and $m_c = 0.5$. In this way, results are comparable with the already discussed numerical results of Fig. 10 and Fig. 11. Moreover, three different power levels/fundamental currents insisting on the passive load are shown. As expected, the three different analytical envelopes match the actual current profiles validating the theoretical developments.

Although the voltage spectra of Fig. 21 present a slightly worse THD in VSF-PWM (due to non-idealities in the experimental setup), the harmonic distribution action ensures a current ripple rms and THD reduction anyway. As Fig. 22 shows, current ripple rms reasonably match the analytical profile of (15) and (25) throughout the modulation index m_x range. Finally, Fig. 23 verifies the neutral current ripple remains confined within the boundary described by (26).

VII. Conclusion

A novel variable switching frequency PWM strategy for a three-phase, four-wire, split-capacitor inverter has been proposed in this paper. Based on the current ripple prediction over each phase, the ripple is forced to have a flat profile, realizing several benefits discussed in detail. This target is achieved by employing switching frequency profiles fully tunable on each leg independently. In this way, it is possible to tweak metrics such as average switching frequency, maximum peak-to-peak value of current ripple, rms of current ripple, and associated switching losses in accordance with specific predetermined working boundaries.

It has been seen that a reduction of the maximum peak-to-peak current ripple, ranging from 33% to 67%, can be achieved at the maximum value of the modulation index. Similarly, the rms of the current ripple is lowered as well. Switching losses can be reduced (for unity power factor operation) to a diapason from 33% to 66% of the one obtained by CSF-PWM. Thanks to these effects on the main converter parameters, design optimization can be achieved. It is possible to find an appropriate trade-off among inverter cost, weight, volume, and efficiency by acting on the switching frequency profile, inductors, power switches technologies, and ac filter design.

On the other hand, formulations proposed here can be reversed to obtain the specific set of VSF-PWM parameters that guarantee the desired average switching frequency, switching losses, peak-to-peak magnitude of current ripple, or its rms as a function of modulation index and power factor.

All claims have been numerically and experimentally verified. The strong agreement between the analytical formulations and the verifications ensures the validity of the proposal. Future works might investigate alternative variable switching frequency paradigms tunings the driving strategy to optimize certain parameters. A statistical evaluation of maximum peak-to-peak and rms values of neutral current ripple could enrich the qualitative considerations proposed here.

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