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SiC-MOSFET and Si-IGBT-Based dc-dc Interleaved Converters for EV Chargers: Approach for Efficiency Comparison with Minimum Switching Losses Based on Complete Parasitic Modeling

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Abstract: Widespread dissemination of electric mobility is highly dependent on the power converters, storage systems and renewable energy sources. The efficiency and reliability, combined with the emerging and innovative technologies, are crucial when speaking of power converters. In this paper the interleaved dc–dc topology has been considered for EV charging, due to its improved reliability. The efficiency comparison of the SiC-MOSFET and Si-IGBT-based converters has been done on wide range of switching frequency and output inductances. The interleaved converters were considered with the optimal switching parameters resulting from the analysis done on a detailed parasitic circuit model, ensuring minimum losses and maintaining the safe operating area. The analysis included the comparison of different inductors, and for the selected ones the complete system efficiency and cost were conducted. The results indicate the benefits when SiC-MOSFETs are applied to the interleaved dc–dc topology for wide ranges of output inductances and switching frequencies, and most importantly, they offer lower total volume but also total cost. The realistic and dynamic models of power devices obtained from the manufacturer's experimental tests have been considered in both LTspice and PLECS simulation tools.

Keywords: electric vehicle (EV); fast charging; interleaved dc–dc converter, SiC devices; Si devices

1. Introduction

Environmental concerns and green energy goals have led to the growing interest in electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) technologies, since they offer reduced greenhouse emissions [1]. Governments worldwide are encouraging electric transportation with public policies and new standards. However, the critical points in the large changeover from combustion engine to EVs are still the batteries, suitable chargers and charging infrastructure [2].

In general, the batteries can be charged by on-board chargers (slow chargers) and off-board ones (fast chargers), both unidirectionally or bidirectionally. In either case, both the topologies and power ratings of the converters differ greatly [3]. EV battery chargers include both a dc–dc stage (typically buck/boost or switch-mode converters) and an ac–dc stage (controlled or uncontrolled rectifiers). The ac–dc stage should ensure high power quality operation, while the dc–dc stage should ensure high controllability and operability with constant current and voltage on battery

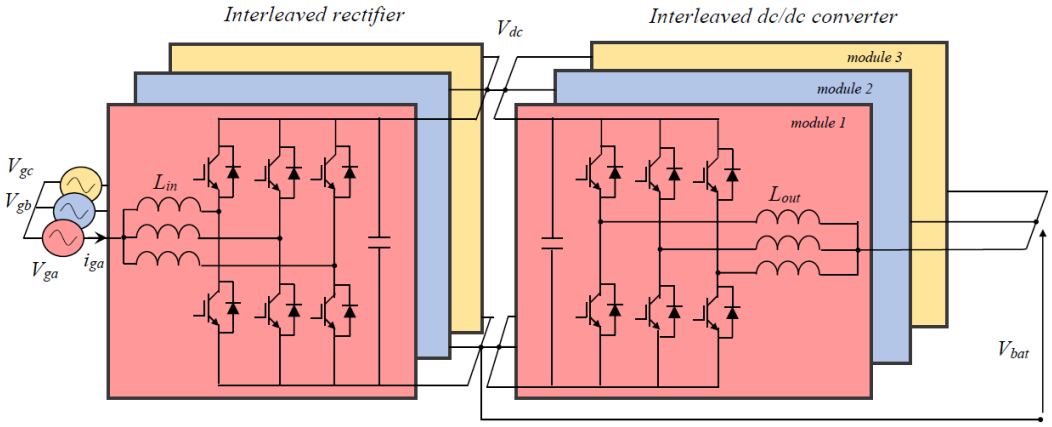
side [4]. The on-board chargers can be conductive (with direct contact) or inductive (transfer power magnetically) [5]. These chargers are nowadays widely employed, but are constrained by weight, space and cost. Nonetheless, all battery chargers have to be of high efficiency and reliability, and high power density. Their operation depends on components, sizing, control and switching strategies.

Fast charging refers to the off-board charging stations with at least 50 kW rated power [6]. Off-board chargers are less subjects of restrictions when compared to on-board chargers and feature high charging rates [7]. Various solutions for both ac–dc and dc–dc stages have been proposed and proven promising [8–12]. The concept which can be viably adopted is interleaved (also multiphase) converters, leading to higher efficiency, with possibilities of current ripple cancellation, and reduction in EMI and output filter size. [8,11,12]. Using interleaving, the power stage of a converter is symmetrically distributed into several smaller power stages. Consequently, the sizes of the passive components are reduced which allows a reduction in the overall cost of the system. Moreover, the system reliability can also be improved, due to the modularity that interleaved converters possess. Many interleaved topologies have been studied, both in ac–dc and dc–dc converter applications [13–15], and for EV charging [11,12,16,17]. When it comes to dc–dc converter applications, in [15] the multiphase interleaved converter for high current applications has been presented, operating in a wide load range. It has been proven that the phase-shift interleaving operation brings the decrease in the current ripple in the multiphase inverter stage. A three-phase interleaved dc–dc converter for EV fast charging with an effective control strategy has been proposed in [11,12], providing ripple-free output current in a wide output voltage range. In [16] the interleaving concept has been used to keep the input current ripple to a very low level in current-fed converter, and can viably be used in PHEV applications.

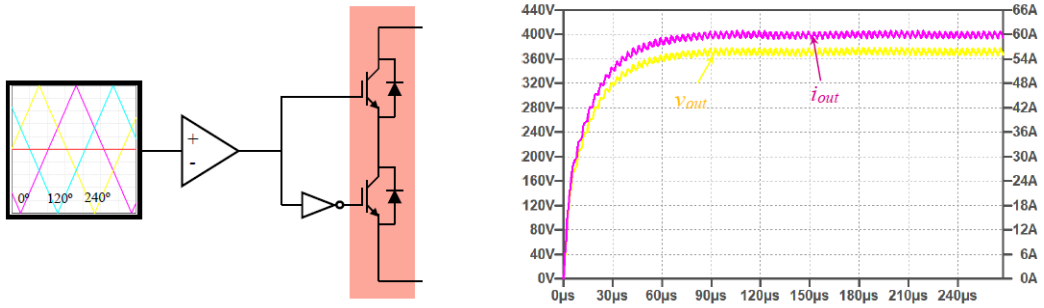
Recently, the wide bandgap semiconductor devices, such as silicon carbide (SiC), have become increasingly popular due to many benefits they offer compared to their silicon (Si) counterparts: lower switching losses and consequently high-switching capabilities, low on resistance and increased junction temperature [18]. With this in mind, and considering the benefits that an interleaved dc–dc converter offers, it is crucial to conduct the fair comparison of this specific topology with SiC metal-oxide-semiconductor field-effect transistor (SiC-MOSFET) and Si insulated-gate bipolar transistor (Si-IGBT) devices. Even though there have been many comparisons conduced in the literature for other topologies [19–21], for this particular topology not many studies are available. This kind of analysis on interleaved converter was firstly introduced in [22], where the efficiencies of SiC-MOSFET and Si-IGBT-based interleaved converters were compared, but considering only one value of the output inductance and switching frequency. This paper extends this analysis and considers the efficiency comparison on a wide range of output inductances and switching frequencies for both SiC-MOSFET and Si-IGBT-based converters. The interleaved topology was considered for the dc–dc power stage, having the possibility of the voltage and current ripple reduction in the battery-side and making it relevant for EV chargers. The comparison with different devices (SiC-MOSFET and Si-IGBT) is crucial in order to ease the decision process of power converter designers, and choose the right topology for the specific application. Moreover, the analysis includes the comparison of the total system losses and costs, including both converters and various output inductors. The goal was to have the maximum efficiency and minimum losses for both converters, maintaining the safe operating area of each device. Consequently, the most optimal switching condition has been derived from the complete parasitic model, based on experimental measurements. Namely, the minimum values of the external gate resistances have been determined by implementing the parasitic model in LTpice (Version XVII, Analog Devices, Norwood, MA, USA) simulation tool. Next, these resistances were used with double pulse testing in LTspice simulation tool on realistic and dynamic spice models of the respective power switches [23], from which the respective conduction and switching losses have been obtained for each device. These losses were finally implemented in complete 3-leg converter simulation in PLECS (Version 4.2.6, Plexim, Zurich, CH) , from which the loss comparison was conducted, with access to the steady state being facilitated.

2. Dc–dc Interleaved Converter

In Figure 1a is given the fast charger topology for electric vehicles. It consists of a three-phase ac–dc converter connected to an interleaved dc–dc converter with three legs having a three-phase structure. This structure was firstly introduced in [11,12]. The interleaved dc–dc converter is made by basic elements which are paralleled. It can be seen as a well-known two-level, three-phase configuration with the output inductor L_{out} and input dc-link capacitor C_{dc}. By having a rather simple structure, this converter features high reliability. The scalability is ensured as well, due to its modular structure.



(**a**)



(**b**)

Figure 1. Fast charger topology for EVs: (**a**) three-phase ac–dc converter and an interleaved dc–dc converter, and (**b**) control signals and typical output waveforms.

The ac–dc converter is connected to the grid and has the task of regulating the dc-link voltage. The interleaved dc–dc converter is able to provide the desired output current by controlling the output voltage. The converter's output current is equally shared among the legs. It is possible to achieve the output current ripple minimization with the control strategy [11]. Namely, with the carrier phase-shift of 360° divided by the number of legs and proper control, it is possible to achieve the minimum of the output current ripple, as shown in Figure 1b in the case of 3-leg converter. In Figure 1b the typical output waveforms of the interleaved converter are also shown.

3. Parasitic Model and Safe Operating Area

The interleaved converter permits the use of standard and reliable three-phase power switch modules. The sizes of the ac–dc stage and dc–dc stage are similar, which can be tracked back to sizing only a two-switch leg, which makes the design process rather simple. The simple two-switch leg can be scaled up by adding more legs. In this way the cost and the complexity of the system can be reduced.

In order to have the maximum efficiency in terms of fastest switching and minimum switching losses of the two converters (one with Si-IGBT and other with SiC-MOSFET devices), it is important

to carefully select the external gate resistance R_{g_ext}, since it can greatly influence the switching losses. The analysis in this regard started from the realistic and complete parasitic model of the three-leg converter, relying on the design practice and experimental measurements done on a existing printed circuit board (PCB) with connection cables for one converter leg. In Figure 2 is presented the three-leg model of the interleaved converter, taking into account the dc power supply V_{dc} with the cable connection for the PCB (in blue); the dc-link capacitors C_{dclink} (details on the dc-link ralization and capacitor parasitics in yellow) with the parasitic inductance of the capacitor bank PCB trace; the parasitic inductances of the PCB traces connecting the different legs and switches; and the impedance of the cable connecting the output inductor L_{out}. In Table 1 are given the values that have been obtained on the basis of the experimental measurements for the dc power supply and load connection cable, and calculated for the PCB traces with the standard trace thickness 105 µm and width of 0.93 cm required for the considered currents [24]:

$$\frac{L}{l} = 2\left(ln\left(\frac{2l}{w+t}\right) + \frac{1}{2}\right) \text{(nH/cm)} \quad (1)$$

where L is the trace inductance, l is the trace length, w is the width and t is the thickness of the PCB trace. The considered values of PCB traces were carefully selected and are based on the real power electronic circuit design.

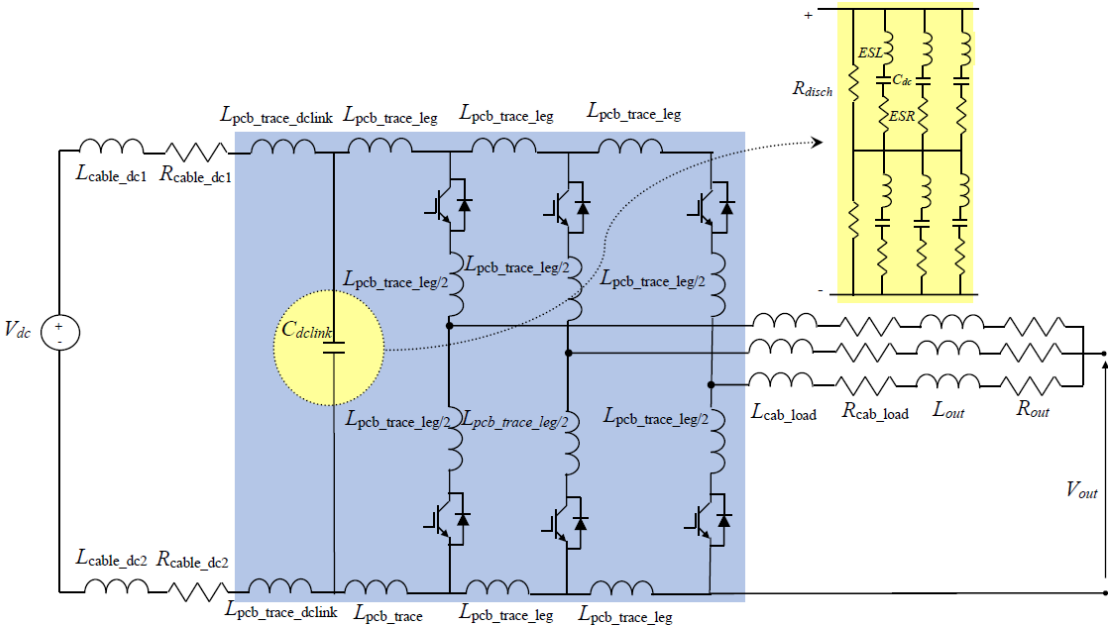


Figure 2. Dc–dc interleaved converter: full parasitic model of 3 legs.

Table 1. PCB parameters.

Parameter (Unit)	Value
L_{cable_dc1} (µH)	1.77
R_{cable_dc1} (mΩ)	8.92
L_{cable_dc2} (µH)	1.74
R_{cable_dc2} (mΩ)	8.79
$L_{pcb\_trace\_dclink}$ (nH)	36.5
$L_{pcb\_trace\_leg}$ (nH)	66.5
$L_{pcb\_trace\_leg/2}$ (nH)	33.25
L_{cab_load} (µH)	0.834
R_{cab_load} (mΩ)	4.21
Thin film capacitor C_{dc} (µH)	15
ESR (mΩ)	4.8
ESL (nH)	12.4
R_{disch} (kΩ)	100

The circuit has been implemented in LTspice simulation tool. The real models of the powers switches were used for this analysis, i.e., the 1200 V SiC device SCT3080KLHR Rohm [25] with the SiC Schottky anti-parallel diode SCS220KG Rohm [26] for the SiC-MOSFET-based converter, and 1200 V Si-IGBT device RGS50TSX2DHR Rohm [27] for the IGBT-based converter (model with fast recovery diode), having the main parameters listed in Table 2, giving quick access to the sizing of different devices. The complete model of three-leg converter has been considered, as shown in Figure 2. The analysis included a set of switching frequencies and output inductors, as listed in Table 3. The goal was to obtain the minimum external gate resistance value for each set of L_{out} and f_{sw}, in order to enable fastest switching with minimum losses, but staying within the safe operating area (SOA) of the device. What has also been considered is the internal resistance of the gate driver BM6105AFW-LBZ (Rohm) R_{int} of 1.5 Ω, which can be used for both SiC-MOSFET and Si-IGBT devices. With this in mind, the gate-source voltage of the SiC-MOSFET-based converter was $-4/18$ V ensuring the optimal turn on and turn off of the device, while for the Si-IGBT inverter the gate-emitter voltage 0/15 V has been used.

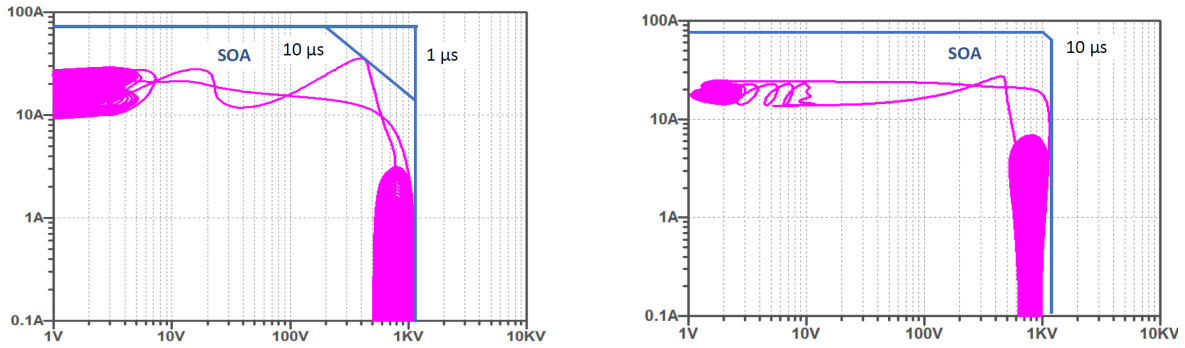
The resulting required minimum gate resistances to be added externally to the gate driver for SiC-MOSFET and Si-IGBT-based converters are shown in Table 3, together with the simulation parameters that are used for LTspice simulation such as the values of the $L_{out} - f_{sw}$ pairs. The minimum required values of the gate resistances have been determined in the LTspice simulation by increasing the value of the gate resistance (starting from 1.5 Ω), and taking the first value for which the SOA region is satisfied. The SiC-MOSFET-based converter requires no additional gate resistance (apart from the internal resistance of the gate driver), while the Si-IGBT-based converter requires 3.5 Ω for all the considered L_{out} and f_{sw}. Figure 3 shows the voltages and currents of one switching period (turn on and off) together with SOA region as indicated in the devices' datasheets. The Figure 3 resulted from the LTspice simulation considering the worst case with the highest one-leg current of 25 A, having for SiC-MOSFET-based inverter the L_{out} = 0.33 mH and f_{sw} = 100 kHz (Figure 3a), and for Si-IGBT-based converter L_{out} = 1.15 mH and f_{sw} = 30 kHz (Figure 3b).

Table 2. Main device parameters.

Parameters	Rohm SiC MOSFET SCT3080KLHR	SiC Schottky diode SCS220KG	Rohm Si IGBT RGS50TSX2DHR
V_{ds}	1200 V	1200 V	1200 V
I_{ds} (25 °C)	31 A	-	50 A
I_{ds} (100 °C)	22 A	20 A/133 °C	25 A
$R_{DS(on)}$ (25 °C)	80 mΩ	N/A	N/A
V_{CE-sat} (25 °C)	N/A	N/A	1.7 V
Q_g	60nC@18 V	N/A	67nC@15 V
V_{th}	2.7 V	N/A	6 V
V_{gs}	−4 to +22 V	N/A	±30 V
T_j	175 °C	175 °C	175 °C
P_{diss} (25 °C)	165 W	210 W	395 W
r_{jc}	0.7 °C/W	0.62 °C/W	0.38 °C/W

Table 3. Main simulation parameters.

SiC-MOSFET-Based Converter			Si-IGBT-Based Converter		
Inductance (mH)	Switching Frequency (kHz)	R_{g_ext} (Ω)	Inductance (mH)	Switching Frequency (kHz)	R_{g_ext} (Ω)
0.56	60	0	3.46	10	3.5
0.51	70	0	2.3	15	3.5
0.45	80	0	1.73	20	3.5
0.4	90	0	1.38	25	3.5
0.33	100	0	1.15	30	3.5



(**a**) (**b**)

Figure 3. Safe operating area: (**a**) SiC-MOSFET-based converter and (**b**) Si-IGBT-based converter.

As can be seen from the figure, the safe operating area is ensured for both cases. The same goes for the rest of the L_{out} and f_{sw} values.

4. Power Loss Analysis

The losses in the specific device are mainly the sums of two losses: the conduction and switching losses. The conduction losses of the IGBT can be calculated with the use of its dynamic on resistance $R_{on,IGBT}$ and zero on-state voltage V_{on}:

$$P_{con,IGBT} = V_{on} I_{av} + R_{on,IGBT} {I_{rms}}^2 \tag{2}$$

where I_{av} and I_{rms} are the average and rms currents through the device.

On the other hand, the conduction losses of SiC-MOSFET can be evaluated by using its on-resistance $R_{DS(on)}$:

$$P_{con,MOSFET} = R_{DS(on)} {I_{rms}}^2 \tag{3}$$

The conduction loss for the diode is based on its threshold voltage V_T and dynamic on resistance $R_{on,diode}$:

$$P_{con,diode} = V_T I_{av} + R_{on,diode} {I_{rms}}^2 \tag{4}$$

The switching losses in the device depend on the switching frequency and the dissipated energies during turning on and turning off:

$$P_{sw,device} = f_{sw}(E_{on,device} + E_{off,device}) \tag{5}$$

where $E_{on,device}$ and $E_{off,device}$ are the device's dissipated energy during turning on and turning off.

4.1. Losses in the Interleaved dc–dc Converter

In the interleaved dc–dc converter, the conduction and switching losses can be analyzed by considering only one converter leg, since all the legs share the same losses. The output current has a DC value I_0 and a ripple component Δi_0. In the upper switch is circulating the current with the rms value [28]:

$$I_{rms,upper} = \sqrt{D I_0^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_0}{I_0}\right)^2\right]} \tag{6}$$

where D is the duty cycle.

Similarly, the rms current of the bottom switch can be written as:

$$I_{rms,lower} = \sqrt{(1-D)I_0^2\left[1+\frac{1}{12}\left(\frac{\Delta i_0}{I_0}\right)^2\right]} \tag{7}$$

Basing on the Equations (6) and (7) for the conduction losses of SiC-MOSFET, Si-IGBT and the diodes we can write:

$$P_{cond,IGBT} = V_{on}D'I_0 + R_{on,IGBT}DI_0^2\left[1+\frac{1}{12}\left(\frac{\Delta i_0}{I_0}\right)^2\right] \tag{8}$$

where $D' = (1 - D)$.

$$P_{cond,MOSFET} = R_{DS(on)}DI_0^2\left[1+\frac{1}{12}\left(\frac{\Delta i_0}{I_0}\right)^2\right] \tag{9}$$

$$P_{cond,diode} = V_TD'I_0 + R_{on,diode}D'I_0^2\left[1+\frac{1}{12}\left(\frac{\Delta i_0}{I_0}\right)^2\right] \tag{10}$$

The switching losses can be evaluated as:

$$P_{sw,device} = f_{sw}E_{sw,device}\left(\frac{I_{avg}}{I_{ref}}\right)^{K_I}\left(\frac{V_{sup}}{V_{ref}}\right)^{K_V} \tag{11}$$

where I_{avg} is the average output current; V_{sup} is the device supply voltage (collector-emitter for IGBT, or drain-source for SiC-MOSFET); I_{ref} and V_{ref} are the respective current and voltage available in the datasheet, obtained from the switching loss measurement; K_I and K_V are the coefficients usually defined as in [29].

4.2. Inductor Losses

The losses in the inductor are the sums of winding losses and core losses. When it comes to winding losses, the DC resistance is associated with the dissipated power of the windings, but also phenomena such as skin effect and proximity effect. The latter two are associated with AC current components, and since the ripple of the current is minimized, can be neglected. The winding losses can be determined using [30]:

$$P_{L,w} = R_{dc}{I_{rms}}^2 \tag{12}$$

where I_{rms} is the rms current through the inductor.

The DC resistance can be calculated basing on the wire properties:

$$R_{DC} = \frac{\rho N mlt}{A_{winding}} \tag{13}$$

ρ being the specific copper resistivity, N the number of turns, mlt the mean length per turn available in the datasheet and $A_{winding}$ the winding's cross-sectional area.

The core losses can be approximated by the Steinmetz equation:

$$P_{L,core} = Kf^{\alpha}B_{pk}^{\beta} \tag{14}$$

where f is the frequency; B_{pk} is the peak flux density when applied for sinusoidal excitation; α and β are constants depending on the core material, magnetic induction and switching frequency operating range. Another way to estimate the core losse is by the use of core loss curves in the case of specific flux density (e.g., available in [31] for different core sizes and shapes).

The peak flux density can be calculated as [32]:

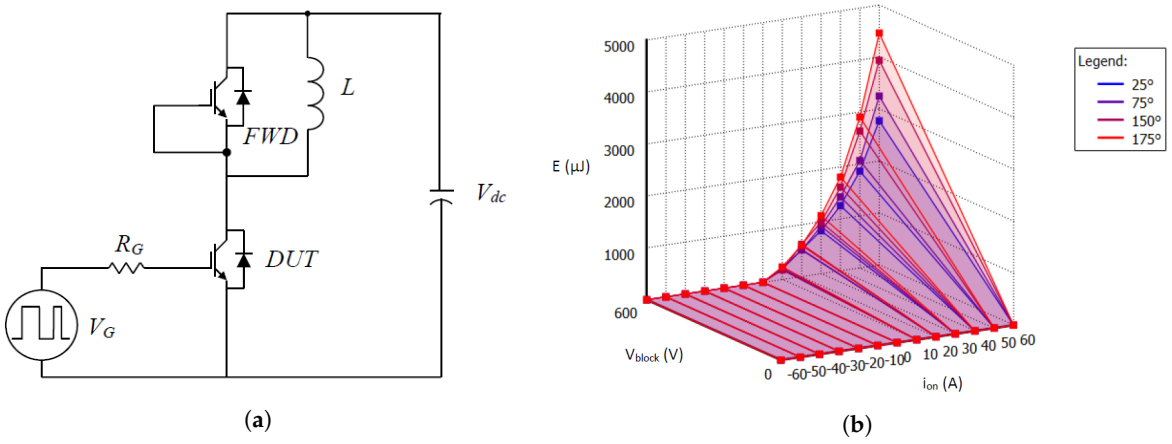
$$B_{pk} = \frac{E_{rms}10^8}{4.44A_eNf_{sw}} \quad (15)$$

where E_{rms} is the rms voltage across inductor (in V); A_e is the cross sectional area (in cm^2); and f_{sw} is the switching frequency (in Hz), while B_{pk} is expressed in gauss. The factor of 10^8 is due to the B_{pk} conversion from Tesla to gauss (1 Tesla = 10^4 gauss). Knowing B_{pk}, the core loss curves available in the core's datasheet can be utilized.

4.3. Double Pulse Test and PLECS Analysis

The simulation package PLECS offers the possibility to the user to merge the thermal and electrical design and provides the cooling solutions. The switching and conduction losses of the specific device are inserted by the user for each operating condition (forward current, blocking voltage, junction temperature) in terms of 3D look-up tables. In this way the simulation speed is not necessarily affected and the long thermal transient can be skipped by the steady-state analysis. The Cauer and Foster thermal networks can be utilized for the thermal description of the device.

The standard double pulse tests (DPT) have been conducted on the spice switch models presenting its realistic and dynamic behavior, as provided from the manufacturer's experimental tests. DPTs were done for each device listed in Table 2 in LTspice (Figure 4a with IGBT devices), in order to obtain the necessary switching and conduction losses of the device, used lateron in PLECS analysis. One example of the turn on losses obtained from LTspice DPT on a realistic switch model and implemented in PLECS is given in Figure 4b in the case of the 1200 V IGBT. In the same way, the losses for the SiC-MOSFET can also be determined and utilized.



(**a**) (**b**)

Figure 4. Double pulse test: (**a**) schematic of the double pulse test and (**b**) an example of IGBT's switching on losses for different temperatures.

After the loss descriptions had been added in PLECS and thermal network has been created, it was possible to select the appropriate heat sink. With the use of steady-state analysis tool, the respective converter losses together with the device junction, case temperatures and the heat sink temperature can be measured.

5. Results

Both LTspice and PLECS were used for the simulation analysis, as explained in Section 4.3. The device characterization in terms of conduction and switching losses has been done by double pulse tests on real device models in LTspice. In the next step, these losses connected to the different operating conditions were inserted in the look-up tables in PLECS and in this way it was possible to characterize each device for each switching period. The three-leg interleaved dc–dc converter

(as shown in Figure 1) was implemented in PLECS. For the efficiency analysis the simpler converter model was considered, i.e., without the parasitics, as usually they can be neglected and are the same for the two converters. As resulted from the parasitics analysis, the external gate resistance of 0 Ω was used for double pulse test in the case of SiC-MOSFET device, considering only the internal resistance of the gate driver, i.e., 1.5 Ω. Instead, for the Si-IGBT device the external gate resistance of 3.5 Ω was used. The other simulation parameters are listed in Table 4. The L_{out}–f_{sw} pairs for each converter have been defined in Table 3 and were used here for simulations of different cases. The specific L_{out}–f_{sw} pairs were selected in order to keep the output current ripple within 5%. Cases with different output currents of 30, 45, 60 and 75 A were analyzed, corresponding to the 25%, 50%, 75% and 100% of the output power. The control reference was compared with three shifted carriers in order to obtain the pulse-width modulation (as explained in Section 2), providing a fixed switching frequency.

Table 4. Simulation parameters.

SiC-MOSFET Based Converter		**Si-IGBT Based Converter**	
Parameter (unit)	Value	Parameter (unit)	Value
V_{DC} (V)	800	V_{DC} (V)	800
R_{g_ext} (Ω)	0	R_{g_ext} (Ω)	3.5
R_{g_int} (Ω)	1.5	R_{g_int} (Ω)	1.5
D (%)	50	D (%)	50

5.1. Inductor Selection

The comparison of different core types given in Table 5 has been shown in Figure 5, for the two core types found as the best compromise for the total inductor losses and inductor volume. Two different types have been considered for both converters, iron (in turquoise) and alloy (in pink) powder core from [31]. In Figure 5 is given the comparison of total core losses, costs (obtained from the core manufacturer) and volume for the case of 25 A inductor current corresponding to the 75 A output current. In the case of SiC-MOSFET the difference between the volume of iron and alloy inductors is not very marked, except in the case of the highest switching frequency (0.33 mH–100 kHz) where the alloy core allows one to have an inductor with volume reduced to half (171 cm^3–85.5 cm^3).

For Si-IGBT-based converter there was more significant difference in the volume of iron and alloy core except for the 3.46 mH–10 kHz pair, where it was not possible to design the alloy powder core. When considering the lowest (10 kHz) and highest (30 kHz) switching frequencies, the alloy allowed 57% reduction in core volume.

Table 5. Comparison of different core types.

L–f_{sw} Pairs	**Iron Core**	**Alloy Core**
SiC-MOSFET-based converter		
0.56 mH, 60 kHz	**T400-14D** *	OP-521014-2
0.51 mH, 70 kHz	**T400-14D**	OP-521014-2
0.45 mH, 80 kHz	**T400-14D**	OP-521014-2
0.4 mH, 90 kHz	**T400-14D**	OP-521014-2
0.33 mH, 100 kHz	T400-14D	**SM-400026-2**
Si-IGBT-based converter		
3.46 mH, 10 kHz	**T650-14**	-
2.3 mH, 15 kHz	T650-14	**FS-650014-2**
1.73 mH, 20 kHz	T650-14	**OD-650026-2**
1.38 mH, 25 kHz	T650-14	**OD-601026-2**
1.15 mH, 30 kHz	T650-14	**FS-601014-2**

* In bold are given the inductors that later on are selected for further analysis.

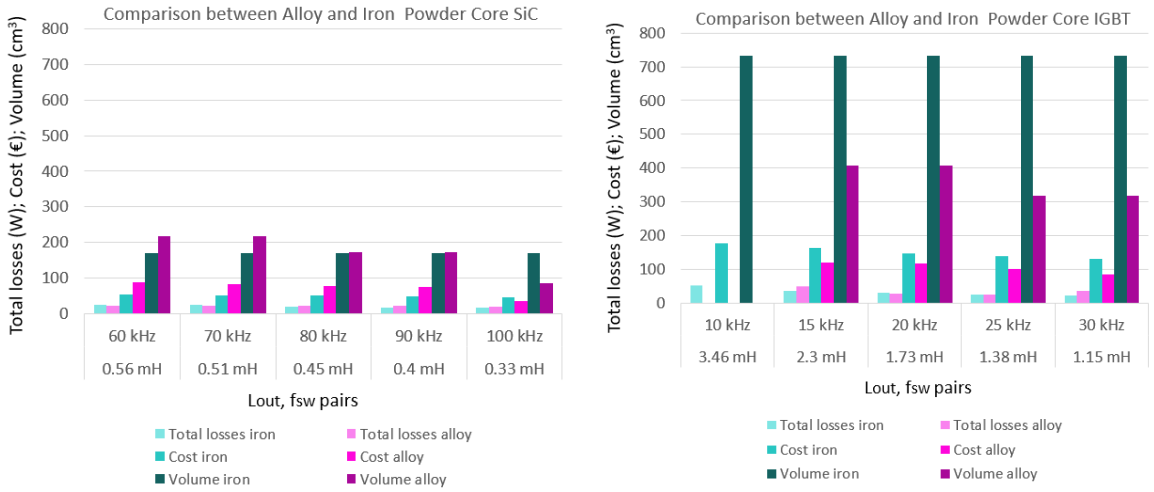


Figure 5. Comparison of cost, volume and total calculated losses for iron and alloy powder cores: (**a**) SiC-MOSFET-based converter; (**b**) Si-IGBT-based converter.

Evident also are the reductions in volume, losses and costs in both iron and alloy powder core when comparing Figure 5a,b for SiC-MOSFET-based converter, confirming the advantages of using the SiC-MOSFET devices. For the two highest switching frequencies (30 kHz for Si-IGBT and 100 kHz for SiC-MOSFET), the SiC-MOSFET-based converter can offer the reduction of 73% of the core volume for alloy core, and 77% for the iron core, having around 60% lower cost.

In this case, the best compromise in terms of total losses and volume has been taken into account. The selected inductors are given in bold in Table 5. In some cases the best choice is iron core, while in other cases it is alloy core. For the SiC-MOSFET-based converter the best solutions are almost always in iron, except for the case with the highest switching frequency (100 kHz), which also represents a significant working condition, allowing one to make the most of the advantages offered by SiC-MOSFET devices and significantly reduce weight and volume. On the other hand, for Si-IGBT the best solutions are always in alloy, except for the lowest switching frequency (10 kHz) with only possible solution in iron. However, this working condition is not very significant because it leads to higher volume and cost. Further on in the analysis, only the inductors given in bold were considered for the efficiency comparisons.

5.2. Power Loss and Efficiency Comparisons

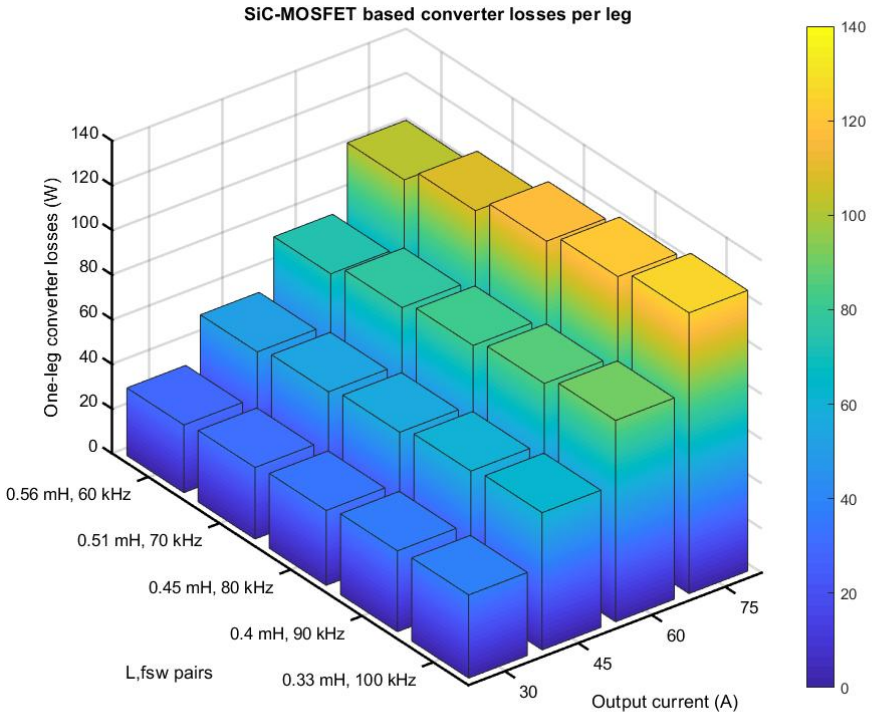
In this section the power loss and efficiency comparison is presented. The three-leg interleaved dc–dc converter supplying a resistive load and implemented in PLECS has been used for this purpose. For each specific value of L_{out} the inductance with its winding resistance (as resulted from the inductor design shown in Table 6) has been used for the modeling. The converter losses have been determined directly from the PLECS simulation tool, while the inductor losses (for each specific inductor designed) have been calculated as described in Section 4.2.

In Figure 6 are given the dc–dc converter losses in the case of different output inductor–switching frequency pairs and output currents in the case of 50 °C heat sink temperature. In particular, four values of the output current have been considered: 30, 45, 60 and 75 A. The two converters show rather similar losses, even though the SiC-MOSFET converter's switching frequency is much higher than the one of Si-IGBT converter (60–100 kHz vs. 10–30 kHz). For the highest output current of 75 A, the SiC-MOSFET-based converter has 28%, 18% or 9% higher losses when compared to Si-IGBT-based converter for the switching frequencies below 80 kHz (for Si-IGBT below 20 kHz) respectively, but lower 1% for the 90kHz and 9% for 100 kHz, as shown in Figure 7a . Generally, all the losses show the same behavior, lower in case of Si-IGBT for the switching frequencies <20 kHz. More flat behavior of the

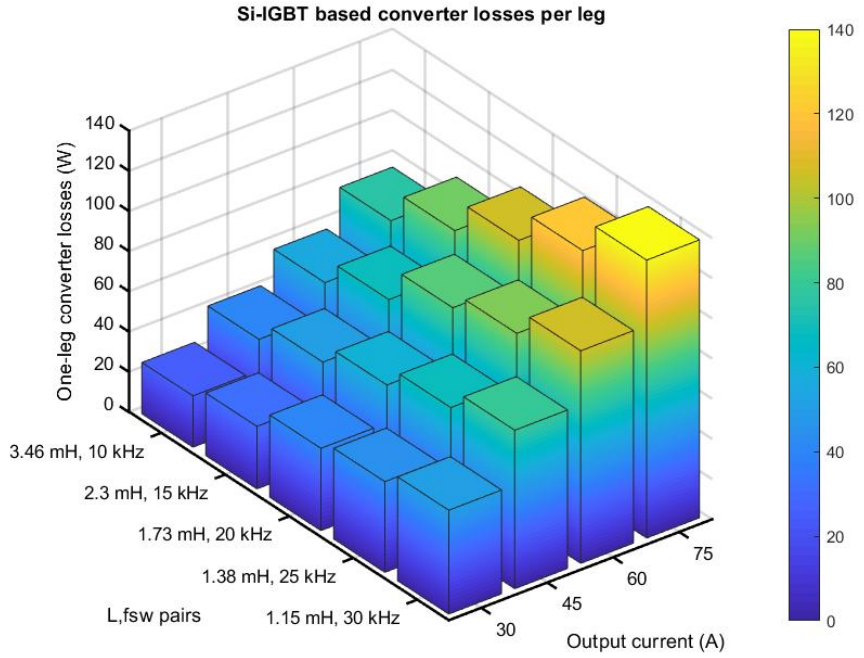
losses for SiC-MOSFET-based converter can be noted, i.e., less variations with the change of L_{out}–f_{sw} pairs for the specific current.

In Figure 8 are given the total inductor losses for the selected inductors from Section 5.1. In particular, they resulted from the sum of inductor core and winding losses in the case of different inductors and output currents, as for converter losses. Different inductors have been designed, as shown in Table 6. The criteria for the design were the lowest total inductor losses, but also the lowest volume. The standard design practice has been applied; for example, the difference of the unloaded and loaded unductor was set to 10%, the cross section of the winding was carefully selected taking into account the minimum banding radius of the wire, the filling of the core window area was set to less than 50%, etc.

From the Table 6 can be noted 3.7 times lower inductor volume when comparing the cases with highest switching frequencies in the case of SiC-MOSFET-based converter. In Figure 8 the maximum losses for SiC-MOSFET-based converter of 24.9 W can be seen for the 0.56 mH–60 kHz pair and 75 A output current, while for the Si-IGBT-based converter the maximum is for 3.46 mH–10 kHz pair reaching 52.6 W at 75 A output current. The minimum losses for SiC-MOSFET-based converter are for 0.4 mH–90 kHz with 6.9 W in the case of lowest output current, while for Si-IGBT-based converter the minimum losses of 10.7 W are for 1.38 mH–25 kHz pair and the same value of the output current. In Figure 7b are given the inductor losses for the highest output current, i.e., 75 A. The losses of SiC-MOSFET-based converter are lower for all L_{out}–f_{sw} pairs, with the highest difference of 53% at the lowest switching frequency. Conveniently, the total one-leg losses are also depicted in Figure 7c, obtained as the sum of device losses and inductor losses per leg at 75 A output current. It is interesting to see that the Si-IGBT-based converter has higher losses in almost all cases, except the 1.73 mH–20 kHz case, where SiC-MOSFET-based converter shows 4% higher losses.



(**a**) SiC-MOSFET-based converter



(**b**) Si-IGBT-based converter

Figure 6. Dc–dc converter losses per leg for different output inductors resulting from the simulation.

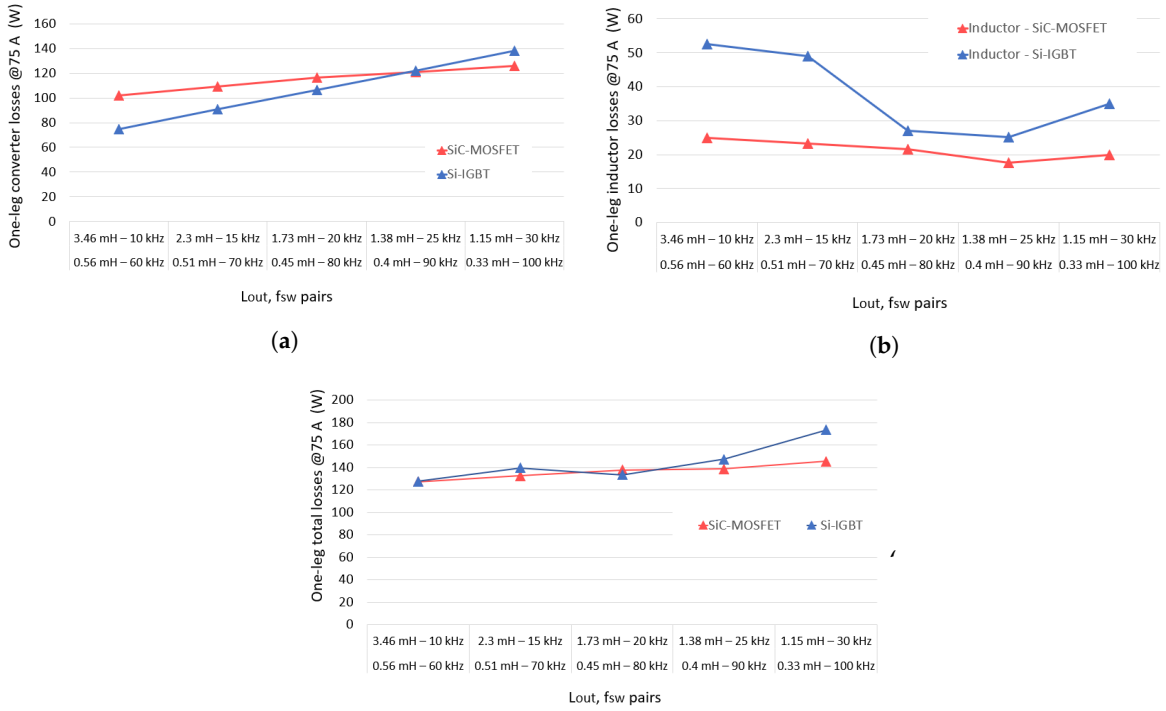
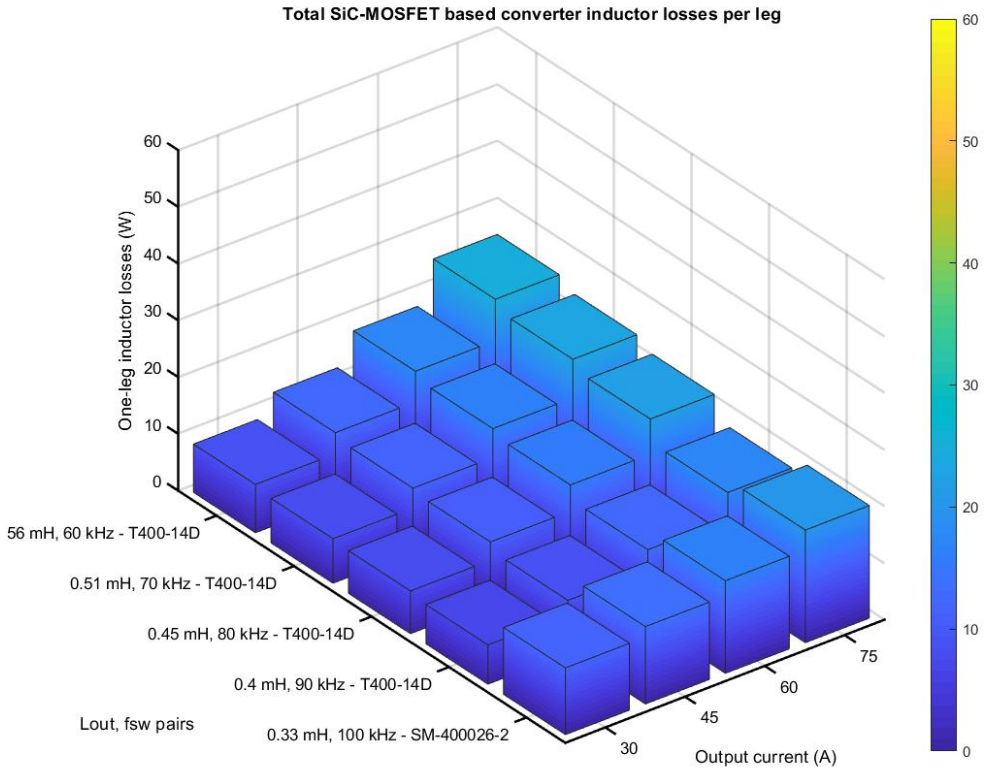


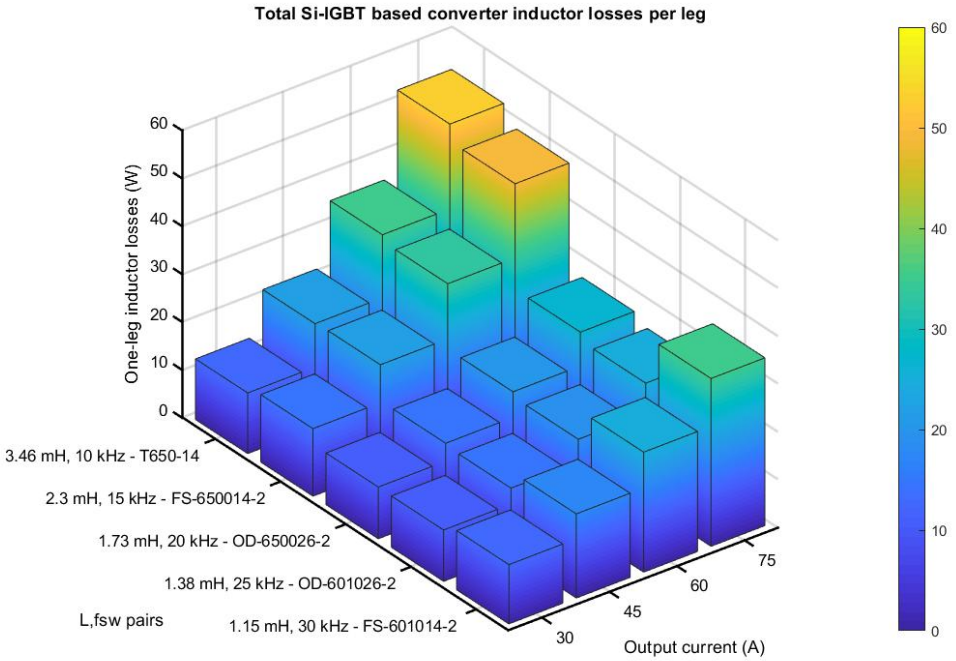
Figure 7. One-leg losses of SiC-MOSFET and Si-IGBT-based converters at 75 A output current: (**a**) simulated device losses, (**b**) analytical inductor losses, (**c**) total one-leg losses.

Table 6. Inductor design.

SiC-MOSFET Based Converter							
L_{out}, f_{sw} pairs	Core type	N	AWG	R_{dc} (Ω)	A_e (cm^2)	*mlt*	V_e (cm^3)
0.56 mH, 60 kHz	T400-14D	110	7	0.03082	6.85	14.62	171
0.51 mH, 70 kHz	T400-14D	105	7	0.02895	6.85	14.46	171
0.45 mH, 80 kHz	T400-14D	98	7	0.02649	6.85	14.24	171
0.4 mH, 90 kHz	T400-14D	92	6	0.02009	6.85	14.76	171
0.33 mH, 100 kHz	SM-400026-2	87	6	0.01522	3.5226	11.51	85.5
Si-IGBT Based Converter							
L_{out}, f_{sw} pairs	Core type	N	AWG	R_{dc} (Ω)	A_e (cm^2)	*mlt*	V_e (cm^3)
3.46 mH, 10 kHz	T650-14	212	6	0.07507	18.4	23.64	734
2.3 mH, 15 kHz	FS-650014-2	241	6	0.06565	9.87	18.09	407
1.73 mH, 20 kHz	OD-650026-2	155	5	0.03049	9.87	17.05	407
1.38 mH, 25 kHz	OD-601026-2	137	5	0.0273	8.8064	17.19	317
1.15 mH, 30 kHz	FS-601014-2	167	6	0.04266	8.8064	17.09	317



(**a**) SiC-MOSFET-based converter



(**b**) Si-IGBT-based converter

Figure 8. Total inductor analytical losses per leg.

For the particular case in Figure 7c, where SiC-MOSFET-based converter shows slightly higher losses, the loss distribution has been analyzed for all the values of the output current. In Figure 9 is shown the distribution of the total losses (simulated device and analytical inductor) of one converter leg, and specifically for the 0.45 mH–80 kHz pair (SiC-MOSFET-based converter) and the 1.73 mH–20 kHz pair (Si-IGBT-based converter) in the case of 50 °C heat sink temperature. The figure also gives the comparison with the theoretical values, calculated as explained in Sections 4.1 and 4.2.

The total losses of SiC-MOSFET-based converter (dark pink) are higher only in the case of 75 A output current, as resulted also in Figure 7c, while for the other current values it shows lower losses compared to Si-IGBT converter (dark green). As for the losses of the devices in one converter leg, the switching losses which are also shown in the figure are slightly lower for the SiC-MOSFET-based converter, even though the switching frequency was four times higher. The total inductor loss (dotted traces) is slightly lower for SiC-MOSFET-based converter, having core losses invariant with the change of the output current, as expected. For the specific case of 75 A output current, the SiC-MOSFET-based converter shows elevated conduction losses, and this is the reason why it resulted in higher total losses. Moreover, also the good agreement between simulation results (first bar) and analytical results (second bar) for all cases can be observed.

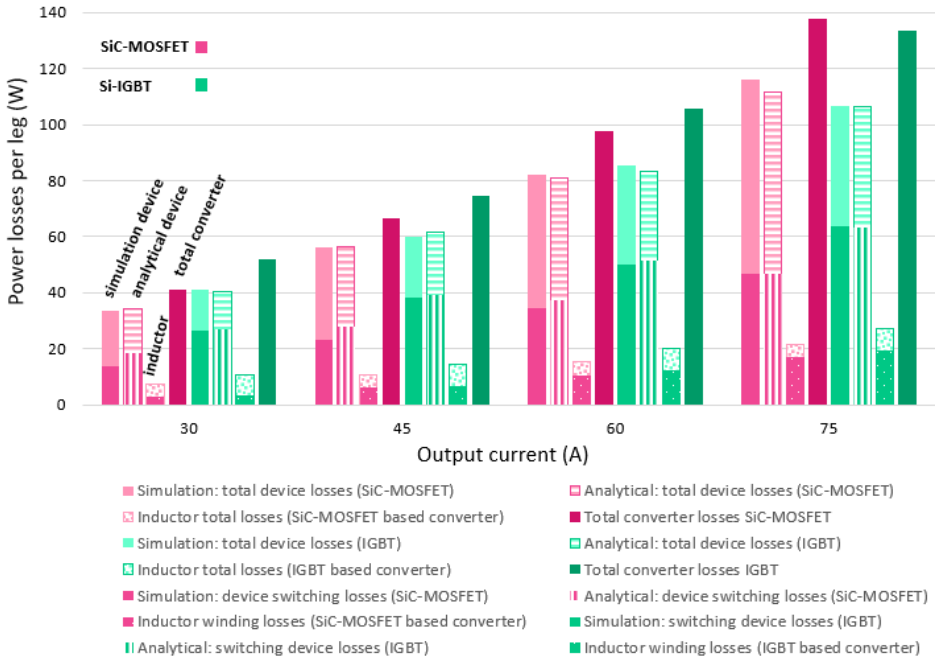


Figure 9. Loss distribution for 0.45 mH–80 kHz and 1.73 mH–20 kHz pairs and comparison with analytical values.

In Figure 10 are shown the total three-leg losses of the two converters, including the inductor losses resulting from realistic simulations (for power switches), and analytical for the different inductors. Generally, the SiC-MOSFET-based converter showed lower total losses (in pink), especially for the lower output currents. The highest losses can be noted for the Si-IGBT-based converter and 1.15 mH–30 kHz pair for all the values of the output current, due to high devices' losses. While the SiC-MOSFET-based converter has more uniform losses behavior with the change of switching frequency, this difference is more outlined in the Si-IGBT-based converter.

In Figure 11 are shown the efficiencies of the two three-leg converters for different L_{out}–f_{sw} pairs and output currents. For both converters, the efficiency is rather high, higher in the case of lower switching frequencies due to lower losses. The SiC-MOSFET-based converter shows higher efficiency (ranging between 98.3% and 98.9%), while in the case of Si-IGBT the efficiency ranges from 98% to 99%. The efficiency curves are closer to each other in the SiC-MOSFET when compared to Si-IGBT

case, meaning that in the SiC-MOSFET case there is a lower variability of efficiency with the change of L_{out}–f_{sw} pairs. In the worst case (30 A) there is a variability of about 0.3% in the case of SiC-MOSFET and 0.7% in the case of Si-IGBT. Therefore it can be concluded that by adopting the SiC-MOSFET solution, efficiency depends less on the choice of switching frequency and inductor.

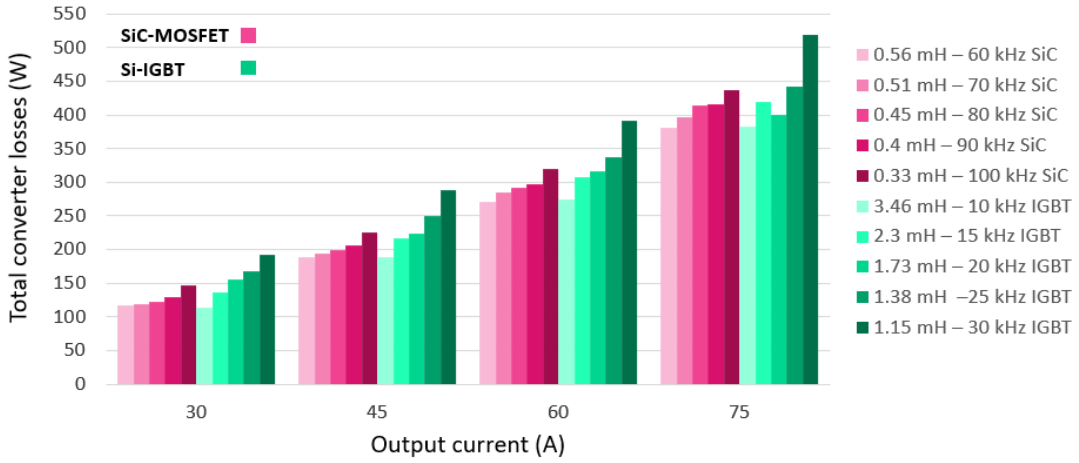
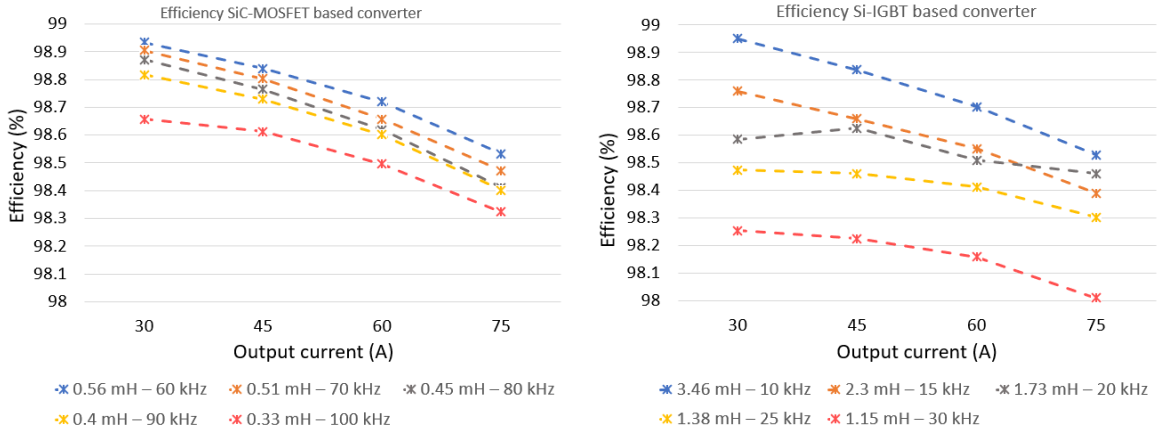


Figure 10. Total 3-leg converter loss for SiC-MOSFET-based and Si-IGBT-based converters.



(**a**) (**b**)

Figure 11. Efficiency comparison: (**a**) SiC-MOSFET-based converter and (**b**) Si-IGBT-based converter.

5.3. Heat Sink Volume

In order to conduct a throughout comparison of the two converters, the heat sink volume and cost should also be taken into account. The heat sink volume analysis was based on the power loss of the two converters at highest output current (75 A) and considering 50 °C heat sink temperature. In order to evaluate the heat sink volume, it is necessary to calculate the thermal resistance of the heat sink:

$$r_h = \frac{T_h - T_a}{P_{tloss}} \tag{16}$$

where T_h is the heat sink temperature, T_a is the ambient temperature and P_{tloss} is the total converter loss.

Once the r_h is calculated, it is possible to obtain the heat sink volume based on natural air convection [33]. The minimum heat sink volume can be obtained from the fitting function:

$$Vol_{heatsink} = 3263e^{-13.09r_h} + 1756e^{-1.698r_h} \tag{17}$$

where $Vol_{heatsink}$ is expressed in cm^3 and r_h in Ω. Equation (17) in [33] has the results of the curve fitting of various extruded naturally cooled heat sinks against heat sink thermal resistance.

Heat sink volume calculated from the curve fitting function for the two converters is presented in Figure 12, starting from the lowest switching frequency considered for both converters. A room temperature of 25 °C was selected as ambient temperature. The results show that the SiC-MOSFET-based converter has an increase of around 3% only in the case of 0.45 mH–80 kHz pair. In the other cases, the Si-IGBT-based converter has higher heat sink volume, with the highest difference of 7% in the case of highest switching frequency.

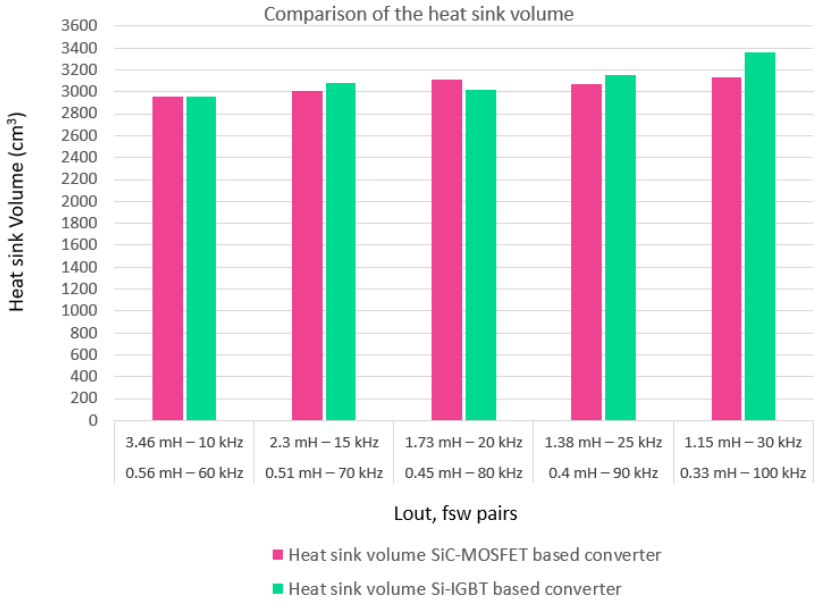


Figure 12. Comparison of the heat sink volume at 75 A output current and 50 °C heat sink temperature for the two converters.

5.4. Cost Comparison

This section presents the cost comparison of the two interleaved dc–dc converters, taking into account only the costs that are different for the two converters, i.e., the switching device costs, the heat sink costs and the inductor costs. The same cost was considered for the other components (for example gate driver, power cables, etc.), and therefore was not included in this comparison.

In Figure 13 is shown the comparison of the converter efficiency (3-legs, including inductors), the total volume (heat sink and inductor, in dm^3) and total converter cost (in € per kW). For the

efficiency comparison, the power switch losses were taken directly from the realistic circuit model implemented in PLECS, while for the different inductors they were calculated analytically. Note that the costs in Figure 13 refer to the sample prices of the main parts' manufacturers in Europe. Having in mind that the price of SiC-MOSFET devices is 2–3 times the price of IGBT devices, and the costs of different inductors for the SiC-MOSFET-based converter generally being lower (due to lower volume), the goal of this analysis was to verify if the difference of the device cost can somehow be compensated with the lower inductor cost. Namely, Figure 13 confirms this fact, where the SiC-MOSFET-based converter shows lower total cost for all the L_{out}–f_{sw} pairs. The trend of the cost curve for the SiC-MOSFET-based converter is almost flat, with the lowest cost for the highest switching frequency, i.e., 100 kHz. The Si-IGBT-based converter shows more cost variation, with the lowest cost for the highest switching frequency as well. For the higher switching frequencies, the two costs are practically the same for each device.

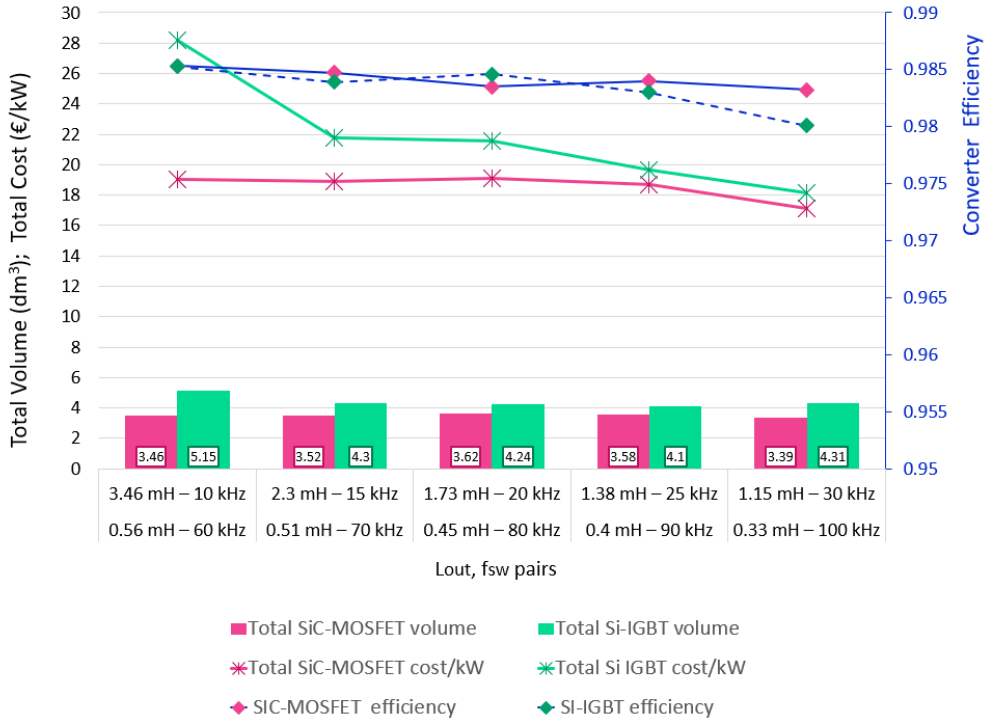


Figure 13. Efficiency, cost and total volume comparison of the two converters at 75 A output current and 50 °C heat sink temperature.

The total volume and efficiency confirm the advantage of using the SiC-MOSFET-based converter. The efficiency is almost always higher or equal to the one of the Si-IGBT-based converter. The only case in which the Si-IGBT-based converter showed higher efficiency was for 1.73 mH–20 kHz pair. The trend of the SiC-MOSFET efficiency curve is more flat, while the Si-IGBT-based converter shows higher variations with the lowest efficiency for 30 kHz switching frequency.

The real benefit can be seen in the total volume, where the lower volume can be noted for all the L_{out}–f_{sw} pairs in the SiC-MOSFET-based converter. For the highest switching frequency, SiC-MOSFET-based converter offers the lowest total volume. Generally, Figure 13 leads to the conclusion that the best working conditions for Si-IGBT-based converter could be medium switching frequencies (20 kHz and 25 kHz), where the cost, volume and efficiency differences are less marked, while the worst working conditions are the lowest switching frequencies, with elevated cost and volume difference. On the other hand, the real advantage of the SiC-MOSFET-based converter can be seen at high switching frequencies, where the cost is practically the same for the two converters (and lowest for all cases), efficiency remains higher and total volume is lower.

These considerations, together with the fact that the prices for SiC-MOSFET devices tend to reduce greatly over ther years, indicate the convenience of using SiC-MOSFET devices, especially given the fact that it offers lower total volume.

6. Conclusions

An investigation of the three-phase interleaved dc–dc topology applied to the EV fast chargers was presented in this paper. This configuration permits the use of classic and reliable three-phase power switch devices, featuring high reliability and modularity, making it particularly interesting for EV fast charging.

Two technologies were considered for the efficiency comparison: dc–dc interleaved converters with SiC-MOSFET power devices and Si-IGBT power devices, on a wide range of switching frequencies and output inductances. The comparison was made by imposing the same requirements on the ripple of the output current (5%), in order to reduce the battery stress and extend its life.

The two converters were considered with the optimal switching parameters, based on the analysis done on detailed realistic parasitic circuit model and experimental measurement. The goal was to have the safe operation and minimum losses for both converters. The output inductor design follows the same criteria. For the simulation analysis, the spice models describing the realistic and dynamic behavior of the power switches and based on the experimental tests were utilized and verified both with LTspice and PLECS simulation packages.

The results show the convenience of using SiC-MOSFETs for the three-phase interleaved dc–dc topology on the wide range of L_{out}–f_{sw} pairs. They also lead to the conclusion that the best working conditions for Si-IGBT-based converter could be medium switching frequencies (20 kHz and 25 kHz), where the cost, volume and efficiency differences are less marked, while the worst working condition is the lowest switching frequency, with elevated cost and volume difference. This is also the working condition where one could prefer the Si-IGBT solution due to its proven reliability and wide utilization by the industry. On the other hand, the real advantage of the SiC-MOSFET-based converter can be seen at high switching frequencies, where the cost is practically the same for the two converters, efficiency remains higher and total volume is lower.

Moreover, the analysis has shown that the higher price of SiC-MOSFET devices can be compensated for by the fact that the inductors utilized in the SiC-MOSFET-based converter have considerably lower costs due to the lower volume. In fact, the SiC-MOSFET-based converter showed lower costs for all L_{out}–f_{sw} pairs. However, this is likely to be changed with greater reductions in the price of SiC-MOSFET devices in upcoming years, making in this way the cost difference more significant.

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