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Abstract—Lithium-Ion batteries are playing an essential role in electric vehicles and renewable sources development. In order to reduce the charging time, high power chargers are necessary. However, lithium-ion chemistry limits the maximum current and charging speed. The diffusion rate of lithium ions into the electrodes determines the rate of charging. The slow lithium diffusion, especially experienced after high current rates, inevitably results in concentration polarization. The increase of the concentration polarization, in addition to the growth of the charging time, may lead to a faster battery deterioration. To deal with this obstacle, the Pulse Charging (PC) protocol has been proposed. There is no common opinion about the benefits given by the PC to the battery charging process in comparison with the conventional constant-current, constant-voltage (CCCV) protocol. Nevertheless, the purpose of this work is to provide an overview of possible methods that can be used to generate current pulses, without focusing on its advantages. Different techniques with the corresponding control algorithms have been implemented and analyzed through simulations in MATLAB/Simulink environment.

Index Terms—Pulse Charging, Fast Charging, Lithium Batteries, Battery Charging Methods, Smart Battery Cell

I. Introduction

Lithium-Ion (Li-ion) batteries are nowadays crucial in the development of Renewable Energy Sources (RES), electric power systems, and Electric Vehicles (EVs). This kind of batteries presents high power and energy density in comparison with other technologies. However, the battery market is requiring even more capacity, shorter charging time and longer lifetime. This is especially true in EV applications, where the "range anxiety" of the users and the required charging time are limiting the expansion of the EVs. For these reasons, the battery's cell chemistry should not be the solely investigated field. More efforts must be undertaken for studying an optimal charging protocol that eventually will guarantee the best battery performance in terms of efficiency, charging time, and battery lifetime.

During the charging process, the lithium ions (Li+) are deintercalated from the cathode and intercalated to the anode passing through the electrolyte. Correspondingly, the formation of cations (oxidation) produces an increase of the cathode potential, meanwhile the potential of the anode decreases (reduction), leading to a cell voltage increase. When the cell voltage has reached a certain threshold value (depending on the battery type), further oxidation may lead to a cathode material instability. Moreover, non-aqueous electrolytes become easier to decompose, resulting in metallic lithium deposition on the anode (lithium planting phenomena). For the previously stated reasons, a maximum charging voltage is usually introduced. The conventional Li-ion battery charging process consists of two phases, namely Constant Current (CC) and Constant Voltage (CV). In the first phase, the battery is charged with a constant current until the cell potential reaches the predefined voltage limit (about 4.2 V for Li-on battery cells) [1]. While, the second phase employs a constant voltage at the battery terminals until the charging current reaches a preset cutoff value. The charging parameters (voltage limit and charging current) may influence the charging-time and the lifetime of the battery. The whole process is commonly known as the CCCV protocol.

Multiple alternative charging protocols have been recently introduced in the literature [2]. The Boost Charging (BC) strategy is derived from the CCCV protocol. It introduces an additional CC interval at the beginning of the CC phase of a typical CCCV profile, regularly with higher value of charging current. This supplementary boost interval reduces the total charging time without deteriorating the battery's life cycle, taking advantage of the smaller lithium plating susceptibility at low State of Charge (SoC) levels. After the preliminary boost interval, the charging process turns into a conventional CCCV protocol. Another charging technique is the so-called Multi-Stage Current Charging (MSCC) protocol. The CV phase, in this charging strategy, is substituted by a series of CC stages, having a gradual decreasing current profile. This swap has been introduced due to the fact that the CV phase normally extends the total charging time.

Another possibility is the Pulse Charging (PC) protocol that consists on charging the battery pack with current pulses. This introduces relaxation periods during the charging process, which permits deep intercalation of the lithium ions inside the electrode. Consequently, the effect of concentration polarization is decreased, and Li-ions diffusion rate is respectively increased. The main parameters of this method are the pulse frequency, the duty-cycle and the charging current amplitude. Several studies in the literature use different values of these

parameters and report different results. The authors in [2, 3, 4] adopt a fixed pulse frequency and a given duty-cycle. The result of this study is a higher degradation of the electrodes in the case of the PC protocol. However, by adapting the pulse frequency, it has been demonstrated the effectiveness of this protocol in comparison with the CCCV method in terms of charging time and battery lifetime [5, 6, 7, 8]. It can be also observed that by modifying the relaxation time and current amplitude during the charging stage, it is possible to minimize the concentration polarization and optimize the charging process [6, 9]. Furthermore, by expanding the relaxation time and reducing the current amplitude at the end of charging action, it is possible to obtain better results than what it would have been with a pulse charging employing constant parameters. Finally, other authors have shown that the charging efficiency can be increased by altering the pulse frequency with the aim to minimize the internal battery impedance [6, 10].

The purpose of this work is to provide an overview of the methods that can be used for generating current pulses, regardless of whether it provides charging benefits or not. In the following sections some methods for generating current pulses at battery terminals are investigated. The focus was mainly on power electronics, feasibility, cost/complexity of implementation, and the control of key PC parameters (pulse frequency, duty-cycle, and charging current amplitude). The paper is organized as follows: Section II describes different methods to generate current pulses; overall, this section is dedicated to power electronics hardware and system control. Section III illustrates simulation results of the described methods, analyzing currents, voltages, and battery SoC values. Finally, conclusions and further discussions are presented.

II. PULSE CHARGING METHODS

Four distinct methods suitable for generating PC profiles are described in this section. Moreover, a general description of the control logic is provided. The involved control parameters are: the pulse frequency (f_c), the duty-cycle (δ), the peak current (I_{peak}), and the mean current (I_{mean}). The duty-cycle is defined as:

$$\delta = \frac{t_{ON}}{T_c} \tag{1}$$

where T_c is the switching period and it is equal to $1/f_c$. Then, the relaxation time (t_{OFF}) can be evaluated as:

$$t_{OFF} = T_c(1 - \delta) \tag{2}$$

However, the mean current depends on the peak current value and on the duty-cycle as it is shown in (3).

$$I_{mean} = \delta I_{peak} \tag{3}$$

Only the parameters δ, f_c, and I_{peak} are used to control the current pulses and to optimize the charging process. The typical current profile is shown in Figure 1 (blue signal). In Figure 1, it can be noticed that even though the amplitude and the frequency of pulses are constant, the average current (red signal) changes according to the duty-cycle.
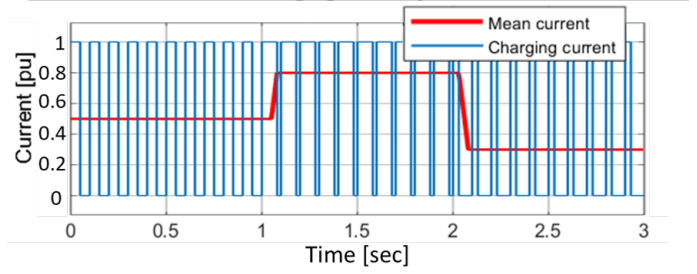

Fig. 1: PC profile @ frequency 10 Hz and 1C peak current.

A. Hysteresis Current Control Method (HCCM)

The Hysteresis Current Control Method (HCCM) takes advantage of a hysteresis regulator to generate current pulses. The charger is composed of a buck dc/dc converter coupled to the power grid through a rectifier (ac/dc converter). The current pulses at the battery side are achieved by the proper control of the buck converter's switch. The switch's gate signal is generated to manage the frequency and the duty-cycle of the pulse current. In order to keep constant the peak current value (e.g. $I_{peak} = 10\ A$), a hysteresis controller is introduced to regulate the gate signal. Figure 2 shows the buck converter schematic model where V_{dc} is the dc-bus voltage, V_b is the battery voltage, I_{dc} is the output current of the rectifier stage and I_{PC} is the pulse charging current. In order to have a pulse charging current profile as close as possible to that in Figure 1, it is necessary to set an optimal value of the hysteresis band and properly size the buck inductor. The control logic and the optimization strategy are shown in the next section.
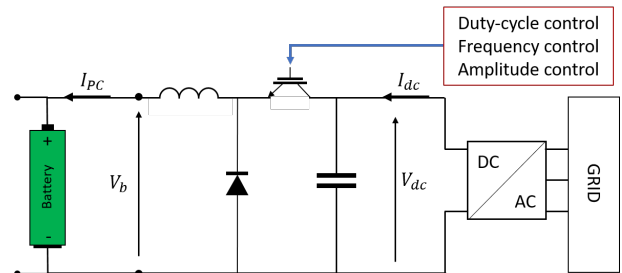

Fig. 2: Buck converter schematic model.

B. Method based on a Boost Converter (MBC)

Another possible solution to generate current pulses is to adopt a dc/dc converter with an inherent output pulse current. This method uses a boost converter to charge the battery with a predefined current profile. The dc/dc boost converter, at this instance as well, is coupled to the power grid through a rectifier and a dc/dc buck converter, as shown in Figure 3. In this method, the aim of the dc/dc buck converter is to either increase or decrease the dc voltage V_{dc} and, consequently, adjusts the peak current value. Meanwhile, the switch in the boost dc/dc stage controls the frequency, the duty-cycle and then the average value of the current pulses, keeping constant the source current.
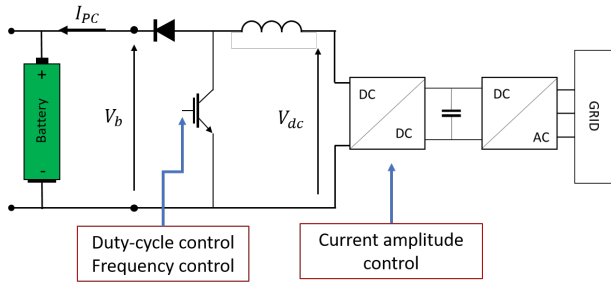
Fig. 3: Boost converter schematic model.

C. Double Switch Method (DSM)

An alternative strategy to generate PC is to work with two battery packs. These battery packs can be connected either in parallel (Figure 4 A) or in series (Figure 4 B) and they are coupled to the charger system by means of two semiconductor switches (S1 and S2) and two diodes. The charging system is composed of a rectifier and a dc/dc buck converter that provides the battery current I_b. The dc/dc converter also regulates the output voltage V_b in accordance to the battery SoC level. Considering the battery side, only the parallel configuration is described in the following.
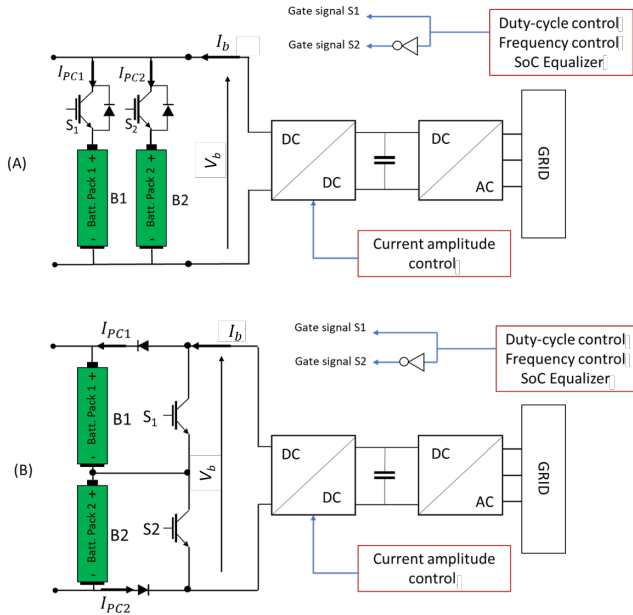

Fig. 4: Double switch method with parallel (A) and series (B) battery packs.

The switches S1 and S2 are simultaneously controlled to achieve current pulses. If the first switch (S1) turns ON, the second (S2) is in OFF state, or vice versa. In such manner, while a battery pack (e.g., B1) is under charge (injecting a current pulse), the other (e.g., B2) is in relaxation phase. In order to achieve the described charging mode, the switches' gate signals must be complementary. In this context, the task of the designed control system is to provide the desired frequency and duty-cycle. As it is visible in Figure 4, the complementary driving signal for the switch S2 is obtained by inverting the gate signal of S1. Since the value of the duty-cycle is proportional to the average current value, the balancing of the

SOCs is achieved by supplying a higher average current value to the pack with a lower SOC, and simultaneously, charging the remaining battery pack (with a higher SOC) with a lower average current. Then, control targets are the following: control the frequency of the current pulses; equalize the SoCs of the charging battery packs by means of the duty-cycle regulation; adjust peak and average values of the supplied current.

D. Bypass Battery Cell Method (BBCM)

The schematic model of the Bypass Battery Cell Method (BBCM) is illustrated in Figure 5. It consists of N series-connected Smart Battery Cells (SBCs) that in turn are composed of a battery cell connected to a half-bridge chopper [11, 12]. As previously described, a rectifier and a dc/dc buck converter are adopted to provide the connection to the grid and the regulation of the battery voltage V_b.
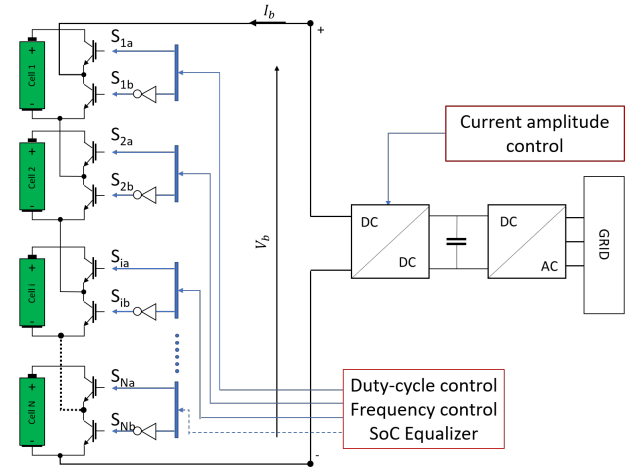

Fig. 5: Bypass battery cells Method: schematic model.

Figure 6 shows a basic principal of the BBCM operation: the smart battery pack inserts or bypasses the battery cell through the half-bridge chopper. If the upper switch (S_{ia}) turns ON and the lower switch (S_{ib}) is OFF, the cell is inserted and then it is in the charging stage. Vice versa, the corresponding cell is bypassed, staying in the relaxation phase. Figure 6 (A) and Figure 6 (B) display the charging and the bypass mode of a SBC, respectively. In order to keep constant the battery voltage (V_b), commutations of switches in SBCs must be coordinated, and only one cell at a time must be bypassed. Consequently, the total battery pack voltage is obtained by considering the contribution of the inserted cells:

$$V_b = \sum_{i=1}^{N} S_{ia} \cdot v_i \qquad (4)$$

where v_i is the single-cell charging voltage and S_{ia} is the status of the upper switch ($S_{ia} = 1$ if the switch is on). The duty-cycle and the frequency of generated current pulses are controlled by the SBC, while the dc/dc buck converter handles the peak current value (I_{peak}). The SoC equalization of individual cells is achieved by controlling the duty-cycle. The control system decreases the duty-cycle of the cell with the highest SOC by leading a reduction of the average cell

current. The cell is then charged less than the others by achieving the equalization.
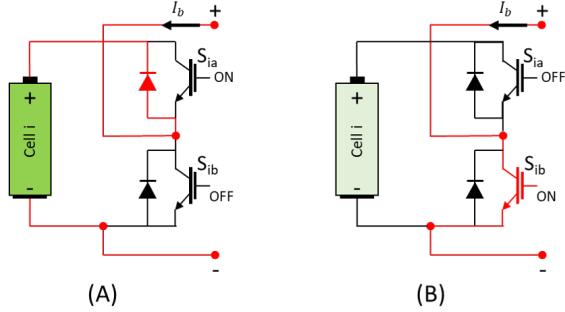

Fig. 6: SBC working principle: (A) the cell is inserted (charging time), (B) the cell is bypassed (relaxation time).

III. SIMULATIONS

The previously pulse-based charging strategies have been simulated in MATLAB/Simulink environment and the achieved results are reported in this section. The current analysis is focused on operational behaviour of presented charging protocols, specifically examining output currents, voltages, and battery/cells' SoC values during the PC period. The battery model is based on a Sony 18650 Li-ion battery cell, whose technological parameters have been introduced in Table I. The Simscape Electronics library was used to model the battery behavior.

TABLE I: Sony 18650 Li-ion battery cell parameters

Rated capacity	Nominal disc. current	Nominal voltage	Internal resistance	Response time
2.5 [Ah]	1 [A]	3.6 [V]	14 [mΩ]	30 [sec]

The simulated battery pack is built up by 96 series-connected individual battery cells. Initial SoC values of the cells were set at $SoC_0 = 10\%$. It has been assumed that the charging process stops when SoC of individual cells reaches $SoC_f = 90\%$. The initial battery pack open-circuit voltage was fixed at $V_{10\%} = 357\,V$, while the charging algorithm limits the output current in case the voltage reaches the cut-off value $V_{max} = 403\,V$.

Figure 7 depicts the working principle of the hysteresis controller: the blue signal represents the reference battery current I_b^*, and the red signal is the simulated battery current I_b. The ramp time (t_r) is the time that a current pulse needs to reach its peak value, and d_{hy} is the hysteresis band. By accurately setting these parameters, it is possible to optimize the charging action, in fact as soon as values of t_r and d_{hy} diminish, the shape of I_b is approaching to I_b^*, but the switching frequency consequently increases. Then, a proper compromise is needed. The value of t_r determines the buck inductor size. Following the generic time-constant rule, once the value of the inductance drops, the ramp time shrinks as well. The dc-bus voltage is assumed to be constant and its value is $V_{dc} = 565\,V$. On the other hand, V_b depends on the battery SoC value and the battery current. Considering a ramp time between 1% to 10%

of T_c and defining $d_{t_r} = (t_r/T_c) \cdot 100$, the buck inductance (L) can be calculated as follow:

$$L = \frac{(V_{dc} - V_b)}{I_{peak}} \left(\frac{d_{t_r}}{100}\right) T_c \qquad (5)$$
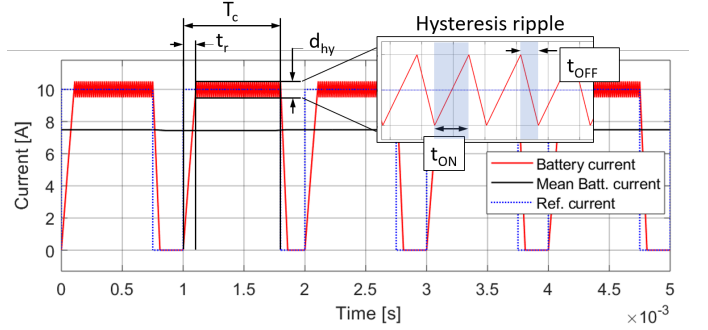

Fig. 7: HCCM: current waveforms and hysteresis control parameters.

Bearing in mind a constant hysteresis band equal to $\pm 5\%$ of I_{peak} (10 A), d_{hy} is equal to $1A$. In order to analytically evaluate the switching frequency, the inductor equations have been introduced:

$$\begin{cases} \frac{(V_{dc}-V_b)}{L} \cdot (t_{ON}) & = d_{hy} \\ -\frac{V_b}{L} \cdot (t_{OFF}) & = -d_{hy} \end{cases} \qquad (6)$$

where $t_{ON} = \delta T_s$ and $t_{OFF} = (1 - \delta)T_s$. T_s represents the switching period, thus the switching frequency is $f_s = 1/T_s$. Solving the set of equations (6) the switching frequency can be determined by:

$$f_s = 100 \frac{V_b}{V_{dc}} \frac{I_{peak}}{d_{hy} d_{tr}} \cdot f_c \qquad (7)$$

Equation (7) shows that f_c is limited by the highest switching frequency of the converter. Figure 8 presents the pulse frequency that can be reached considering the ramp time slot from 1% to 10% of the corresponding pulse period, and applying a switching frequency up to 100 kHz.
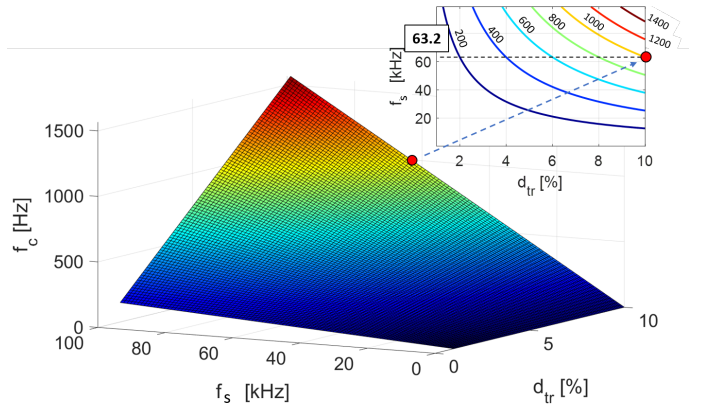

Fig. 8: HCCM: max pulse frequency depending on the maximum switching frequency during the hysteresis ripple (f_s) and by the ramp time (d_{tr}).

From Figure 8 it can be noted that to reach a pulse frequency of 1kHz with a ramp time equal to 10% of the corresponding pulse period, a converter switching frequency of 63.2 kHz is required. In all performed simulations, the battery pack has been charged applying current pulses with constant frequency

in the order of few kHz (e.g. $f = 1kHz$). The charging rate is set to 4C (where peak current is $I_{peak} = 10\,A$). Nevertheless, the mean charging current also depends on the applied duty-cycle value. The initial duty-cycle is 0.75, which corresponds to an average 3C rate ($I_{mean} = 7.5\,A$). As soon as the battery voltage reaches its upper limit 403 V, the control algorithm decreases the mean current to keep the mean value of the battery voltage (V_{Bmean}) constant. Figure 9 displays the SoC, output current and voltage profiles during the simulated charging process.
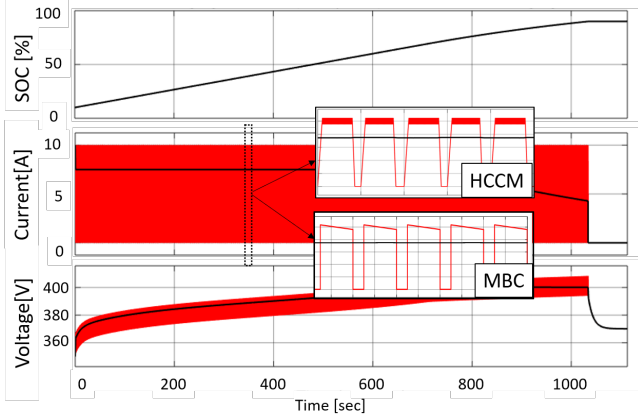

Fig. 9: HCCM and MBC charging process: SoC - top figure; battery pulse current (red line) and battery mean current (black line) - middle figure; battery voltage (red line) and battery mean voltage (black line) - bottom figure.

To reach higher frequencies of current pulses, the MBC strategy has been implemented. The MBC switching frequency is the same as the pulse frequency, then utilizing the MBC technique, a higher value of the current pulse frequency might be achieved. Figure 9 displays current profile differences between HCCM and MBC protocols. Figure 10 depicts a basic block-diagram of the MBC controller. The value of V_{dc} is adjusted in order to achieve the reference peak current, which is equal to $10\,A$ in these simulations. In the meantime, the duty-cycle is controlled to keep $I_{mean} = I^*_{mean}$. When V_{Bmean} reaches its upper limit 403 V, the control acts on I^*_{mean} keeping constant the voltage at the utmost value.
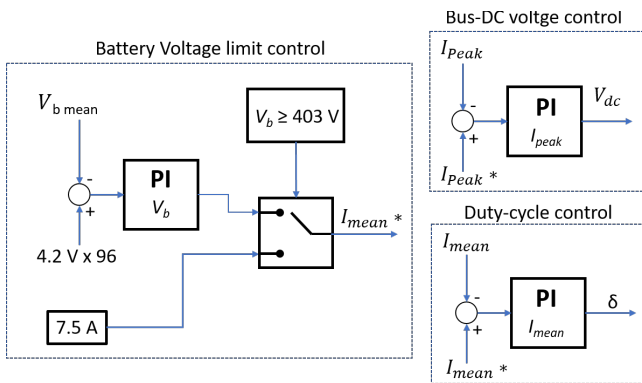

Fig. 10: MBC control system.

For the DSM and BBCM methods, it is necessary to introduce the SoC equalization rule in their control design. As it was described in Section II, in order to achieve the SoC balance for each pack in DSM and for each cell in BBCM,

the mean charging current must be controlled individually: a lower average current charges the cell (pack) with the highest SoC, and vice versa, a higher average current is supplied to the cell (pack) with the lowest SoC. If the SoCs are equal, all cells (packs) are charged with identical average current (the same duty-cycle). Figure 11 shows the performance of the equalizer in the DSM charging strategy. The initial SoC value of pack 1 is set to $SoC_{01} = 15\%$, while for pack 2 is $SoC_{02} = 10\%$. In the first phase of charging, the pack 1 average current is lower than pack 2 current. After about 100 seconds, the SoCs are equalized, and the charging currents reach the same value for both battery packs. When the battery voltage reaches 403 V, the peak value of the charging current decreases to keep the voltage limit constant, while the duty-cycle does not change as long as the individual SoCs are equal.
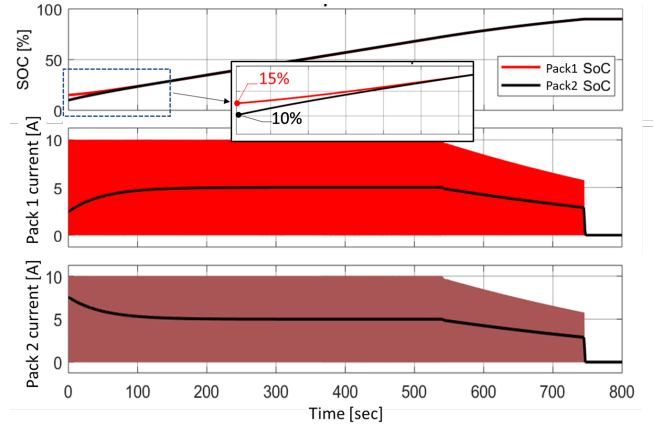

Fig. 11: DSM pulse charging process with 2 battery packs of 1.25 Ah capacity: SoCs - top figure; battery pulse current (red line) and battery mean current (black line) of pack 1 - middle figure; battery pulse current (brown line) and battery mean current (black line) of pack 2 - bottom figure.

A scale-down BBCM model of a battery pack with $N = 4$ series-connected SBC was simulated. The dc/dc buck converter supplies a battery current equal to $10\,A$ to the battery pack. During the BBCM charging process, only $(N-1)$ cells (3 in the considered case) are simultaneously inserted and then they result under charge. The remaining one is instead bypassed. This leads to a relaxation period for the bypassed cell.

Figure 12 shows the individual cell SoCs equalization process, applying BBCM charging strategy. The simulation is initialized using for each cell distinct SoC values: $SoC_{01} = 12\%$, $SoC_{02} = 10\%$, $SoC_{03} = 11\%$, $SoC_{04} = 13\%$. The peak current value is equal to the current provided by the dc/dc buck converter (10 A). During SoC equalization, the duty-cycle of current pulses is controlled in order to adjust the average cell current. For this aim, a sorting algorithm is adopted to sort the cells based on the SoC values. Once the SoCs are sorted, a lower duty-cycle is assigned to the cell with the highest SoC. As soon as cell SoCs are balanced, the equalization process will set the same value for all the duty-cycles by leading the same mean current for all the cells:

$$I_{mean} = I_{peak} \cdot \frac{N-1}{N} \tag{8}$$

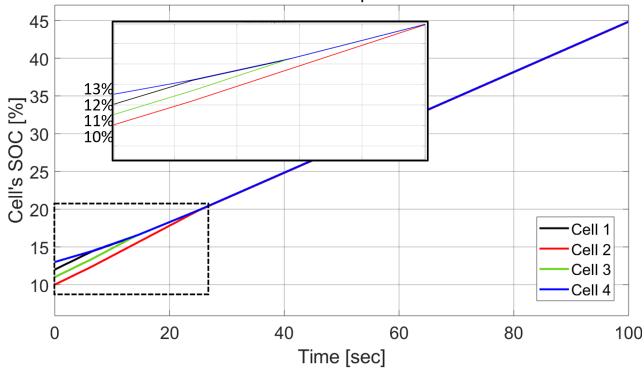It is visible that the current mean value after the SoC equalization has reached $I_{mean} = 7.5A$.

Fig. 12: BBCM simulation: cells SoC equalization.

IV. DISCUSSIONS AND CONCLUSIONS

The main purpose of this work is to propose and discuss possible circuit schemes that can be used for the PC. The supposed advantages of PC in comparison with the CCCV protocol (in terms of charging efficiency, battery lifetime, and total recharging time), as it was shown in previous studies, depend on the PC parameters, namely frequency of pulses, duty-cycle and peak current value. The PC methods, described in Section II, have different control logic that could eventually provide more or less operational flexibility.

The HCCM strategy allows to take advantage of duty-cycle tuning, robustness and control simplicity. However, by cause of narrow hysteresis band and restricted ramp time, the output PC current profile may be too different compared to the reference profile. Furthermore, the switching frequency is much higher than the pulse frequency ($f_c << f_s$), and for this reason, the utmost pulse frequency can be limited to a value around $1 - 1.5kHz$. To overcome the aforementioned problems, the MBC pulse charging technique was introduced.

The MBC adopts a boost converter with an inherent output pulse current. It provides flexibility of the main parameters and may reach pulse frequencies of one order of magnitude higher than the HCCM method. In this context, current ripple can be reduced by optimizing the boost inductor size. However, in order to decrease the peak current value, the dc bus voltage should have a wide range of variation.

In DSM method, two batteries are charged simultaneously. They are then separately supplied by pulsed currents. The DSM introduces frequency flexibility, but the regulation of the duty-cycle depends on the SoC value. At the SoC equalization stage, the control system adjusts individual duty-cycles. When the balancing is achieved, the regulator keeps constant the duty-cycle values. For this reason, in this method, only frequency and peak current management can be achieved to optimize the PC charging process. Furthermore, the equalization stage does not involve each cell but only involves the two battery packs. Then, as for the previous methods, a cell equalization strategy should be implemented separately.

Finally, the BBCM improves controllability of the PC charging, adjusting charging pulses in each cell separately.

Thanks to the SBC's control, the SoC equalization can be achieved avoiding the need of extra components. In analogous fashion as in the DSM, the duty-cycle cannot be used to optimize the charging efficiency because it is used during SoC cell equalization. However, the PC duty-cycle strongly depends on the number of series cells; in particular, it rises as the number of series cells increases.

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