A Compact System for On-line Electrochemical Impedance Spectroscopy on Lithium-Ion Batteries

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***Abstract*—A compact measurement system for electrochemical impedance spectroscopy on lithium-ion batteries is presented. The system is composed of vector impedance analyzer (VIA) and state parameter estimation from raw impedance data. The VIA is based on ΔΣ digital-to-analog and analog-to-digital conversions to achieve the compactness, low-power consumption and high resolution required to be potentially integrated within a battery cell. The estimation of state parameters is based on equivalent circuit models. The proposed measurement system aims at enabling on-line estimation of battery state parameters, like state-of-charge and state-of-health, through non-invasive electrochemical impedance spectroscopy technique.**

A prototype of the compact measurement system was realized to assess the proposed approach. Experimental results are provided and validated by comparison with a reference laboratory instrument, showing a good agreement. On-line discharge tests are also provided. These experimental results are then used for modeling purposes, showing that the proposed system is suitable for usage in conjunction with a battery management system for on-line monitoring of the battery cell, and future smart actuation on the battery operation for optimization of its performance and lifetime.

***Keywords*—Battery, EIS, Modeling, Impedance measurement**

I. Introduction

Batteries have attracted considerable research interest in recent years due to their increasing usage in a variety of applications. Such applications, which were once limited to low-power systems such as portable electronics, are recently expanding towards higher energy scenarios, including electrical vehicles and energy storage systems [1]. In this context, lithium-ion batteries are among the most commonly employed, thanks to their high energy density and compact size [2].

In order to ensure safe operation of lithium-ion batteries and improve efficiency, battery management systems typically employ parametric battery models. By identifying the model parameters, it is possible to indirectly evaluate the State of Charge (SoC) and the State of Health (SoH) of the battery. Furthermore, the models allow for simulating the battery behavior under different SoC and SoH conditions, thus allowing to develop and test algorithms for battery management [3]. The model parameters are typically identified by processing measurement data obtained by electrochemical impedance spectroscopy (EIS) [4]. To obtain EIS data efficiently, broadband and narrowband measurement systems have been proposed in the literature [5]. In the former system, broadband signals are fed to the battery input and excite a wide range of frequencies simultaneously. Such signals may be implemented efficiently by using binary or ternary sequences that are designed specifically for system identification [6] [7]. The latter system consists in exciting the battery by using a narrowband signal and spanning the center frequency of this excitation. The narrowband measurement system is intrinsically slower but with superior resolution [8], [9]. Most EIS instruments are benchtop devices and cannot be applied directly on the field to characterize batteries while they are operating. However, the capability of measuring the impedance of a battery in a cost-effective, efficient, and fast manner is crucial for the safe and efficient operation of lithium-ion batteries, thus motivating research in this area.

This paper proposes a compact system able to gather EIS data and estimate the target parameters of interest by using suitable electrical models. The proposed system could potentially operate "*on-line*", that is while the battery is under operation, thanks to its compactness, low power consumption, and isolation from the battery under test. Compactness and *on-line* operation of the proposed system could enable the development of built-in battery management systems, fault warning solutions, and real-time diagnostics.

A prototype of the system is implemented and compared with a commercial benchtop instrument used as the gold standard for EIS. The prototype consists of a vector impedance analyzer (VIA) realized as a small printed circuit board. The VIA core is implemented as an application-specific integrated circuit (ASIC) to reduce size and allow energy-efficient operations. This device measures the battery impedance at several frequencies with a very small form factor and overall low power consumption. Potentially, all the components in the realized prototype could be integrated into a single ASIC and embedded inside the battery cell itself, thus allowing for efficient monitoring of battery parameters.

The remainder of this paper is organized as follows. In Section II, the architecture of the proposed vector impedance analyzer is presented and its principle of operation is described. Then, experimental characterization results are provided in Section III. Subsequently, the usage of such experimental results for modeling and parameter

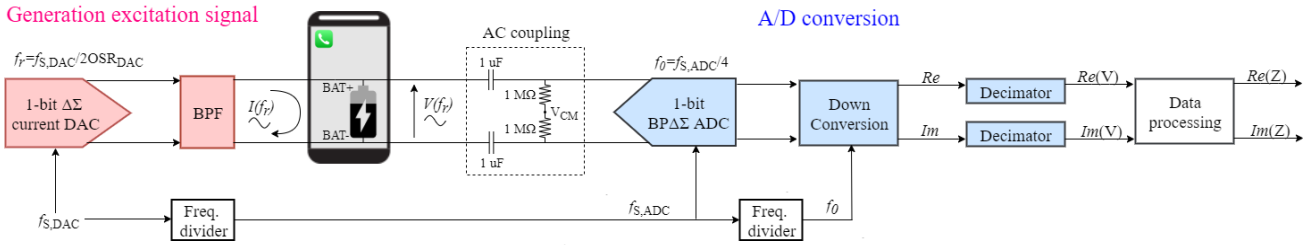

Fig. 1. Block scheme of the vector impedance analyzer architecture.

identification purposes is investigated in Section IV. Finally, conclusions are drawn in Section V.

II. Architecture of the Vector Impedance Analyzer

The VIA architecture is based on a delta-sigma (ΔΣ) digital-to-analog (D/A) converter for the generation of a narrowband AC excitation signal and a band-pass delta-sigma (BPΔΣ) analog-to-digital (A/D) converter for the acquisition and conversion of the response signal (Fig. 1) [8] [9]. The use of 1-bit ΔΣ D/A and A/D conversion architectures ensures very low-power consumption while preserving high resolution, thanks to the well-known oversampling and noise shaping. In addition, relatively power-hungry computational steps inherent to ΔΣ D/A conversion (e.g., noise shaping) are implemented off-line via software, with a considerable reduction in power consumption. These operations are realized just once, and the resulting bit sequence is simply pre-stored into the system memory. Following this approach, the 1-bit ΔΣ D/A is realized in hardware by just a 1-bit I/O port connected to a memory device. The 1-bit BPΔΣ A/D conversion is more power-efficient than conventional low-pass A/D conversion. It makes possible to replace non-linear and noisy analog mixers with a low-power digital down-conversion stage, which provides (after suitable filtering and decimation) full vector information on the battery impedance. Finally, the band-pass architecture of the A/D converter minimizes the in-band thermal noise.

The combination of ΔΣ D/A conversion with the implementation of BPΔΣ A/D conversion also allows real-time tuning of the operative excitation frequency f_r, so as to span the target portion of the frequency domain. More precisely, the frequency f_r of the excitation sine wave can be tuned in real-time by simply varying the D/A converter sampling frequency $f_{S,DAC}$, since these two frequencies are related by the following equation:

$$f_r = \frac{f_{S,DAC}}{2 \cdot OSR_{DAC}}, \qquad 0$$

where OSR_{DAC} is the chosen oversampling ratio of the ΔΣ D/A converter implemented in the architecture.

BPΔΣ A/D conversion works in a similar way with respect to the conventional low-pass ΔΣ technique, but benefits from the bandpass nature of the signal to be acquired to obtain higher OSR values (thus, more effective noise shaping) with lower sampling frequencies (i.e., lower consumption). In this case, the oversampling ratio of the BPΔΣ A/D converter is defined as the ratio between the Nyquist frequency $f_{S,ADC}/2$ and the bandwidth B_W of the acquired signal:

$$OSR_{ADC} = \frac{f_{S,ADC}}{2 \cdot B_W}, \qquad 0$$

in which $B_W << f_0$, which is the center frequency of the BPΔΣ. The latter can be parametrized to the sampling frequency $f_{S,ADC}$ through the linear relation:

$$f_{S,ADC} = P \cdot f_0,$$

where P is a factor depending on the actual implementation. A clever choice is P = 4 because it simplifies the electronic implementation of the BPΔΣ. Since $f_{S,ADC}$ is internally generated from $f_{S,DAC}$ as follows:

$$f_{S,ADC} = \frac{f_{S,DAC}}{K_{DIV}}, \qquad 0$$

then the frequency equalization is assured by the combination of (1) and (3). The factor K_{DIV} is set by the hardware frequency divider and is a power of two for simple implementation. Therefore, the target frequency spectrum can be easily spanned only by sweeping $f_{S,DAC}$, while the frequency equalization of the D/A and A/D conversions is assured by construction.

The DC voltage of the battery under test is decoupled both from the D/A and A/D converters. The 1 Hz - 10 kHz band-pass filter (BPF), placed in between the D/A converter and the battery, removes the high-frequency noise of the ΔΣ excitation and prevents slow-varying DC-like currents from battery to D/A converter without affecting the normal behaviour of the battery and of the device powered by the battery itself. The bandwidth of the BPF is chosen with the twofold aim of *i)* not limiting the frequency sweep required to estimate the interesting portion of the electrochemical impedance (EI) spectrum of the battery under test, and *ii)* minimizing the noise associated with the ΔΣ excitation. The AC coupling on the A/D side separates the power supply domain of the VIA from the battery, so as to prevent spurious currents through the electrostatic discharge (ESD) circuits placed on the input of the BPΔΣ. The AC coupling circuit consists of two 1-μF capacitors in series to the battery to block the DC voltage, and of two 1-MΩ resistors to set the common-mode DC input voltage of the A/D converter.

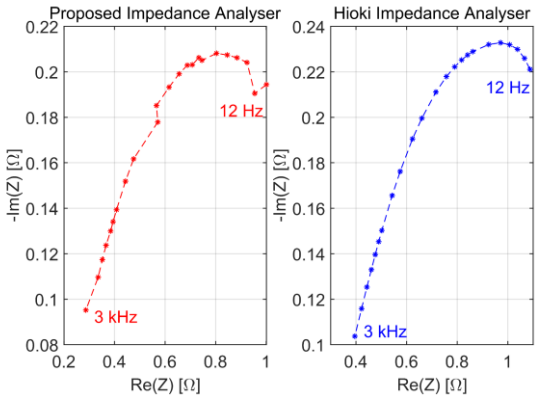

Fig. 2. Comparison of the impedance estimates obtained by the proposed impedance analyzer with the impedance reference values, in the case of a fully charged LIR2032 coin cell. Each point in the Cole-Cole plot obtained by the proposed VIA is the result of an average over 30 measurement samples.

The proposed VIA could potentially be used to on-line monitor the EI of battery cell even while the battery is supplying a circuital load. The AC current excitation $I(f_r)$ provided by the VIA is AC-injected into the battery through the BPF and adds to the slow-varying DC-like current generated by the battery itself. The AC excitation will flow through the battery and not through the load because of the low input impedance of the battery. AC voltage across the battery due to slow variations of the load is rejected by the intrinsic frequency-locked operation of the VIA. The proposed VIA architecture is appropriate to be implemented in very compact dimensions, down to few mm^2, by exploiting microelectronic techniques. This capability, together with the low power consumption and the electrical isolation from the battery, allow to integrate the VIA with every battery module or even every battery cell, opening new perspectives in battery applications.

III. Experimental Results

With the aim to assess the functionalities of the VIA architecture and its applicability to EIS on battery modules, a prototype of the VIA is realized on a 3-cm x 6-cm PCB board [9]. The main sub-circuits are realized in a CMOS ASIC while ancillary digital sub-circuits are implemented onto a microcontroller (µC). This approach does not achieve fully optimized compactness but guarantees best resolution and accuracy together with a good level of flexibility and testability. On one hand, the CMOS implementation of the analog front-end ensures better noise immunity and lower parasitics, improving prototype robustness and accuracy. On the other hand, the implementation of the digital algorithms in the microcontroller allows for the optimization of the measurement parameters to the target application. Following this approach, the prototype can be programmed by choosing the amplification gain as well as the amplitude and the frequency of the excitation current.

The excitation frequency could be spanned in the range 12 Hz – 45 kHz but only the 12 Hz – 3 kHz range will be used in the following measurement. For the tests on this prototype, the low-frequency limit is set by a trade-off with the time required for a complete measurement of the spectrum. Due to technological limitations, each frequency point in the Cole-Cole plot is the result of an averaging over 30 measurement samples, in order to lower the random noise that affects the single measurement. A low-frequency limit of 12 Hz has been selected to maintain a suitable measurement time without limiting the "real-time" characteristic of the "on-line" operation of the VIA.

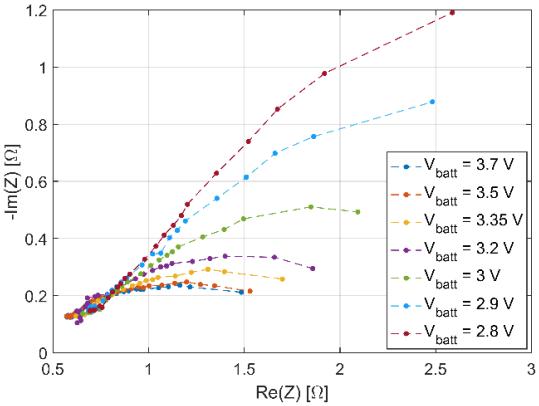

Fig.3. On-line acquisition of the impedance data of a LIR2032 at different battery voltage while it is discharged by a constant DC current. Each point in the Cole-Cole plot obtained by the proposed VIA is the result of an average over 30 measurement samples.

The prototype consumes a maximum of 500 mW when it generates the maximum excitation frequency of 45 kHz, but the power consumption lowers to 100 mW when operating at f_r = 1 kHz. It is worth noticing that most of the power is dissipated by the general-purpose µC while the ASIC consumes only 1.45 mW. Future implementations of the VIA may integrate all the blocks shown in Fig. 1 into a single ASIC to further boost the performance, minimize the power consumption as well as the form factor.

The impedance analyzer architecture was validated by the measurement of the EI spectrum of commercially available lithium-ion rechargeable coin cells (LIR2032) of chemistry lithium cobalt oxide ($LiCoO_2$), having a weight of 2.5 grams, nominal voltage of 3.8 V, and nominal capacity of 35 mAh. The prototype was configured by setting the sine wave amplitude to the maximum value of 1 mA and the amplification gain of the front-end to the maximum value of 100. Twenty arbitrarily chosen frequency points between 12 Hz and 3 kHz were generated. Fig. 2 compares the impedance estimates obtained by the proposed impedance analyzer aftercalibration with the impedance reference values obtained by using the IM3590 Hioki Chemical Impedance Analyzer, whose basic accuracy is better than 3% of the reading for the impedance magnitude and better than 0.6° for the impedance phase. The battery under test was a charged LIR2032 at the 1st cycle.

Fig. 3 demonstrates the on-line capabilities of the VIA architecture. The figure shows impedance estimates obtained by the VIA during the on-line monitoring of the LIR2032 battery under constant current discharge. The DC current from the battery was set to 10 mA by using a Keithley 2600 source measurement unit (SMU) in constant sinking operation that emulates the effect of a fixed-current load. The reported Cole-Cole plots are smoother than previous figure because the measured battery was at its 3rd cycle. The time evolution of the impedance due to the discharge process is clearly pointed out by the monitoring system visible. These results prove the correct functionality of the VIA in measuring the EI of commercial lithium-ion battery.

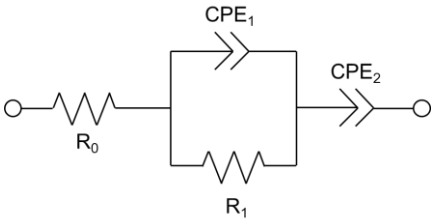

Fig. 4: Equivalent circuit of Model 1.

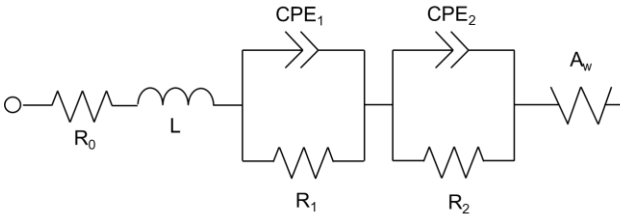

Fig. 5: Equivalent circuit of Model 2.

IV. MODELING

The experimental results presented in Section III are used to identify the parameters of models based on equivalent circuits. These parametric models can then be employed by a battery management system to evaluate the SoC and SoH of a battery under test or for simulation purposes.

In the literature, the most commonly used equivalent circuit models are based on the Randles circuit or on one of its variants, see e.g. [10]. Among these variants, to model the low-frequency behavior of the EIS curve, the Warburg element is often employed [11]. Instead, to model the high frequency behavior, a resistor in series with an optional inductor is typically used. Regarding the mid-frequency behavior, one or more cells consisting of a parallel connection between a constant-phase element (CPE) and a resistor are used.

In this paper, two models are considered and compared. These models are denoted as Model 1, whose related circuit is shown in Fig. 4, and Model 2, which is depicted in Fig. 5. The impedance of Model 1 is given by [2]:

$$Z_1(s) = R_0 + \frac{R_1}{1 + R_1 Q_1 s^{p_1}} + \frac{1}{Q_2 s^{p_2}} \quad ,$$

where Q_1 and p_1 are the parameters of CPE$_1$, Q_2 and p_2 those of CPE$_2$, $s = \mathrm{j}\omega$ is the Laplace variable, and ω is the angular frequency. The parameters of Model 1 can be grouped in vector θ_1 as follows:

$$\theta_1 = [R_0 \;\; R_1 \;\; Q_1 \;\; p_1 \;\; Q_2 \;\; p_2]^T$$

where T denotes the transpose operator. Furthermore, the impedance of Model 2 is:

$$Z_2(s) = sL + R_0 + \frac{R_1}{1 + R_1 Q_1 s^{p_1}} + \frac{R_2}{1 + R_2 Q_2 s^{p_2}} + \frac{A_w(1-j)}{s^{0.5}} \quad ,$$

where A_w is the Warburg parameter. For Model 2, we define the parameter vector θ_2 as:

$$\theta_2 = [R_0 \;\; L \;\; R_1 \;\; Q_1 \;\; p_1 \;\; R_2 \; Q_2 \;\; p_2 \;\; A_w]^T \quad .$$

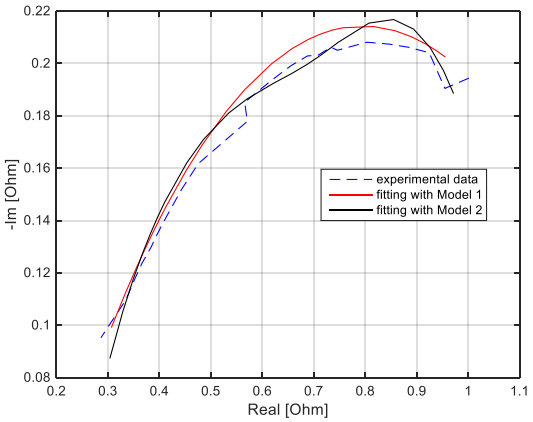

Fig. 6. Fitting results provided by the considered models 1 and 2 with experimental data obtained by the proposed impedance analyzer. The root-mean-square error (RMSE) between the Model 1 curve and the experimental data is 0.0166, whereas the RMSE between the Model 2 curve and the experimental data is 0.0129.

Let us assume that N measured values of the complex impedance $\tilde{Z}(s_i)$ are available at radian frequencies ω_i, with i=1,…,N. Based on these measurement results, the parameters of the models can be estimated by solving the following optimization problems [3]:

$$\min_{\theta_k} \sum_{i=1}^{N} (J_R^2 + J_I^2), \qquad k = 1,2$$

where $J_R = Re\{\tilde{Z}(s_i)\} - Re\{Z_k(s_i, \theta_k)\}$, $J_I = Im\{\tilde{Z}(s_i)\} - Im\{Z_k(s_i, \theta_k)\}$, and θ_k indicates the vector of the parameters to be estimated, with k=1 in the case of Model 1, and k=2 for Model 2. These optimization problems are nonlinear in the parameters. Therefore, they can be solved using iterative numeric procedures that consider the constraints on some parameters and require an initial guess of their values.

In this paper, the initialization for Model 1 is derived by observing the EIS data at different frequency ranges, based on the procedure described in [3]. Specifically, the initial value of R_0 is the high-frequency intercept with the horizontal axis, R_1 and Q_1 are initialized as the real and imaginary parts of the impedance at the maximum of the mid-frequency semicircle, respectively, and p_1 and p_2 are initialized at 0.5, which is a common value used in the literature [2]. An arbitrary initial value of Q_2=10 was used, since it was found empirically that the minimization procedure is not sensitive to the initial value of Q2. The cost function for Model 1 is minimized using a trust region reflective algorithm [12]. For Model 2, a multi-start initialization is performed. In particular, 100 random initial conditions are generated, the cost function is minimized for

each initial condition using a trust region reflective algorithm, and the parameter values that provide the lowest value of the cost function are selected.

Fitting the considered models 1 and 2 to data obtained by the realized VIA yields the curves shown in Fig. 6. A good fit to the experimental data may be observed from these curves. Moreover, for evaluation and reference purposes, the two considered models are fitted also to data obtained by the reference instrument, Hioki IM3590, as shown in Fig. 7 and 8. It is possible to notice that, when the battery voltage is 4.1 V, both models result in a good fit. However, when the battery voltage is 3.5 V, Model 2 provides a better fit, indicating that this model is more suited to capturing SoC changes, at the expense of an increased number of parameters to be estimated, which results in greater computational cost.

The computational complexity of the fitting procedures was also investigated, evaluating both the number of iterations and the processing time. The number of iterations of the trust region reflective algorithm used to solve the minimization problem for Model 1, in the case of Fig. 6, was 28 (34 ms execution time on an Intel Core i9-9900KF CPU 3.6 GHz with 32 GB of RAM), whereas for Model 2, the 100 multistart instances that were used required a total of 9361 iterations (19 s on the same computer). In the case of Fig. 7, the number of algorithm iterations was 9 for Model 1, corresponding to a processing time of 20 ms, and 8211 for Model 2, leading to a processing time of 32 s. In the case of Fig. 8, 11 iterations were required for Model 1 and 5717 for Model 2, the corresponding processing times being respectively 22 ms and 30 s.

V. Conclusion

This paper proposes a compact system able to gather EIS data of lithium-ion batteries and estimate the target parameters of interest by using suitable electrical models. The proposed system could potentially operate "*on-line*", that is while the battery is under operation, thanks to its compactness, low power consumption, and isolation from the battery under test. Compactness and *on-line* operation of the proposed system could enable the development of built-in battery management systems, fault warning solutions, and real-time diagnostics.

The proposed system is composed of a low-power vector impedance analyzer gathering raw impedance estimates, and a parameter estimator based on equivalent circuit models. The realized VIA prototype was shown to provide experimental EIS results that are consistent with those of a reference laboratory instrument. The proposed modeling approach was applied to the measured data, showing that the parameters of the equivalent circuit model can be estimated based on measurements obtained by the realized VIA, and that the model provides a good fit to experimental data. Therefore, the proposed compact system is suitable for battery management applications, and could further be integrated into a single chip. Potentially, the VIA can be embedded within the battery cell to realize an efficient and low-power measurement system able to on-line estimate state parameters of the target battery.

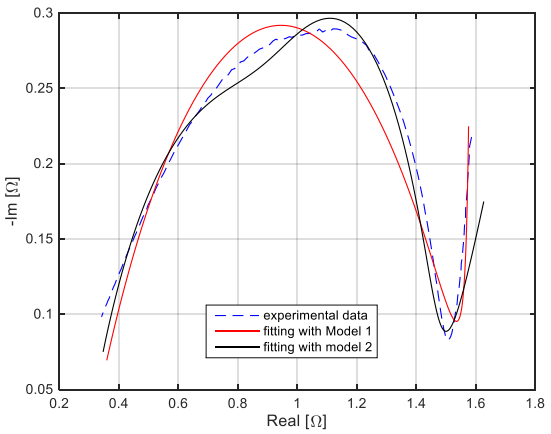

Fig. 7: Fitting results obtained using Model 1 and Model 2 on experimental data obtained by the reference impedance analyzer instrument Hioki IM3590 with a battery voltage of 4.1 V.

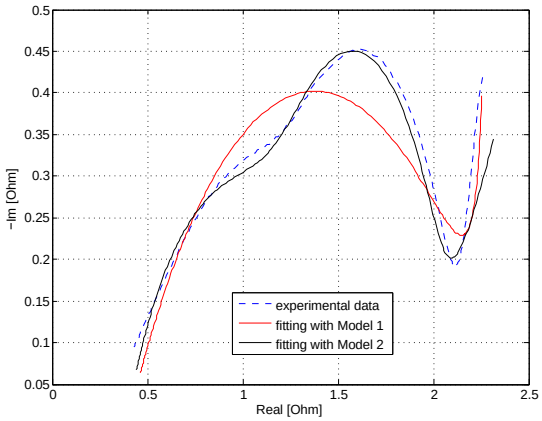

Fig. 8: Fitting results obtained using Models 1 and 2 on experimental data obtained by the reference impedance analyzer instrument Hioki IM3590 with a battery voltage of 3.5 V.

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