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Abstract

A combined experimental and simulation analysis of the degradation mechanisms induced by hot carriers in a silicon-based split-gate n-channel LDMOS transistor featuring an STI structure is reported. In this regime, electrons can gain sufficient kinetic energy necessary to create charged traps at the silicon/oxide interface, thus inducing device degradation and causing the shift of the electrical parameters of the device. In particular, the on-resistance degradation in linear regime has been experimentally characterized at different stress conditions and at room temperature. The hot-carrier degradation has been reproduced in the frame of TCAD simulations by using physical-based models aimed at reproducing the degradation kinetics. An investigation of the electron distribution function at different stress conditions and its dependence on the split-gate bias is carried out achieving a quantitative understanding of the role played by hot electrons in the hot-carrier degradation mechanisms of the device under test.

Keywords: Hot-carrier degradation, LDMOS, split-gate, TCAD, Reliability

1. Introduction

High-voltage lateral double diffused MOS transistors (LDMOS) are of great interest as they are needed for a variety of applications and can be easily integrated in smart power technologies. One of the key challenges in building this kind of devices is given by their reliability. The scaling of LDMOS devices inevitably leads to high-field issues, thus charge injection and hot carrier stress degradation mechanisms are identified to be the driving forces of device degradation. Moreover, nitrided gate oxides affect the long-term reliability [1] and, for high-voltage devices, the use of shallow-trench isolation (STIs) in the active region of the device would require an optimization accounting for degradation [2].

Previous studies on rugged LDMOS de-

vices with STI structures mainly focused on the device characterization and optimization [3], [4] and some works addressed recently the hot-carrier stress (HCS) analysis [2], [5], [6], [7]. The high electric fields lead to the generation of interface traps in the proximity of the silicon/oxide interface within the drift region. This causes the shift of the electrical parameters (e.g., the on-resistance, R_{ON}) limiting the device lifetime.

The implementation of gate field-plate is a strategy in the design of integrated high-voltage LDMOS in order to improve the time-zero breakdown and the HCS performance of the device. Several gate field-plate architectures have been proposed [8], [9], [10], [4] including grounded [9] and independently-biased [4] gate field-plate, each one addressing one or more figures of merit of the device. The introduction of a secondary gate has been proved to be a good technique [4], [5], [10] in order to reduce the HCS degradation effects and, being characterized by a lower gate capacity with respect to continuous gate architectures, it might be used to improve the dynamical behavior [9].

The primary function of the secondary gate is to help the depletion of the drift region of the device reducing the superficial electric field and decreasing the impact-ionization generation rate around the STI edge near the channel side during stress, while maintaining a high blocking voltage.

In this work, a TCAD investigation of the HCS degradation in n-channel split-gate LDMOS transistors designed for a nominal operating voltage of $40V$ is proposed. In particular, the on-resistance degradation in linear regime has been experimentally investigated for different split-gate biases and stress conditions and reproduced by means of TCAD simulations using degradation models [6] implemented into the framework of the TCAD tool. Consequently, a detailed analysis of the electron distribution functions at different stress biases and of the interface trap generation rates has been carried out aiming at obtaining a deeper insight on the role played by hot-electrons in the HCS degradation mechanisms of the the device under test.

2. Device structure and experiments

The n-channel split-gate transistor featuring a shallow trench isolation (STI) structure, schematically shown in Fig. 1, is realized in a 90 nm Bipolar-CMOS-DMOS (BCD) mixed technology by STMicroelectronics and designed for a nominal operating voltage of $40V$. The $12nm$-thick gate oxide is designed for operation at a maximum gate voltage $V_{GS} = 5V$. The poly-Si gap (the spacing between the two poly-Si gates) is the minimum spacing compatible with V_{GS}.

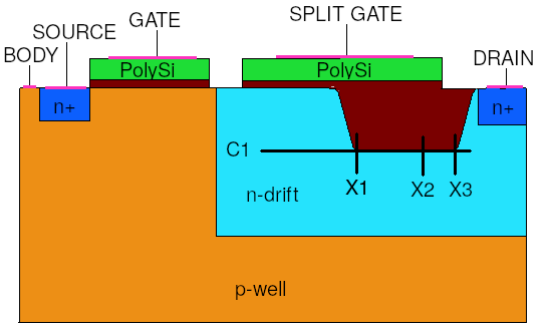

Figure 1: Schematic representation of the n-channel split-gate LDMOS transistor.

The analysis of hot-carrier effects on the stressed device has been carried out by monitoring the most relevant quantities in the linear regime, i.e., the on-resistance R_{ON} at $V_{GS} = 5V$ and $V_{DS} = 0.1V$ (defined as the ratio of the drain voltage to the linear drain

current at $V_{GS} = 5V$) and the threshold voltage. The drift of the on-resistance has been calculated as:

$$\Delta R_{ON} = \frac{R_{ON} - R_{ON,0}}{R_{ON,0}} \qquad (1)$$

where $R_{ON,0}$ is the on-resistance of the fresh device and R_{ON} is the on-resistance measured at stress time t, while the threshold voltage shift is $\Delta V_t = V_t - V_{t0}$.

3. Fresh characteristics analysis

First of all, 2D simulations of the device cross-sections have been carried out to fully investigate the behavior. The impurity concentration within the cross section has been inferred from process simulation results. Numerical simulations have been carried out using the drift-diffusion transport model with default parameters for the adopted physical models. The comparison of simulation results with measured turn-on characteristics in linear regime with different split-gate biases at room temperature is shown in Fig. 2. A quite good agreement has been found, even if slight differences might be observed at $V_{GS} \geq 3$. In such regime the series resistances given by the accumulation and drift regions take place as shown in [11], and they are expected to be significantly influenced when a split-gate voltage of $5V$ is applied.

As far as the TCAD modeling of LDMOS devices is concerned, it is very important to correctly predict the onset of avalanche breakdown in order to determine the worst-case degradation conditions. To this purpose, simulations have been performed on the n-channel split gate LDMOS transistor in order to determine whether the breakdown voltage was affected by the presence of an additional, independently-biased gate

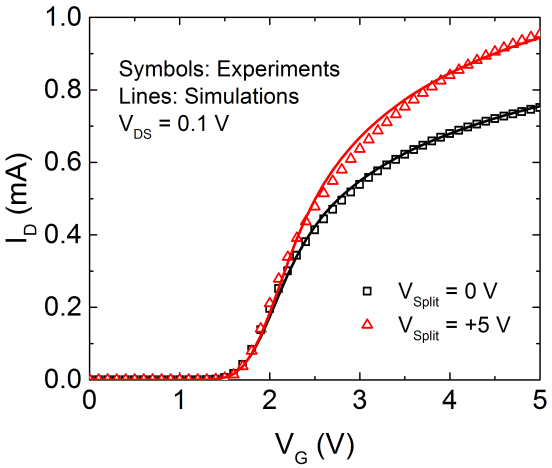

Figure 2: Turn-on characteristics at different split gate biases.

contact (the split-gate). Fig. 3 shows the output characteristics at zero gate voltage up to the breakdown at different split-gate biases. The very little dependence of the breakdown voltage on the split-gate voltage is fairly captured by simulations. The electric field represented in Fig. 4 confirms what the output characteristics shows: the maximum difference (which is reached at the drain side corner of the STI interface) between the electric fields in the case of the two split-gate biases considered is less than 10%.

Finally, in order to have a complete analysis of the effect of the split-gate on the performance of the device, the output characteristics up to the avalanche regime have been measured and simulated at different split-gate biases $V_{Split} = 0V$ and $V_{Split} = 5V$ as represented in Fig. 5 and Fig. 6. Simulations have been carried out using the drift-diffusion transport model coupled to the heat equation in order to take into account the self-heating effect, which arises at high gate voltages, as clearly shown by the experimental current level decrease at

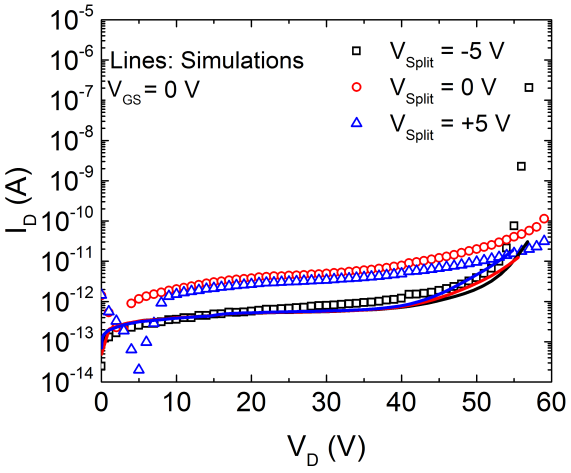

Figure 3: Output characteristics up to breakdown regime at zero gate voltage and different split gate biases.

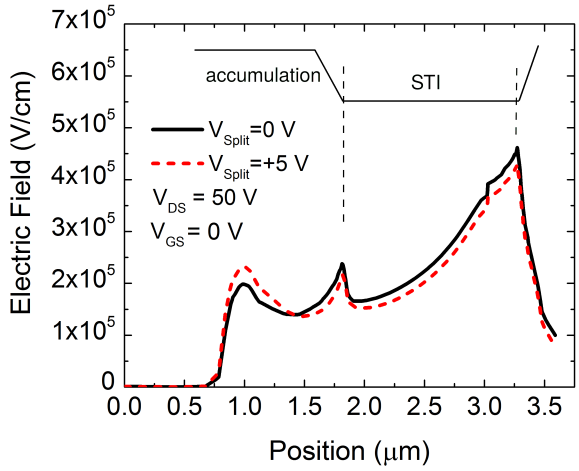

Figure 4: Electric field along the cutline C1 of Fig. 1 from the source contact (position 0) to the drain contact (position $3.5\mu m$) at different split-gate voltages, $V_{DS} = 50V$ and $V_{GS} = 0V$. A sketch of the relevant positions is represented on top.

$V_{GS} = 4V$ and $V_{GS} = 5V$ in Fig. 6.

At low gate biases, namely $V_{GS} = 2V$, the current levels at different split-gate biases are very similar, while at $V_{GS} \geq 3V$ the current level is greater at a high split-gate voltage ($V_{Split} = 5V$) (see Figs. 5 and 6). The latter feature can be ascribed to the onset of the quasi-saturation regime in the LDMOS devices, as explained in [12]. The channel region of the LDMOS reaches a full saturation condition at low V_{GS} due to the limited role played by the series resistances given by the accumulation and drift regions. In this case, the maximum current of the device would be limited by the channel saturation only, which is independent of the split-gate bias. At larger V_{GS}, the output current is partially limited by the accumulation and drift resistances, which also reduce the voltage drop at the channel-drain edge causing the quasi-saturation regime. As the accumulation resistance is modulated by the split-gate bias, a significant dependence of the output current level on the V_{Split} is observed.

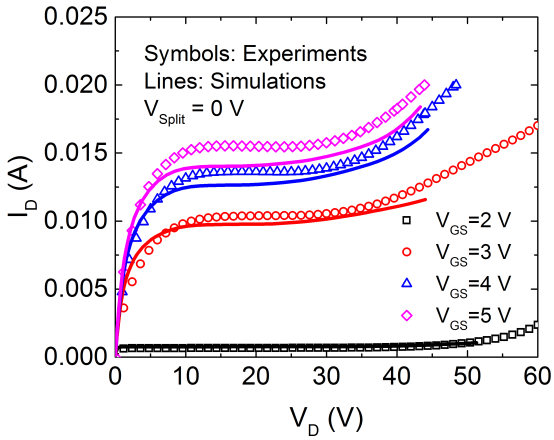

Figure 5: Output characteristics up to breakdown regime at zero splt-gate voltage and different gate biases.

4. TCAD analysis of hot-carrier stress degradation

Concerning HCS degradation, simulations have been performed using the Hot Carrier Stress degradation model implemented in the Synopsis TCAD tool [13] in order to reproduce the on-resistance shift as

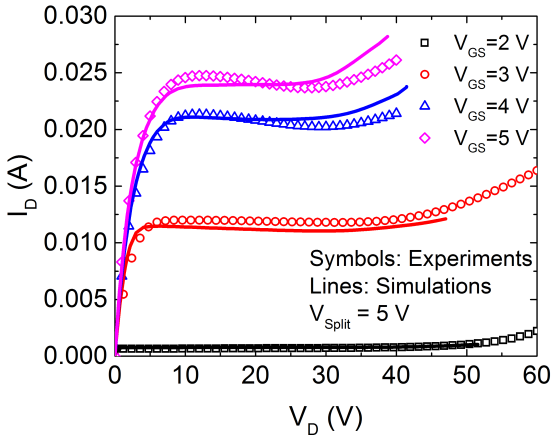

Figure 6: Output characteristics up to breakdown regime at $V_{Split} = 5V$ and different gate biases.

a function of the stress time by directly using the simulation tool.

By following [6], three different competing mechanisms such as single-particle (SP), multiple-particle (MP) and field-enhanced thermal interaction (TH) might contribute to the bond breaking at the Si/SiO_2 interface. Thermal-induced trap generation mechanism has been excluded from simulations, as self-heating effects are negligible at the stress conditions analyzed ($V_{GS} = 2.4V$), thus only the SP and MP mechanisms have been taken into account.

Concerning the shift of the relevant quantities in the linear regime, the threshold voltage shifts were measured and clearly showed that there is no significant degradation at the investigated stress conditions, therefore interface trap generation in the channel region has been assumed negligible. In Fig. 7, the on-resistance shifts extracted from simulations are represented against the experimental results at a drain-to-source voltage of $40V$ with a gate bias $V_{GS} = 2.4V$ corresponding to the body-current peak, as checked against TCAD simulations. A nice agreement has been observed at the two split-gate biases, with a slight enhancement of the degradation induced by the larger bias condition. The limited increase of degradation shows that $V_{Split} = 5V$ gives a better R_{ON} (see Fig. 2) and a controlled parameter shift. In Fig. 8, the on-resistance shift at $V_{Split} = 5V$ for two different drain-to-source biases is shown confirming the latter consideration even at larger V_{DS}.

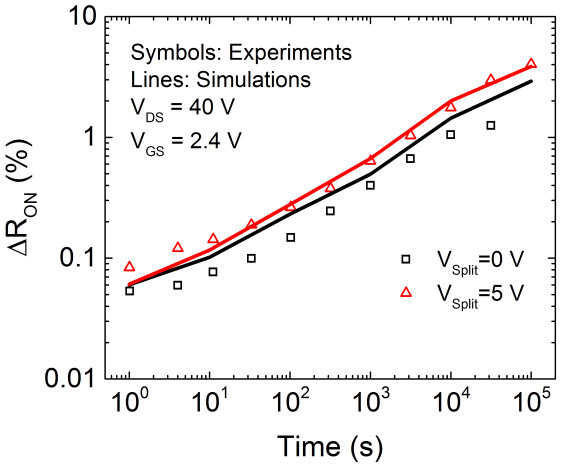

Figure 7: Measured and simulated on-resistance shift as a function of time at $V_{DS} = 40V$ and different V_{Split}.

In order to predict the degradation behavior of the device, so that a complete understanding can be achieved of the relevant physical mechanisms and of the regions of the Si/SiO_2 interface where the degradation takes place, a detailed study of the electron distribution function is necessary. Indeed, the analysis of the electron distribution function, determined from the solution of the Boltzmann transport equation (BTE) by means of a full band structure deterministic solver based on the spherical harmonic expansion (SHE) method implemented in the Synopsys tool taking into account the Coulomb, phonon and impact

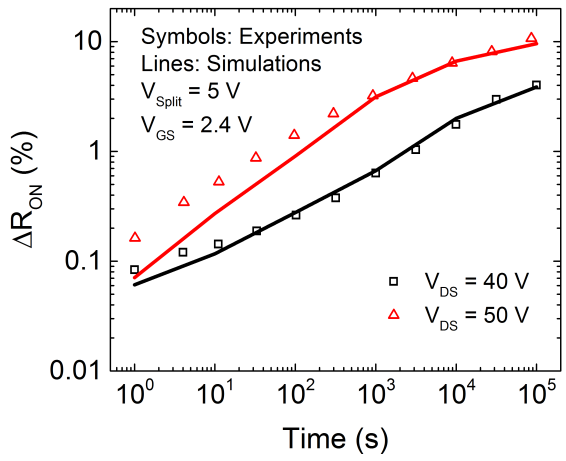

Figure 8: Measured and simulated on-resistance shift as a function of time at $V_{Split} = 5V$ and different V_{DS}.

ionization scattering mechanisms which can be used to numerically solve the BTE on the whole device domain [16], together with the on-resistance experimental curves, provides an excellent indication of which of the two different trap-generation mechanisms, i.e. single particle (SP) and multiple particle (MP), is dominant at the different points of the STI interface and at the stress conditions analyzed.

To this purpose, a detailed analysis of the effect of the split-gate voltage on the distribution function extracted at those points of the interface (reported in Fig. 9) where the interface trap generation is expected to be more critical has been carried out. In Fig. 10 and Fig. 11 the electron distribution functions at a drain-to-source voltage of $40V$ and $50V$, respectively, are reported.

The difference in ΔR_{ON} between $V_{Split} = 0V$ and $V_{Split} = 5V$ at a drain voltage of $40V$ has to be ascribed to the low-energy part of the distribution functions at the source-side corner of the STI and at the central part of the interface, as both the STI-drain side corner distribution and the

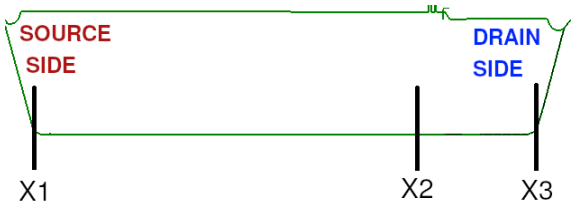

Figure 9: Points of the STI interface at which the distribution function has been extracted (see Fig. 1).

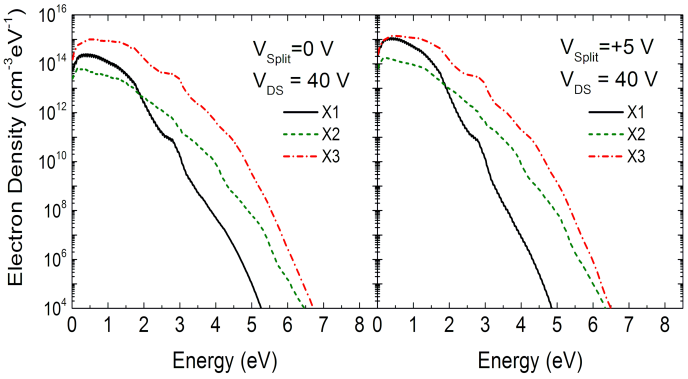

Figure 10: Electron distribution function at relevant interface points with $V_{DS} = 40V$ and $V_{Split} = 0V$ (left), $V_{Split} = 5V$ (right).

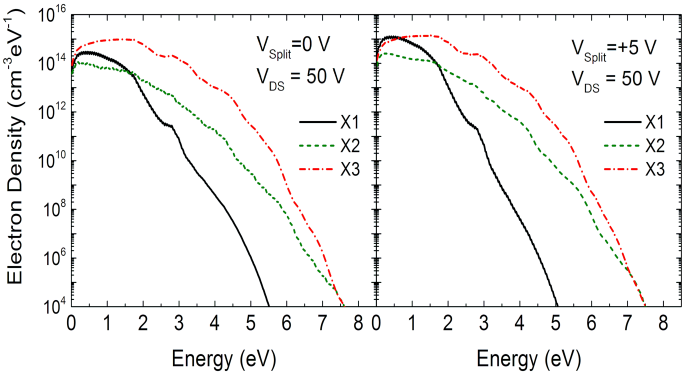

Figure 11: Electron distribution function at relevant interface points with $V_{DS} = 50V$ and $V_{Split} = 0V$ (left), $V_{Split} = 5V$ (right).

distribution tails of all the interfaces cannot lead to a significant on-resistance split. This means that at relatively low stress biases, the mechanism which dominates inter-

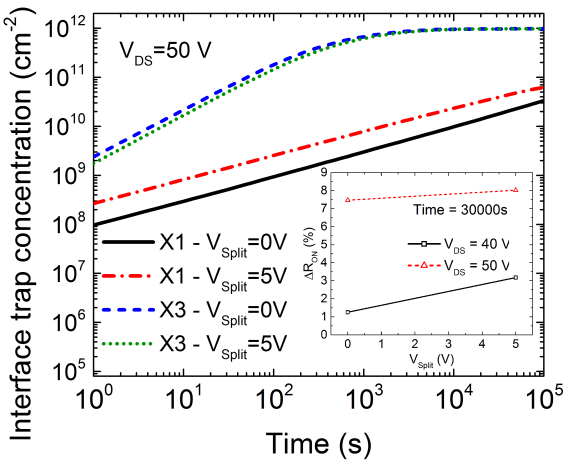

Figure 12: Interface trap concentration as a function of time at $V_{DS} = 50V$ and different V_{Split} extracted at two relevant points of the silicon/oxide interface. Inset: Experimental on-resistance shift versus the applied split-gate voltage at $V_{DS} = 40V$ and $V_{DS} = 50V$ and time of $30000s$.

face trap generation is the multiple particle process, as it is associated to the low-energy part of the distribution function, having an activation energy of a few hundreds of meV ($0.25eV$).

At higher drain voltages ($V_{DS} = 50V$), the dependence of the on-resistance shift on the split-gate voltage is negligible (as shown in the inset of Fig. 12). The total interface trap generated at the drain corner of the STI, which is independent on the applied split-gate bias, is significantly greater than the trap concentration at the source side corner of the STI. Thus the contribution of the latter to the on-resistance shift (which shows a clear dependence on V_{Split}) is negligible, indicating that the dominant process is the single particle trap generation. By comparing Figs. 10 and 11, the tail of the distribution is greater than at $V_{DS} = 40V$, while the low-energy distribution is substantially unaltered. This leads to a much greater single-particle related trap generation at the drain side corner of the STI interface.

5. Conclusion

The role played by hot-electrons in the Hot-Carrier degradation mechanisms of a split-gate n-type LDMOS device featuring an STI structure has been extensively investigated by using TCAD models available in Synopsys TCAD tool. The TCAD has been proved to be a useful tool in order to quantitatively describe the role played by two HC degradation competing mechanisms, such as SP and MP, and to gain a deeper insight on which are points of the silicon/oxide interface where the degradation effects are more critical. Moreover, the device has been proved having an electric field peak almost independent on the split-gate bias.

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