Full Understanding of Hot Electrons and Hot/Cold Holes in the Degradation of p-channel Power LDMOS Transistors

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Full Understanding of Hot Electrons and Hot/Cold Holes in the Degradation of p-channel Power LDMOS Transistors

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***Abstract*—Degradation induced by hot-carrier stress is a crucial issue for the reliability of power LDMOS transistors. This is even more true for the p-channel LDMOS in which, unlike the n-channel counterpart, both the majority and minority carriers play a fundamental role on the device reliability. An in-depth study of the microscopic mechanisms induced by hot-carrier stress in new generation BCD integrated p-channel LDMOS is presented in this paper. The effect of the competing electron and hole trapping mechanisms on the on-resistance drift has been thoroughly analyzed. To this purpose, TCAD simulations including the deterministic solution of Boltzmann transport equation and the microscopic degradation mechanisms have been used, to the best of our knowledge, for the first time. The insight gained into the degradation sources and dynamics will provide a relevant basis for future device optimization.**

***Index Terms*—Hot-carrier stress, on-resistance degradation, impact ionization, p-channel power LDMOS, reliability, TCAD modeling.**

I. Introduction

P-channel power MOSFETs, despite the higher on-resistance compared to n-channel counterparts with same area, due to the lower hole mobility, receive much interest from circuit designers because their adoption can simplify high-voltage IC while optimizing performance [1]. There are several switching power applications which can benefit from the use of p-channel MOSFETs, such as Low-Voltage Drives and non-isolated Point of Loads. The main advantage is the simplified gate driving technique for the high-side switch, possibly reducing the overall cost [2].

When a transistor is adopted in switching applications, it can operate in bias conditions which are detrimental for its reliability, i.e. high drain biases while it is turned-on. In this stress regime, named hot-carrier stress (HCS), carriers can gain sufficient kinetic energy creating interface defects and/or inducing charge injection, causing device performance degradation. This is even more relevant in LDMOS transistors due to the large applied drain voltage leading to the need of complex lateral structures. Recently, a few studies on HCS degradation in p-channel LDMOS have been carried out reporting experiments and static simulations [3-8]. Overall, all papers ascribe the degradation to electron interface/oxide trapping mechanisms occurring in the accumulation-drift region [3-8] along with the nearby sidewall of the shallow-trench isolation (STI) [6-8], causing a reduction of the on-resistance (R_{ON}) and, in some cases, gate failure [8]. In [6], electron interface trapping is localized also in the channel region, giving rise to the reduction of the threshold voltage (V_{TH}), whereas in [3], the channel region is interested by hole trapping inducing V_{TH} increase. Finally, in [4], the electron trapping due to acceptor-type defects in the accumulation region gets balanced by a slower donor-type trap generation in the same region, leading to saturation of the long-term ΔR_{ON}.

Even if the role of negative charge trapped at the interface was clearly established, however the source of these electrons and their spatial location are still unclear especially as far as their dependence on the drain stress bias is concerned. Moreover, the role of the energetic distribution of holes, leading to relatively cold particles contributing to degradation along with high-energy carriers, was never addressed. The latter issues require TCAD simulations aimed at reproducing the microscopic mechanisms and their dynamics. In this paper, we provide an experimental characterization of the combined roles of electron and hole trapping mechanisms with a detailed interpretation through physics-based TCAD simulations.

II. Results and Discussions

Fig. 1 shows a schematic view of a 48 V p-channel LDMOS integrated in a 90nm-BCD technology by STMicroelectronics. The device features a STI architecture with separated body and source contacts allowing direct access to impact ionization (II) related body current.

Figs. 2 and 3 show the measured and simulated transfer and body characteristics in saturation regime at different V_{DS}, respectively. Electro-thermal simulations were performed by Sentaurus TCAD [9]; contact thermal resistances have been

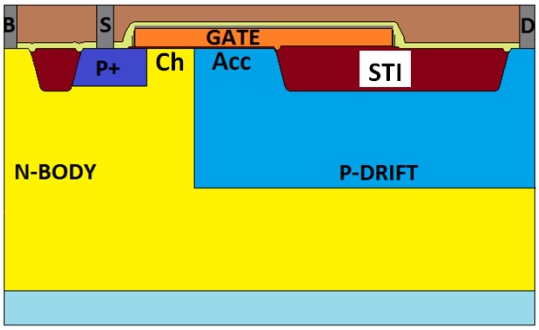

Fig. 1. Schematic view of the BCD integrated p-channel power LDMOS transistor.

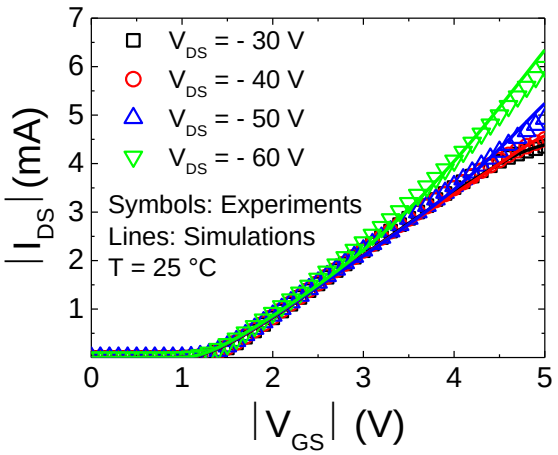

Fig. 2. Experimental (symbol) and simulated (line) I_{DS}-V_{GS} characteristics at different V_{DS}.

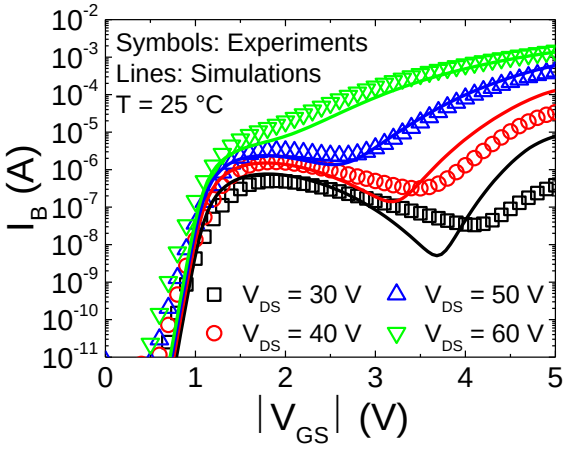

Fig. 3. Experimental (symbols) and simulated (lines) I_B-V_{GS} characteristics at different V_{DS}. Body current peak at $|V_{GS}| = 1.9$ V.

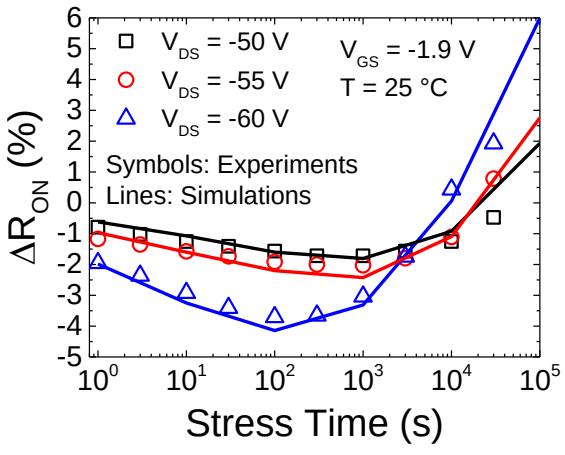

Fig. 4. Experimental (symbols) and simulated (lines) on-resistance degradation at the body-current peak condition (see Fig. 3).

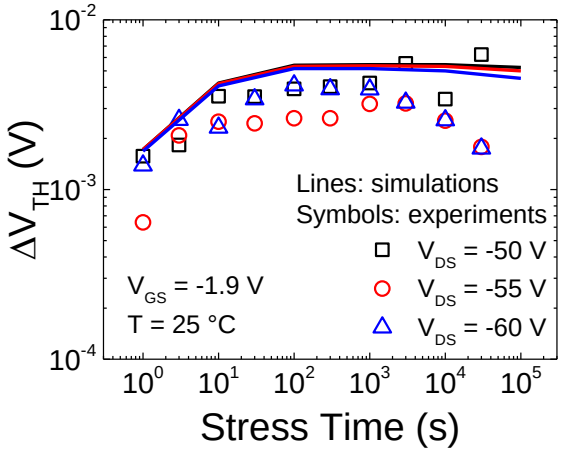

Fig. 5. Experimental (symbols) and simulated (lines) threshold voltage degradation at the body-current peak condition (see Fig. 3).

tuned against experiments to obtain accurate matching. Unlike the n-channel counterpart, in which the II is purely dominated by the majority carriers, in p-channel devices minority ones play a fundamental role as well. To separate the two effects, the II coefficients for electrons (EII) and holes (HII) of the UniBo2 TCAD model [9] have been calibrated on n-channel LDMOS transistors [10] and ad-hoc p-channel 5V-MOSFETs [11], respectively. As shown in Fig. 3, the body current (I_B) features a peak at V_{GS} values ($V_{GS} = -1.9$ V) close to the threshold voltage, with carriers experiencing high electric field in the region located between the channel and the STI sidewall (Fig. 1), representing the worst-case scenario for hot-carrier degradation as it is periodically experienced during the switching processes in a real switching power application.

Fig. 4 shows the measured and simulated R_{ON} degradation during HCS in the I_B-peak condition as a function of V_{DS} at room temperature. Our physics-based HCS degradation model [9, 12] has been used to determine the R_{ON} drift. It takes into account both contributions due to hot-carriers (single particle process, SP) and colder-carriers (multiple particle process, MP). To this purpose, the carrier energy distributions (CED) have been obtained by solving the Boltzmann Transport Equation (BTE) through the spherical harmonic expansion (SHE) method [9]. By observing Fig. 4, two stages can be identified: a short-term negative R_{ON} shift followed by long-term positive one. A negative ΔR_{ON} indicates an improvement of the device conductance, which is ascribed to negative-charge trapping, while the positive ΔR_{ON} is due to a conductance degradation induced by positive-charge trapping. The higher the V_{DS}, the higher the negative and positive ΔR_{ON}, due to faster acceptor-type (stage 1) and donor-type (stage 2) trap generation activated by the increased lateral electric field. On the contrary, threshold voltage (V_{TH}) does not show appreciable degradation (Fig. 5), suggesting that trapping mechanisms affect only the drift region, i.e., accumulation and STI interfaces, without significantly affecting the channel (Fig. 1).

Fig. 6 shows the interface traps created and filled with electrons and holes during the stress transient along the Si/SiO_2 interface of the drift region, at the positions defined in the inset, for the two limit stress conditions analyzed in Fig. 4, i.e., V_{DS} = -50 V and -60V. Trapped charges occurring at the drain-side edge of the STI are not reported because they do not affect R_{ON} due to the very high doping concentration in the

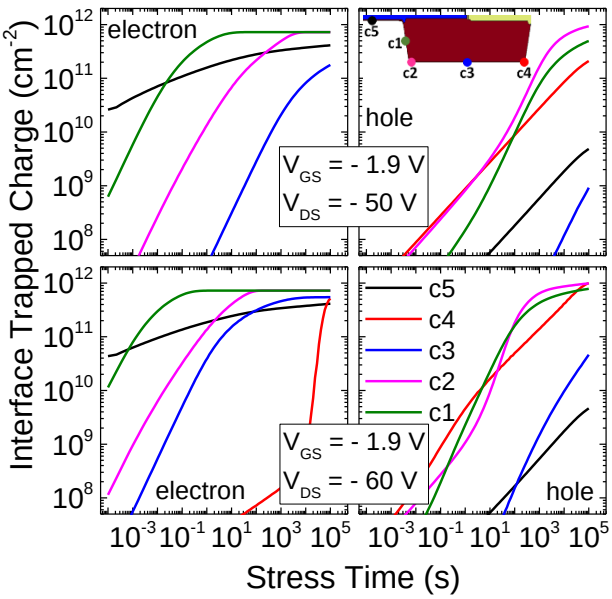

Fig. 6. Interface traps created and filled with electron (left) and hole (right) during the stress time along the Si/SiO_2 interface at the positions defined in the inset (c4 is the closest position to drain).

nearby semiconductor region close to the drain contact. A significant electron trapping is observed at the accumulation region ('c5') and at the STI edge ('c1'), extending up to part of the STI bottom ('c2' and 'c3') for V_{DS} = -60 V. Hole trapping mechanisms are dominant at the source-side corner of the STI ('c2'), with a significant contribution of the trapped hole at the nearby STI sidewall ('c1'), as expected, along with a relevant trap density at the drain-side STI corner ('c4'). The above results are consistent with the CED curves shown in

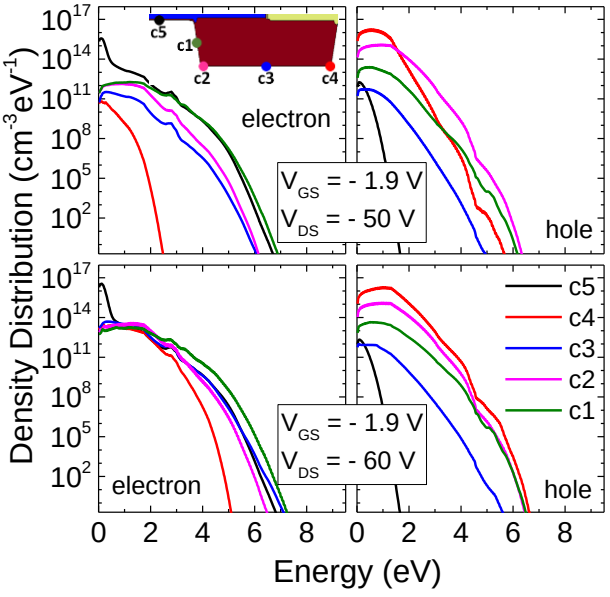

Fig. 7. Electron and hole distribution function (CED) at the two limit stress conditions, evaluated along the Si/SiO_2 interface at the positions defined in the inset (c4 is the closest position to drain).

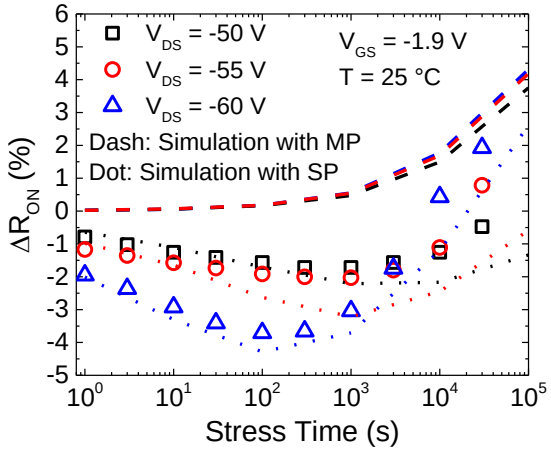

Fig. 8. Experimental (symbols) and simulated on-resistance degradation at the body-current peak condition by separately taking into account only the multiple particle (dash lines) or the single particle (dot lines).

Fig. 7 at the same points along the interface.

It is worth observing that the hole distribution functions at the two STI corners ('c2') and ('c4') in Fig. 7, in addition to a significantly extended high-energy tail, are characterized by a high hole density with energy lower than ~3 eV (2-3 orders of magnitude larger than the electrons), giving rise to an additional source of cold carriers relevant to the MP degradation mechanism causing further positive R_{ON} drift. This is confirmed by Fig. 8, where the R_{ON} degradation has been simulated by separately considering the contributions of the single (dot lines) and multiple (dash lines) particles for both electrons and holes. In particular, by observing the role of the cold carriers (MP), a significant contribution to degradation is found in the long-term positive ΔR_{ON}. On the contrary, by selecting only the contribution of the hot carriers (SP), a short-term negative R_{ON} shift followed by long-term positive one is obtained. As a result, it can be concluded that the short-term negative ΔR_{ON} is purely caused by hot electrons, whereas the positive one is triggered by the combined effect of hot and cold holes. The interface trap generation due to cold holes (multiple carriers having limited energy) occurs at the two STI corners and represents a substantial difference compared to n-channel counterpart, where it has been largely demonstrated that for relatively low V_{GS} and high V_{DS} the device degradation is purely ascribed to hot carries [10, 13].

Focusing on the trapped-electron spatial distribution, the considerable trapping observed in the accumulation region ('c5' in Fig. 6) can only partially explain the experimental negative ΔR_{ON} (ad-hoc TCAD simulations were carried out to monitor this aspect). In our case, contrary to [3-5] where the negative ΔR_{ON} is ascribed to accumulation region, we clearly identified as dominant the role played by electrons trapping along the source-side sidewall of the STI ('c1'), where, especially at high V_{DS}, the electrons feature the highest CED-tail (Fig. 7). Since hot electrons originate from hole impact ionization, the HII generation plot is reported in Fig. 9 for V_{DS} = -50 V and -60 V. Two HII peaks are observed, located at the left (source-side) and right (drain-side) STI corners,

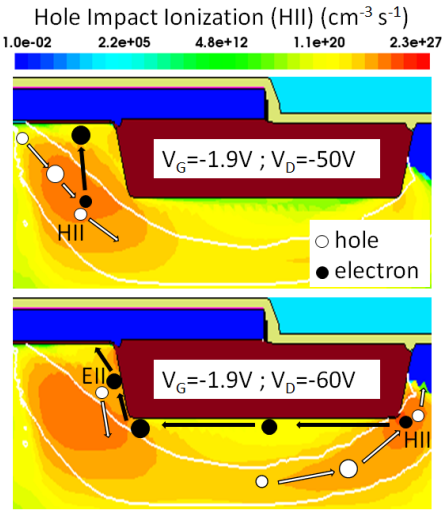

Fig. 9. Hole impact ionization (HII) rate at the body-current peak ($|V_{GS}|$ = 1.9 V) for the two limit stress conditions. Electrons responsible for the negative ΔR_{ON} are mainly generated by the left and right HII peak at low and high V_{DS}, respectively.

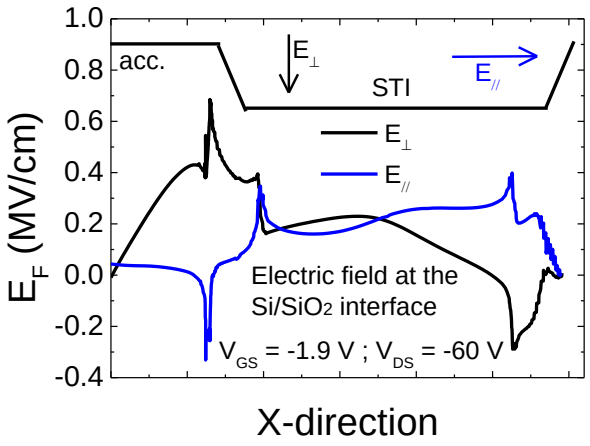

Fig. 10. Normal (black) and longitudinal (blue) components of the electric field along the Si/SiO_2 interface.

significantly modulated by V_{DS}. At low V_{DS}, electrons generated in the left HII peak are mainly drifted towards the accumulation interface by the vertical electric field [3-8], while the second HII peak at the drain side is negligible. At high V_{DS}, a relevant contribution of electrons comes from the HII peak at the right corner of the STI. The generated electrons are accelerated by the longitudinal electric field (Fig. 10) from right to left along the STI, hence acquiring significant kinetic energy in reaching the left STI corner. After reaching the left corner, they are forced against the STI sidewall by the normal electric-field component (Fig.10).

The proposed picture is further supported by Fig. 11, where the electron current density and the conduction band energy along a cutline under the STI are reported for the two limit stress conditions. In particular, the electron current density in Fig. 11a shows a peak at position 'c4', i.e., the position of the second HII peak in Fig. 9, and increases moving towards positions 'c3' and 'c2' along the STI path by collecting further II-generated electrons. This is confirmed by

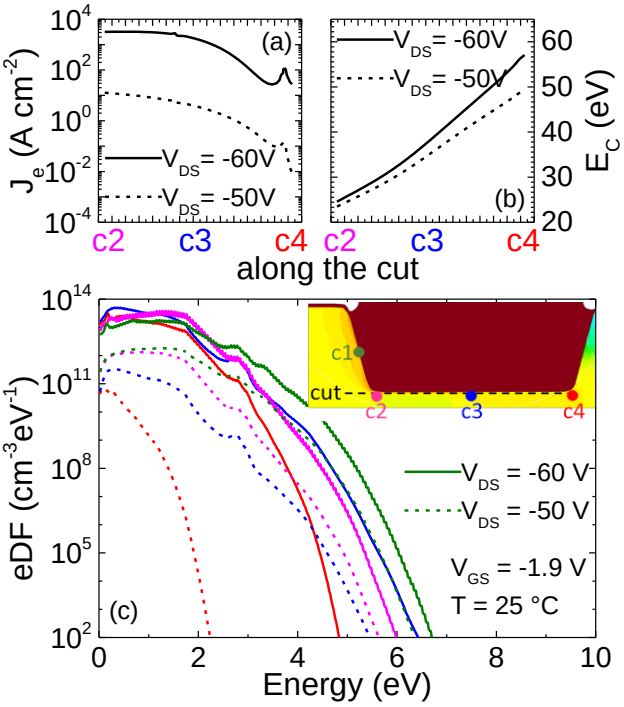

Fig. 11. (a) Electron current density and (b) conduction band energy evaluated along the cut shown in the inset. (c) Electron distribution function evaluated at the positions c1, c2, c3 and c4.

Fig. 12, where the plots of the EII generation are reported for both V_{DS} biases. It is worth noting that at high V_{DS} the electron current density is about 500 times larger than at low V_{DS} (Fig. 11a) leading to a significant contribution to hot electrons. The electron energetic increase is sustained by the favorable energy potential as shown in Fig. 11b. The progressive heating of the electrons along the path is demonstrated by their CED curves reported in Fig. 11c: the tail of the distribution function increase from 'c4' to 'c2' due to the longitudinal electric field. Then, as already anticipated above, they are further accelerated by the vertical electric field against the left sidewall of the STI as shown by the CED in 'c1'. Eventually, hot electrons can create traps by a collision with the electrically inactive bonds at the Si/SiO_2 interface, and/or create additional electron-hole pairs by electron impact

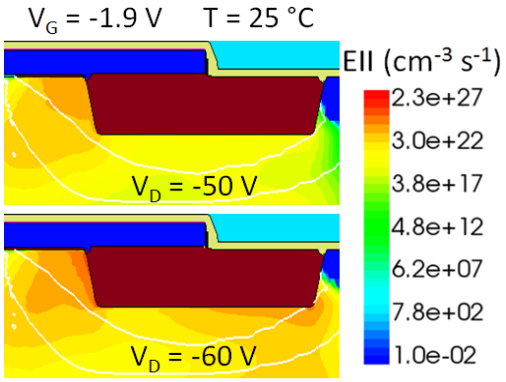

Fig. 12. Electron impact ionization (EII) rate evaluated at the body current peak ($|V_{GS}|$ = 1.9 V) with different V_{DS}.

ionization as shown in Fig. 12.

III. CONCLUSIONS

In this paper, we investigated the physical mechanisms of the hot-carrier stress degradation in p-channel power LDMOS transistors with STI architecture. The R_{ON} degradation has been simulated by advanced TCAD, obtaining an accurate matching with the experiments and highlighting the presence of two competing interface trapping mechanisms. The generated acceptor-type traps causing the fast negative ΔR_{ON} are mainly ascribed to hot electrons generated by hole impact ionization nearby the STI corners. In particular, by increasing V_{DS}, electrons generated at the drain-side corner of the STI are accelerated toward the source-side one gaining kinetic energy and creating interface defects filled with electrons along the source-side edge of the STI, hence inducing a larger negative ΔR_{ON}. Electrons trapping occurs also in the accumulation region as suggested in [3-5] but the associated effect is not sufficient to justify the measured negative ΔR_{ON}, especially at high V_{DS}. In addition to this, a slower generation of donor-type interface traps leads to the long-term positive R_{ON} shift, which is ascribed to combined effect of hot and cold holes coming from the channel and impinging both corners and source-side sidewall of the STI.

ACKNOWLEDGMENT

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