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Role of the AlGaN barrier on the long-term gate reliability of power HEMTs with p-GaN gate

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Abstract – Forward gate constant voltage stress (CVS) has been performed on GaN-on-Si (200 mm) HEMTs with p-GaN gate, controlled by a Schottky metal-retracted/p-GaN junction, processed by imec with different gate process splits. In particular, the adoption of devices with a different magnesium (Mg) concentration in the p-GaN layer, AlGaN barrier thickness and AlGaN aluminium percentage (Al%), allowed us to identify the degradation of the AlGaN barrier as responsible for time-dependent gate breakdown at room temperature. Lowering the Al% of the barrier and the Mg concentration of the p-GaN layer leads to a longer gate lifetime, while an optimum AlGaN barrier thickness is identified at given Al%.

1. Introduction

In the last years, several degradation mechanisms affecting the p-GaN gate reliability of GaN-on-Si power HEMTs have been recognized [1-19]. In particular, such mechanisms, occurring when a positive bias is applied on the gate, may mainly cause threshold voltage instability [3-14] and/or time-dependent gate breakdown [15-19].

The threshold voltage instability has been largely ascribed to the presence of two competing mechanisms occurring in the p-GaN/AlGaN stack, i.e. hole and electron trapping, causing negative and positive V_{TH} shift, respectively [3-9]. The prevalence of one over the other may depend on the gate bias and temperature [3], the kind of technology [11], the stress/characterization time [12]. Overall, hole injection from gate metal and/or impact ionization in the high-field depleted Schottky junction have been identified as root cause of such phenomena causing V_{TH} instability. Process optimizations such as reduction of the active Magnesium doping concentration in the p-GaN layer near the gate metal [11], reduction of the aluminium content in the AlGaN barrier [3], and optimization of the etching and passivation of the p-GaN sidewalls [10] have been proposed to limit the negative and positive V_{TH} shift under forward gate stress.

A similar effort has been made to investigate the time-dependent gate breakdown (TDGB) under DC and pulsed forward bias stress [15-19]. In [16, 17], a correlation between TDGB and magnesium (Mg) concentration in the p-GaN layer has been proposed, i.e. the lower the Mg concentration, the longer the gate time-to-failure (TTF). Recently, it has been reported that a lateral-etching of the gate metal interlayer on top of the p-GaN can significantly improve the gate lifetime because it suppresses the leakage current occurring at the gate edges for relatively high gate voltages and temperatures [19], eventually causing a premature time-dependent gate breakdown. Moreover, on the same optimized samples, we have demonstrated that TDGB occurs in different regions depending on the temperature, i.e. active gate area and isolation region at low (< 80°C) and high (> 80°C) temperatures, respectively [20].

In this paper, we report a degradation analysis aimed at understanding the root cause for TDGB at low temperatures, i.e. when the failure occurs in the active gate area.

2. Device Structure

Enhancement-mode GaN-HEMTs with a p-type gate, fabricated at *imec* on 200 mm Si-substrates using an Au-free CMOS-compatible process flow [21] are considered in this study. A schematic cross section is shown in Fig. 1. The top layers of the reference device (Process C, see Table I), grown on a super lattice buffer, consist of a 1 μm carbon-doped GaN back barrier, a 400 nm-thick GaN channel, a 12.5 nm-thick AlGaN barrier with 25 % of aluminium concentration, a 80 nm-thick p-type GaN layer doped with a magnesium concentration of $2.7 \cdot 10^{19}$ cm^{-3}, and a 30 nm-thick TiN metal. Devices feature the gate metal retraction (GMR) process step, which consists in removing ~ 130 nm of TiN gate metal interlayer from the edges of the gate in order to avoid the breakage at the gate sidewalls [19, 20]. The access regions were passivated by a dielectric stack containing Al_2O_3 and SiO_2. More details on the process steps can be found in [21].

The devices under test (DUT) feature a 100 μm-wide symmetric structure, realized for gate reliability tests, with gate and gate-source/drain spacing length of 1.5 μm and 0.85 μm, respectively. Finally, different process variants in terms of p-GaN and AlGaN barrier layers have been adopted to identify the root causes responsible for time-dependent gate breakdown at

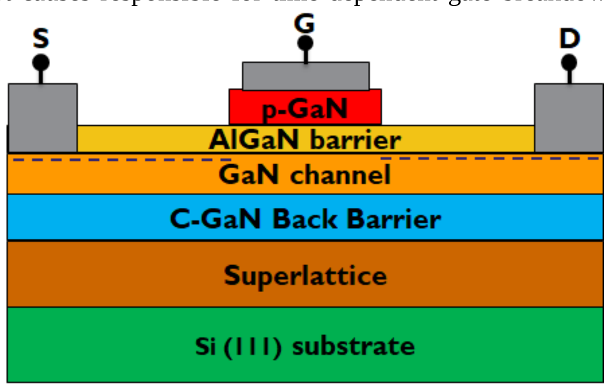

Fig. 1. Schematic of a GaN-on-Si power HEMT with p-type gate, controlled by a Schottky metal-retracted/p-GaN junction (not in scale).

TABLE I: p-GaN HEMTs with different gate process splits.

Process	Mg (cm-3)	pGaN (nm)	Al (%)	AlGaN (nm)
A	Same as C	80	Lower	12.5
B	Slightly lower	80	Same as A	12.5
C (Ref.)	$2.7 \cdot 10^{19}$	80	25	12.5

room temperature.

3. Results and discussion

Forward gate CVS tests have been performed on devices with different gate process splits, reported in Table I, in order to localize the physical damage causing time-dependent gate breakdown. Unlike the classic TDGB test, the stress was periodically interrupted to monitor the threshold voltage V_{TH} (Fig. 2) and the gate leakage (I_G) at different gate voltages (V_G) in order to probe different physical regions. At V_G = - 6 V the gate leakage ($I_{G(REV)}$) is dominated by the reverse-biased p-GaN/AlGaN/GaN junction, hence by the AlGaN barrier (Fig. 3a), whereas at V_G = 6 V, $I_{G(FW)}$ is ascribed to the reverse-biased metal/pGaN Schottky junction (Fig. 3b). A detailed analytical model for the p-GaN gate leakage and voltage distribution has been reported in [16]. A significant drift is observed in Fig. 2a and 3a, suggesting a degradation of the AlGaN barrier, whereas the Schottky junction is almost unaffected (Fig. 3b).

It is worth noting that the gate leakage at V_G = -6 V (Fig. 3a) is mainly dominated by an edge/perimeter component, since, in reverse mode, the channel is completely depleted but the two-dimensional electron gas (2DEG) is still present in the access region, giving rise to electric field peaks at the gate edges (not shown). However, since the stress was performed in forward gate regime (V_G = 9.5 V) and given the observed V_{TH} shift (Fig.

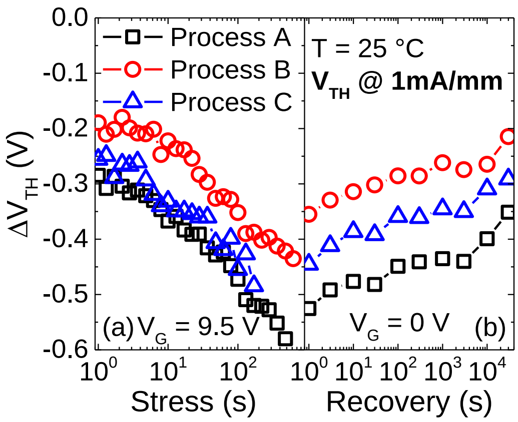

Fig. 2. V_{TH} shift during (a) stress and (b) recovery of devices with different Mg concentration and Al%. Data represent the mean value of 6 analyzed devices. ΔV_{TH} is mainly due to trapping and de-trapping of holes in pre-existing defects [3]. The larger hole trapping in process A and C is explained by the higher Mg-dose, inducing a higher generation of holes by impact ionization in the depleted Schottky junction, then accelerated towards the AlGaN where they get trapped.

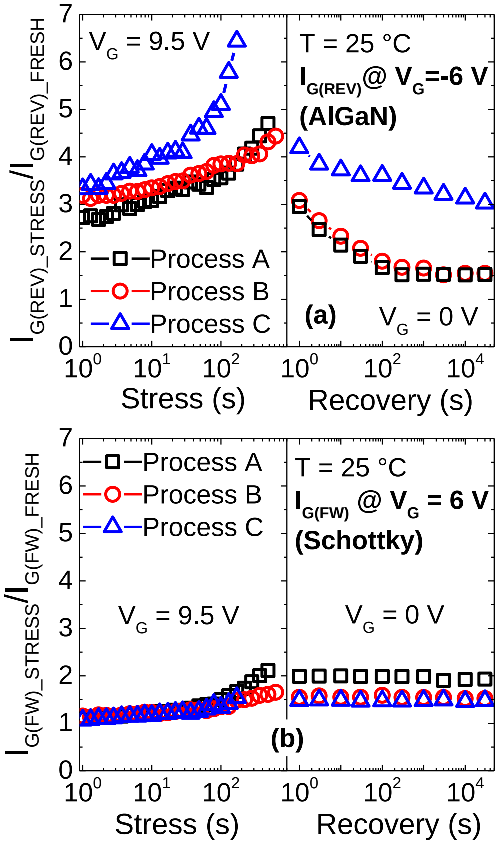

Fig. 3. Gate leakage drift during stress (V_G = 9.5 V) and recovery (V_G = 0 V) measured during characterization phase at (a) V_G = - 6 V ($I_{G(REV)}$) hence dominated by the AlGaN barrier, (b) V_G = 6 V ($I_{G(FW)}$) hence dominated by the Schottky junction. The large and negligible I_G drift in (a) and (b), respectively, proves that AlGaN barrier is the responsible layer for TDGB.

2a), it is suggested that the AlGaN barrier layer is degrading along the entire area below the gate, including the perimeter. The inference is strengthened by the area-dependent TDGB reported in [20] and by Fig. 4, where the gate leakage current of Process

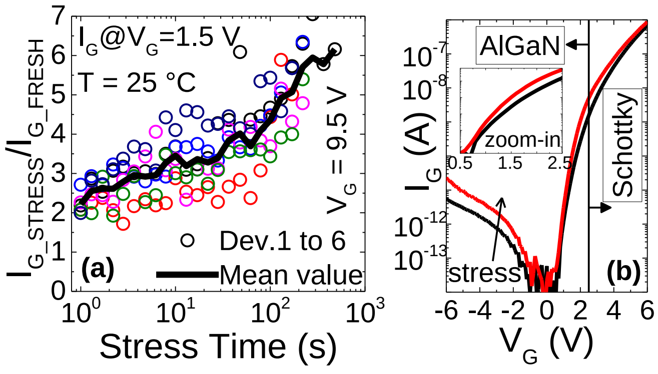

Fig. 4. (a) Gate leakage drift during stress (V_G = 9.5 V) measured on Process A during characterization phase at V_G = 1.5 V, hence still dominated by the AlGaN barrier. The line represent the mean value of the 6 analyzed devices (circles). (b) Representative gate leakage characteristics before and after the stress. A marked I_G degradation is only observed in the region dominated by the AlGaN barrier, i.e. < ~2.5 V.

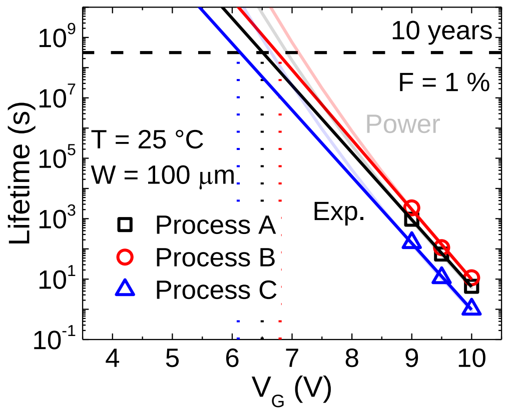

Fig. 5. Lifetime comparison of devices with different Mg concentrations and Al%. Failure criterion: 1 % of failure at 25 °C extrapolated from Weibull plots (Fig. 4) with a slope, independent of V_G, of ~ 2.2, 2.3 and 2.7 for Process A, B and C, respectively.

A is measured also under forward mode but in a bias regime still dominated by the AlGaN barrier, i.e. V_G = 1.5 V. As shown in Fig. 4a, the AlGaN degradation is still visible, even slightly larger than that monitored under reverse mode (Process A, Fig. 3a), confirming the degradation along the entire area.

The AlGaN degradation is due to both pre-existing (probably Mg-related [3]) and newly created defects. The presence of the pre-existing defects is proven by the recoverable component shown in Fig. 2b and 3a. The creation of new defects is caused by hot-holes generated by impact ionization (ii) in the high-field Schottky depletion region and accelerated towards the AlGaN barrier [3]. This is supported by Fig. 5, where a lifetime comparison between Process A, B and C, evaluated at 25 °C and considering 1 % as failure criterion, is reported. It is worth noting that a Weibull distribution has been adopted to fit the TDGB data at different gate biases, although, as shown in Fig. 6, both Weibull and LogNormal [1] distributions can accurately fit the data. However, the choice of the Weibull has been dictated by a more conservative approach, i.e. the gate time-to-failure (or TDGB) extrapolated at F = 1% is shorter in the case of Weibull (Fig. 6). By observing Fig. 5, an improved gate robustness is obtained (higher V_G extrapolated at 10 year lifetime) by reducing the Mg concentration (Process B), since the impact ionization and hence the creation of defects in the AlGaN barrier is reduced as well. Note that an exponential fitting is usually preferred than a power one for the lifetime extrapolation, since it is more conservative, providing a lower extrapolated V_{G_MAX} at 10 year's lifetime. However, as shown in Fig. 5, the extrapolation law does not affect the reliability comparison between devices with different gate processes, therefore not relevant for such analysis.

Distribution	Goodness of Fit	Statistics	P-value	Level (1%)
Lognormal	K-S mod. test	0.08505	>0.15	Can't reject
	A-D test	0.23076	0.78026	Can't reject
Weibull	K-S mod. test	0.10981	>0.1	Can't reject
	A-D test	0.29924	>=0.25	Can't reject

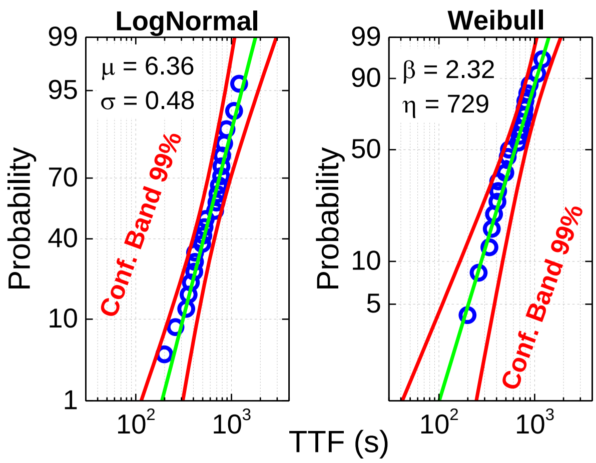

Fig. 6. LogNormal and Weibull fitting of the gate time-to-failure (TTF or TDGB) at V_G = 9.5 V and T = 25 °C. Data can be accurately fitted with both Weibull and LogNormal distributions [1].

Moreover, the rate of defect creation (structural) in the barrier increases when the crystalline lattice of the AlGaN is subjected to larger mechanical stress [3], i.e. when higher Al% is adopted (Process C). As a result, the significantly larger $\Delta I_{G(REV)}$ ascribed to AlGaN barrier (Fig. 3a), the lack of Schottky junction degradation (Fig. 3b) and the lower extrapolated maximum V_G for higher Al% (Fig. 5) identify the AlGaN barrier as responsible for the time-dependent gate breakdown.

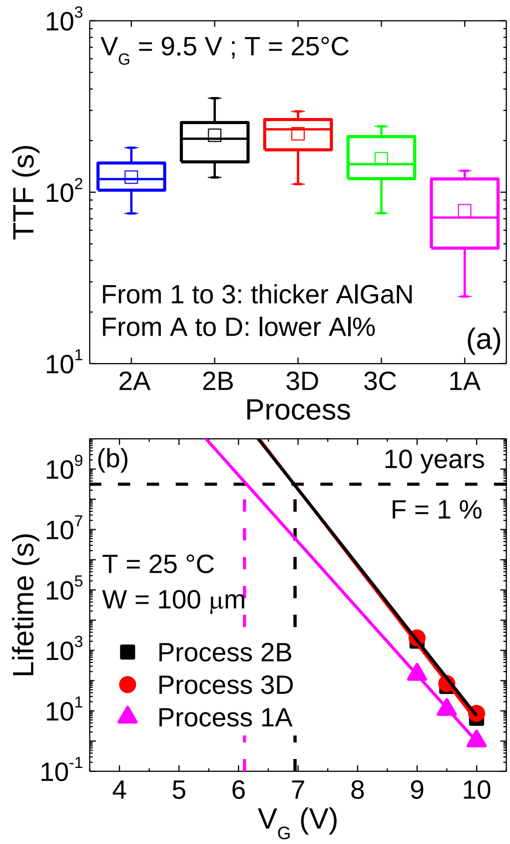

Fig. 7. (a) Time-to-failure at V_G = 9.5 V of devices featuring different AlGaN barrier thicknesses and Al%. Each box plot is the result of 24 devices stressed up to gate failure (see Fig. 6a). (b) Lifetime comparison between processes featuring longest and shortest TTF (a).

As soon as a percolation path is created in the AlGaN barrier, the voltage drop across the metal/p-GaN Schottky junction suddenly increases, causing also its breakdown, as confirmed by the post-failure gate leakage increase in the bias regime dominated by the Schottky junction, i.e. $V_G > 2$ V [20].

Once the role of the AlGaN barrier on the TDGB was established, additional experiments have been performed to understand the role of the AlGaN thickness. Five splits featuring identical process flow except for the AlGaN thickness and Al% have been adopted (Fig. 7a). In particular, note that Process 1A is the same as Process C (reference). Moreover, moving from 1 to 3 means thicker AlGaN, whereas from A to D implies lower Al%.

Fig. 7a shows the time-to-failure (TTF) extrapolated from TDGB tests reported in Fig. 8a. TTF is the time when an uncontrolled increase in the gate current (breakdown) occurs. In particular, observing Fig. 7a and comparing processes with same AlGaN thickness (2A and B, or 3C and D), the role of the Al% is confirmed, i.e. the lower Al%, the longer TTF. In the case of AlGaN thickness, by comparing processes 1A and 2A, the thicker the AlGaN the longer the TTF; however, a further thickness increase (e.g. from 2B to 3C/3D) does not produce a further TTF improvement despite the lower Al% in 3C and 3D compared to 2B. These results can be explained by the combination of two mechanisms:

1) a too thin AlGaN requires the creation of only a few defects to form a percolation path (failure), hence a thicker AlGaN improves TTF (1A and 2A);

2) a thicker AlGaN implies a lower V_{TH} as shown in Fig. 8b, which causes a higher gate leakage during the stress (Fig. 8a) due to larger voltage drop on the Schottky junction at given gate voltage (V_G). Consequently, as reported in [3, 19, 20], the increase of gate leakage shortens the TTF.

Overall, a trade-off between mechanism (1) and (2) guides towards an optimum thickness at a given Al% (e.g. 2B and 3D).

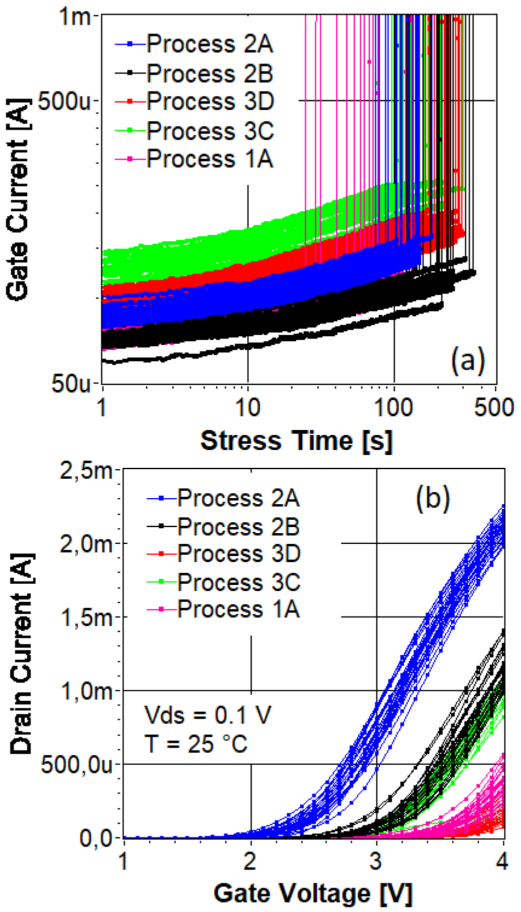

Fig. 8. (a) TDGB stress at $V_G = 9.5$ V and T = 25 °C. (b) Fresh transfer characteristics of DUTs with different AlGaN configurations.

4. Conclusions

Long-term gate reliability has been experimentally investigated on power HEMTs featuring a p-GaN gate with different process splits. The AlGaN barrier has been identified as the responsible layer for TDGB at room temperature. In particular, on one hand, lower Al% leads to longer TDGB because of two benefits: 1) the AlGaN barrier is structurally more robust due to lower mechanical stress; 2) the gate leakage is lower due to higher V_{TH}. On the other hand, an optimum AlGaN barrier thickness at given Al% exists with respect to TDGB, since: 1) too thin a layer can speed up the build-up of a percolation path, reducing the TDGB; 2) too thick a barrier increases the gate leakage because of lower V_{TH}. Overall, by combining gate reliability and V_{TH}, the optimum AlGaN barrier is attained (2B).

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