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Implementation of a DC/DC Converter with Stepwise Charge and Improved Battery Lifetime

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***Abstract* — An integrated buck-boost DC/DC converter for interfacing battery sources to capacitive loads such as supercapacitors is presented. The converter features a current regulation circuit on the source side, which applies a predefined constant DC current to the battery source, thus preventing the application of sharp current pulses generally associated with conventional DC/DC switching activity and resulting in long-term battery degradation. In fact, flat current shaping positively affects lifetime of battery sources. A specific digital control technique is proposed, which guarantees low energy losses during conversion by implementing a stepwise pseudo-adiabatic energy transfer that limits the maximum current inside the circuit and reduces the damping effect on current oscillation due to resistive paths.**

Keywords— DC/DC converter, stepwise charge, low-power, battery reliability, digital control, current shaping

I. Introduction

An increasing number of portable devices in consolidated markets, e.g. smart-phones and entertainment applications, and innovative sectors, like the Internet-of-Things, has opened new research perspectives in the field of power conversion, especially related to reliability and efficiency issues of battery sources. On one hand, the existence of a great variety of batteries associated with different operating voltages requires the development of buck-boost solutions capable of matching the voltage demands of supplied circuitry. On the other hand, advanced studies show how highly impulsive current profiles applied to common Li-Ion battery can dramatically reduce battery lifetime [1]. Conversely, passive storage sources such as capacitors or supercapacitors can reliably provide such peak currents without suffering from degradation. Consequently, developing dedicated solutions to efficiently combine battery and capacitive sources to improve system lifetime is an urgent need. Indeed, the use of simple filter capacitances to reduce current peaks [2] doesn't represent an optimal solution due to its intrinsic lack of flexibility and adaptability. Moreover, the capability to dynamically control the actual current drawn by the battery is a crucial aspect of the problem. In this direction [3] and [4] present a DC/DC converter able to actively modulate the average current and to clamp possible overshoot currents. However, high frequency peaks due to switching activity are not properly filtered in both cases. Another fundamental point in this field is to achieve high efficiency values for DC/DC conversion, while limiting the value and the size of external inductors. Peak currents inside the converter are responsible for high power dissipation due to the on-resistance of switches, hence large inductance values are conventionally used to limit these peaks. An advanced approach relies on the concept of quasi-adiabatic capacitive charge [5], in which the overall charge of a capacitor is split into multiple charges at intermediate values of the final voltage. This method is the best solution for capacitive charge in terms of power dissipation [6]. Using this idea, advanced DC/DC converters have been developed [7], which implement a stepwise charge of the output load thus increasing efficiency.

The proposed integrated circuit provides a comprehensive answer to both aspects of battery degradation and conversion efficiency, combining input current regulation and stepwise output charge. Differently from other solutions, a programmable constant current is always drawn by battery under all converter conditions. Moreover, a stepwise approach is applied to the energy transfer between capacitive nodes of the circuit, by splitting it into a controlled number of steps. As a consequence, the peak current inside the inductor is limited, increasing efficiency. In fact, each stepwise energy transfer has a shorter duration than a one-shot transfer, so the damping effect on the current waveform due to parasitic resistances is limited as well [8]. In addition, design criteria include minimization of the overall intrinsic and quiescent current consumptions.

II. Architecture and Operation

The overall architecture is sketched in Fig. 1, which shows the proposed integrated circuit (*IC*) along with the required external discrete components. The circuit consists of three main blocks: (*A*) a current regulator directly connected to the battery source, (*B*) the core DC/DC converter, consisting of (*B.1*) the main switching circuit and (*B.2*) the digital block that controls the stepwise conversion. The external blocks include a precision reference current, a fixed-frequency oscillator, an inductor L, and an intermediate buffer capacitance C_{buff}.

During normal operation, the current regulator forces the battery to linearly charge the buffer capacitance C_{buff} with a constant, programmable current I_{reg}. Once voltage V_{buff} reaches a predefined high threshold, ideally equal to the battery voltage V_{BAT}, the converter starts transferring energy from C_{buff} to the external load (e.g. a super-capacitor) through the inductor L, by adopting a stepwise algorithm, described in (Section II-B). This transfer produces a drop in V_{buff} voltage, which must be bounded by a low threshold, set above 90%-95% of V_{BAT} (Section II-A).

Once the low threshold is reached, the energy transfer is paused and C_{buff} is linearly recharged again, so starting a new

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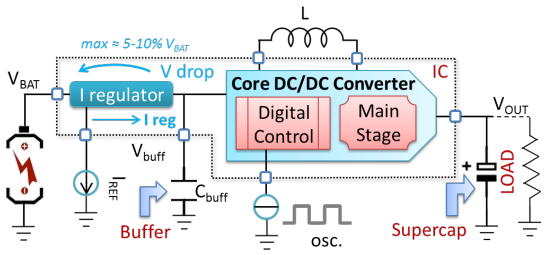

Fig. 1 Architecture of the proposed power converter

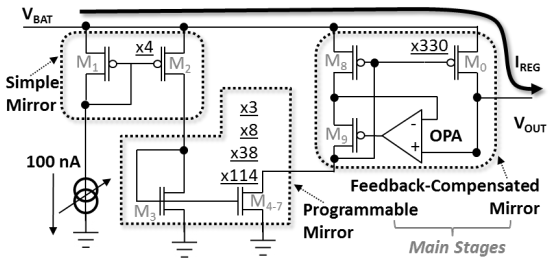

Fig. 2 Schematic of the current limiter

transfer cycle. As a result, the source battery always provides a flat current I_{reg}, while buffer capacitor C_{buff} always operates between two predefined thresholds, providing the current peaks required by the core DC/DC converter.

A. The Current Regulation Block

The current regulation block allows to continuously draw a constant, controlled current from the battery, which depicts the best condition for Li-Ion sources lifetime [9, 10]. Compared to a common filtering approach through a simple by-pass capacitor, the proposed solution, which combines a current regulation circuit with a buffer capacitor, allows the use of lower capacitance values with reduced area occupation and parasitic elements. The structure of the regulator is shown in Fig. 2, and consists of three different current mirrors. The first one is a simple x4 mirror composed by MOSFETs M_1 and M_2, used to decouple the two main mirror stages from the external reference current I_{ref}. Therefore, the more critical stages can be dimensioned on the basis of the first stage (M_2) to obtain a reliable multiplication factor substantially independent of the electrical properties of the external reference. The second stage is a programmable mirror composed by M_3 and $M_{4\text{-}7}$, which is an array of four transistors with different sizes implementing four different mirror ratios (x3, x8, x38, x114), selectable through two external signals. Finally, the third and output stage implements a feedback-compensated current mirror with an x330 ratio ($M_{8,9,0,}$ *OPA*). This architecture allows compensating mirror mismatch due to different values of drain voltages of M_0 and M_8 caused by variations of V_{OUT} node [11, 12]. As V_{OUT} is forced by the output capacitance, the operational amplifier *OPA* modulates the resistance of M_9 in order to equalize the drain terminals of M_0 and M_8, increasing mirror precision. The precision in regulation is directly proportional to the precision of external reference current I_{ref} and of current mirrors, although in this scenario the flat profile of regulation is more crucial rather than its actual value. In fact, by tuning I_{ref} it is also possible to obtain a wider range of regulated values to better meet different application requirements. For example, for I_{ref} = 100 nA, the circuit acts like a single current mirror with four programmable output currents of nominally 0.396, 1.056, 5.016 or 15.048 mA.

As for block efficiency, input and output currents are equal except for bias currents, which can be considered separately. Thus efficiency, defined as the ratio between output and input power, can be reduced to the ratio between output and input voltage. Input voltage is fixed at V_{BAT}, while output voltage varies between two predefined thresholds, $\alpha_H \cdot V_{BAT}$ and $\alpha_L \cdot V_{BAT}$.

Efficiency is therefore:

$$\eta_{REG} = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{V_{IN}} = \frac{\frac{\alpha_H + \alpha_L}{2} \cdot V_{BAT}}{V_{BAT}} = \frac{\alpha_H + \alpha_L}{2} \quad (1)$$

α_H should be chosen as close as possible to V_{BAT}, with a limit set by the complexity of the circuits needed to detect such threshold, which are supplied by the same V_{BAT}. A 1% margin can be chosen, setting α_H to 99%. Consequently, α_L can be selected accordingly to the required efficiency, obtained as

$$\eta_{TOT} = \eta_{CORE} \cdot \eta_{REG} \quad (2)$$

For example, to obtain an overall efficiency of 85% with a core efficiency of 90%, η_{REG} should be 94.4% with α_L = 90%. Considering the bias current, we can estimate it as

$$I_{BIAS} = I_{BIAS_{M8|9,4-7,2|3}} = \left(\frac{I_{REG}}{330} + \frac{I_{REG}}{330 \cdot 3} + \frac{I_{REG}}{330 \cdot 3 \cdot 4}\right) \cong \frac{I_{REG}}{233} \quad (3)$$

with respect to regulated current, which can impact as a 0.5% loss in efficiency as worst case. On the other hand, bias current of op-amp OPA is about 1 µA, thus weighting for another 0.4% loss as worst case. Ultimately, an overall 1% loss in efficiency can be considered for all bias currents of this block.

B. The Core DC/DC Converter and Stepwise Charge

Energy conversion is accomplished through a buck-boost DC/DC architecture combined with a dedicated digital control circuit, which periodically transfers a predefined amount of energy from C_{buff} to external load. In the proposed stepwise architecture, the ON phase duration, during which the inductor L is loaded, is regulated by the period of external oscillator OSC, while the OFF phase lasts the exact time needed to fully discharge the inductor towards the output load. Consequently, the converter operates on the boundary between continuous and discontinuous conduction mode, with no dead time between OFF to ON transactions. For regulated currents in the range from hundreds of µA to tens of mA, suitable values fall in the range of µF for C_{buff} and few hundreds of µH for inductor L.

1) Buck-Boost Architecture

The switching circuit is depicted in Fig. 3. This type of buck-boost topology allows to achieve high efficiencies [13, 14]. High-voltage (8V) lateral diffusion MOS transistors (LDMOS) have been used for the power section (switches *A*, *B*, *C*, *D*), while standard CMOS devices have been used for control logic. Fig. 4 shows the ideal waveforms of inductor current and buffer capacitance voltage. The ON phase initially starts when V_{buff} crosses $\alpha_H \cdot V_{BAT}$; switches *A* and *B* are ON (*D*-*C* OFF), and an increasing current flows from C_{buff} to ground through inductor L, approximately with a linear slope proportional to 1 / L. The energy stored in L is equal to $0.5 \cdot L \cdot I_{MAX}^2$, where I_{MAX} is the peak current at the end of this phase, which terminates at the next second edge of the clock signal (OSC oscillator), either falling or rising. Since its starting point is asynchronous with the clock,

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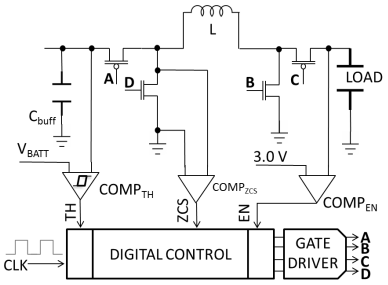

Fig. 4 Schematic of the core buck-boost converter

this phase can last from 1/2 to 1 clock period. Lastly, the value of I_{MAX} is determined by the duration of this phase. The OFF phase starts once I_{MAX} is reached (switches *D-C* ON, *A-B* OFF), and inductor L transfers its stored energy towards the output *LOAD* by forcing a decreasing current initially equal to I_{MAX}. When current is zero, *D* and *C* are opened again and a new ON phase is started. The alternation of ON-OFF phases produces an energy transfer between C_{buff} and the output *LOAD* with a consequent drop in the V_{buff} voltage, and it terminates when V_{buff} reaches $\alpha_L \cdot V_{BAT}$. Moreover, the regulation of the output voltage is performed through a hysteretic voltage monitor which disables the conversion when desired value is obtained.

In order to correctly manage the timing of all switches, three control signals are generated by different comparators. *EN* is used to monitor the output voltage and to enable the converter when it is different from the desired one. *TH* instructs the digital block whether V_{buff} is between the two predefined thresholds ($\alpha_H \cdot V_{BAT}$ - $\alpha_L \cdot V_{BAT}$). If true, the converter is enabled and the stepwise energy transfer is performed. Finally, *ZCS* is required to detect when the inductor current is zero during the OFF phase. In fact, during this phase the drain voltage of MOSFET *D* is kept slightly negative by the inductor L, so that a positive current can flow from ground to drain towards *LOAD*. At the instant when all inductor energy is transferred, drain current starts flowing in the other direction, so that drain of *D* returns positive. This behavior can be exploited by connecting a comparator between drain and source of *D* to detect the zero-cross event. Therefore *TH* is used to determine the beginning and the end of the stepwise transfer, while *ZCS* is used to trigger the end of the OFF phase, so that an additional signal is necessary to define the end of ON phase. This signal *IMS* is derived from the clock signal in a way that ON phase can last from half to one clock period. In a different perspective, the *IMS* signal also sets the maximum current I_{MAX} of the inductor so determining the stepwise transfer length as well as its intrinsic switching frequency.

2) Digital Block

The main purpose of the digital block along with gate drivers is to generate gate signals of MOSFETs *A-B-C-D*, accordingly to control signals described in *B.1* and the external clock.

Different aspects have been taken into account:

- Cross-conduction is prevented by delaying gate signals, so that switch *D* is always closed after *A* is opened, and *D* is always opened before *A* is closed (i.e. *A* and *D* are never closed at the same time). The same is for *B* and *C*.
- The first activation after the idle state is regulated by *TH* signal (when V_{BUFF} exceeds $\alpha_H \cdot V_{BAT}$). When *TH* goes high, if *CLK* is high then *IMS* is triggered by a positive edge of *CLK*, and vice versa. In this way the ON phase lasts at least 1/2 clock period, which is necessary as if ON phase is too short, then comparators may not able to detect threshold crosses and DC/DC converter may stall.
- After *TH* goes low (when V_{buff} falls behind $\alpha_L \cdot V_{BAT}$), the ongoing energy transfer is completed, to guarantee that inductor current is 0 before opening switches *B-C*, which otherwise may cause voltage spikes on their drain nodes.

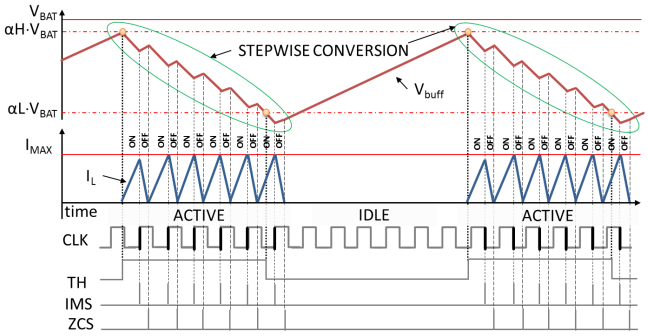

Fig. 3 Waveforms of proposed converter during normal operation

The proposed stepwise solution has a positive impact on converter efficiency if compared to a simpler architecture in which the energy transfer is performed through a single step (from $\alpha_H \cdot V_{BAT}$ to $\alpha_L \cdot V_{BAT}$ in a unique operation). Moreover, a higher number of steps implies a higher expected efficiency. Considering the energy losses caused by the circuit parasitic resistance R crossed by a current with an approximated triangular waveform, the ratio between the energy losses of a stepwise transfer of N_S steps of length T_{CLK} ($E_{LOSS(stepw.)}$) and an equivalent single transfer of length $\sqrt{N_S} \cdot T_{CLK}$ ($E_{LOSS(single)}$) is:

$$\frac{E_{LOSS(stepw.)}}{E_{LOSS(single)}} = \frac{R \cdot \frac{1}{3}\left(I_{MAX(stepw.)}\right)^2 \cdot N_S \cdot T_{CLK}}{R \cdot \frac{1}{3}\left(\sqrt{N_S} \cdot I_{MAX(stew.)}\right)^2 \cdot \sqrt{N_S} \cdot T_{CLK}} = \frac{1}{\sqrt{N_S}} \quad (4)$$

The consequent improvement in efficiency is:

$$\eta_{CORE} = \eta_{stepw.} = \frac{E_{IN} - E_{LOSS(stepw.)}}{E_{IN}} = \frac{\eta_{single}}{\sqrt{N_S}} + \left(1 - \frac{1}{\sqrt{N_S}}\right) \quad (5)$$

where the target simulated efficiency for a single step approach is $\eta_{TOT} = \eta_{REG} \cdot \eta_{CORE} = 85\%$. Finally, considering the impact on efficiency due to the introduction of the clock, operating at hundreds of kHz in our case, state-of-the art discrete oscillators can feature bias current down to 500 nA [15], while integrated solutions can reach down to 24 nA [16]. In worst case, the overall impact on efficiency can be estimated in the order of *0.5(μA)/400(μA) = 0.12%*. A possible jitter in clock period may cause a limited variation in the number of steps and eventually in the efficiency, which may be neglected in first approximation.

III. Results

The proposed solution has been implemented in a STMicroelectronics 0.16 μm BCD smart power technology in a 0.23 mm2 area (Fig. 5), and tested with a dedicated breadboard.

The current regulation was verified with a digital multimeter HP® 34401A in series with the input source (Agilent® E3631A power supply) and by analyzing the timing of the linear charge

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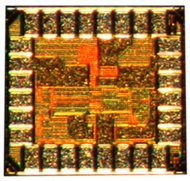

Fig. 5 Microphotograph of the implemented chip

of the buffer capacitor in order to infer both the flatness and the value of the regulated current. For example, with a measured current of 0.6 mA from multimeter and a voltage drop of 40 mV over a 10 µF buffer capacitance, the charge time is correctly observed to be ~ 680 µs with a constant slope. Similar tests were performed with an external current reference of 130 nA for different configurations, showing a discrepancy of about 10% with respect to nominal values probably due to mirror mismatches. Nevertheless the most crucial aspect of the flatness of discharge profile was verified. Concerning overall operation, measurements demonstrate that an increase in clock frequency actually produces an increase in overall efficiency as suggested, and values are consistent with analytical model (1), (2) and (5). A sample test is shown in Table 1. The remarkable aspect is that the measured efficiency increase (+1.1%) matches the expected value (+1%), although an offset of ~15% is observed, which can be explained by considering the realistic additional losses due to breadboard parasitics, which will be optimized at a later stage.

TABLE I.-RESULTS

Parameter		Value	*Unit*
Input V_{BAT} – Output V_{OUT} Voltage		2.0 – 2.77	V
C_{buff}		55	µF
L		100	µH
Quiescent Current		4	µA
I_{LIM}		0.6	mA
Thresholds (α_H- α_L)		98-95	% of V_{BAT}
η_{REG} (exp.)		(96.5)	%
η_{TOT} meas. (exp.)	@ 125kHz (N_S = 21)	71.9 (87)	%
	@ 140 kHz (N_S = 26)	73.0 (88)	

As for output load, a 10 mF capacitor and a 1 F supercap was tested, while output power is always limited by maximum input power = $V_{BAT} \cdot I_{LIM}$. Since duty-cycle and operating frequency do not depend on output load, they cannot be used to compensate high variable loads, so the output capacitor must be dimensioned depending on the application. Similarly, output ripple is regulated by the hysteresis of the enable comparator controlling the activation of the conversion. Waveforms showing multistep energy transfer and current regulation are shown in Fig. 6. A single transaction from α_H to α_L is focused, displaying single sub-steps and their correct synchronization with external clock, as well as threshold comparator output.

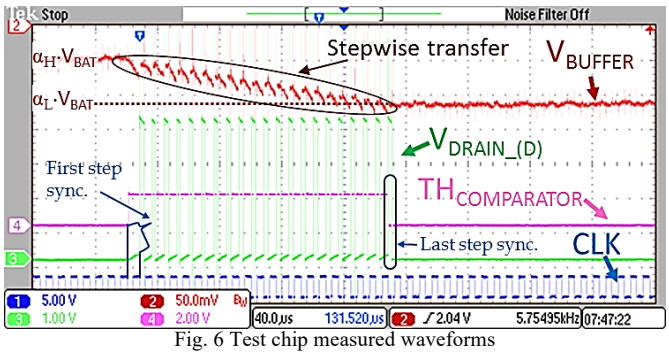

Fig. 6 Test chip measured waveforms

IV. CONCLUSIONS

In this paper we present an integrated buck-boost DC/DC converter addressing issues related to portable applications powered by batteries which can suffer from impulsive current loads in terms of reliability and lifetime. To this extent, a dedicated current regulator was designed to draw a constant, programmable current from sources, avoiding current peaks typical of conventional converters. Another crucial aspect is obtaining high efficiency with low bias currents, to extend operating time of connected devices. In this direction, a stepwise transfer policy is proposed to limit maximum currents inside circuit, dramatically reducing resistive dissipation losses.

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