An Integrated DC/DC Converter with Online Monitoring of Hot-Carrier Degradation

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***Abstract* — An integrated DC/DC converter with online monitoring of the degradation level of power MOSFETs due to hot-carrier injection (HCD) is proposed. The converter is able to dynamically estimate the on-resistance of the power switches and to provide its value to the user during normal operation. In fact, the correlation between an increase in on-resistance of power switches and HCD is fully documented, and it can be exploited to perform an estimation of degradation. The presented solution, developed in STMicroelectronics 90nm BCD technology, features a non-invasive current sensing and voltage sampling architecture, which is applied to a common boost DC/DC converter to evaluate the resistance of the switching power MOSFET. Without lack of generality, this specific sensing structure can be applied to any kind of converter, e.g. buck or buck-boost, as it doesn't require any change in the main conversion circuit.**

Keywords— DC/DC converter, hot-carrier degradation, online monitoring, reliability, current sensing

I. INTRODUCTION

Power conversion is an increasingly important research field in microelectronics, in particular as regards reliability and durability aspects which are gaining a crucial role in the design of this devices. The ability to predict an imminent failure or, more generally, to estimate the degradation level of power switches (e.g. power MOSFETs) is a promising approach in order to obtain more robust power management circuits that can be used in critical applications with low values of Mean-Time-To-Repair required or with high maintenance costs, as in Internet-of-Things applications. A widely studied deterioration pattern in double-diffused MOS (LDMOS) transistors can be associated with the degradation induced by hot-carrier stress (HCD), whose main effect is to produce an increase in the on-resistance of such devices [1][2]. This deterioration, which is caused by the concurrent presence of high gate-source and drain-source voltages, is easily observed in DC/DC converters due to the fast commutations of power MOSFETs. Different methods are proposed to tackle HCD issue, including the development of advanced physical layouts which are less susceptible to this kind of degradation [3]. On the other hand, working at circuit level, zero-voltage and zero-current (ZV-ZC) conversion architectures are proposed, aiming at smoothing or shifting the commutation edges in order to avoid the concomitant presence of high gate-source and drain-source voltages [4]. Finally, a growing interest is evinced in finding solutions able to monitor the degradation level of MOSFETs, in order to predict an imminent failure or possibly to compensate the negative effects from the increased on-resistance on the behavior of the converter. More precisely, various approaches are currently studied in this direction, either at circuit level by developing dedicated testing structures [5] or in combination with common conversion architectures [6], or by using advanced passive techniques like the measurement of the luminescent emission [7]. In this varied scenario, new improved transistor layouts as well as advanced passive measurements offer an interesting solution to the HCD prevention and monitoring problem, although they require specific equipment at very high costs. On the other hand, circuital approaches commonly introduce complex structures which impose a redesign of the original architecture as in the case of ZV-ZC converts, or which require additional external components to actually perform the monitoring operation.

The proposed circuit was developed in STMicroelectronics 90nm BCD technology and provides a complete integrated solution for online monitoring of hot-carrier degradation affecting LDMOS transistor in a common DC/DC boost architecture. The on-resistance of the transistor is constantly evaluated through a dedicated sensing architecture during normal operation of the converter, and its value is compared to a reference standard. In order to obtain the resistance measure, both current and voltage applied to drain-source nodes of the monitored transistor are tracked, by means of non-intrusive techniques. More precisely, the main structure of the DC/DC converter is separated from the monitoring circuit, and no additional elements are required inside the conversion path, e.g. shunt resistors, which may compromise the efficiency of the system. As a matter of fact, conversely to the ZV-ZC convert approach, no changes are required in the conversion architecture and standard structures can be used with improved efficiency and flexibility. Indeed, the proposed approach can be easily applied to other kinds of converters as buck or buck-boost. Moreover, differently from other solutions, conversion and sensing blocks are combined together in a single integrated circuit, providing a low-cost, comprehensive solution to the HCD monitoring problem. A special effort went into minimizing the overall intrinsic and quiescent current consumptions especially considering low-power IoT applications.

II. ARCHITECTURE AND OPERATION

The proposed architecture is depicted in Fig. 1, which shows the proposed integrated circuit delimited by the dotted line along

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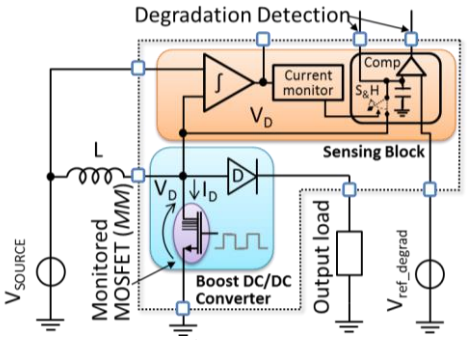

Fig. 1 Architecture of the proposed power converter

with additional discrete components. The circuit can be divided into two main blocks: the actual boost DC/DC converter (*A*) and the monitoring and sensing block (*B*). As introduced, the two modules can be considered as separate architectures because the power conversion circuit operates in a substantially independent way with respect to the sensing block. During normal operation, the monitored power MOSFET (*MM*) is periodically switched between an *ON* and an *OFF* state, as in common DC/DC converters. While in *ON* state, the current flowing inside *MM* is equal to the current inside the inductor, so that the latter can be effectively sensed without affecting the conversion circuit. Once the current is known, the voltage on the drain node of *MM* can be sampled at specific predefined values of flowing current, so determining the actual resistance of the MOSFET. Consequently, the degradation level of *MM* due to hot-carrier injection can be continuously estimated during normal operation of converter, starting from its relationship with the on-resistance, which can differently be characterized off-line. Additionally, the sampled resistance can also be compared to a reference value in order to generate an alert flag if the degradation level overcomes a predefined threshold.

A. *The Actual Boost DC/DC Converter*

The target architecture chosen to validate the monitoring solution is a conventional boost DC/DC converter [8]. The main purpose of this work is to introduce an integrated methodology for online monitoring of hot-carrier degradation in power MOSFETs used in power conversion circuits, so a general purpose approach is preferable to the use of a more specific conversion architecture. On one hand, the proposed solution is intended to be easily ported to other kinds of DC/DC converters (buck, buck-boost, etc.), while on the other hand the adoption of a boost structure allows the study of high-voltage architectures for both input and output stages, leading to a wider range of possible application scenarios.

The main conversion circuit is shown in Fig. 1 and it is made of the monitored MOSFET (*MM*), namely a 25V-tolerant power LDMOS, in a common source configuration and the output diode (*D*), plus an external inductor connected to supply source. The DC/DC operates on the boundary between continuous and discontinuous conduction mode, which means that the inductor is charged from a zero-state and then fully discharged at any conversion cycle, with no dead time between charge and discharge phases [9]. During an ON phase, *MM* is switched on and the inductor L is charged with a growing current flowing from supply source to ground through *MM*. This phase lasts until a predefined maximum current value I_{MAX} is reached, which is

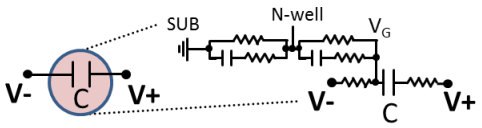

Fig. 2 Equivalent circuit of the integrated capacitor

estimated thanks to the sensing block (*B*). Subsequently *MM* is switched off, and an OFF phase is started, in which the inductor forces a current to flow toward the output load through the diode *D*, initially equal to I_{MAX}. The flowing current decreases until it is totally reset, and when the current is equal to zero, a new ON phase is started with a cyclic behavior. Differently from conventional boost converters, the duty cycle of the switching activity is used to control the maximum current inside the power MOSFET, rather than to control the output voltage. Consequently, an additional hysteretic comparator is necessary to sense the load voltage and to enable the power conversion only when its value is below the target one. The predefined hysteresis of this control block guarantees that the output voltage always stays within a fixed range. The overall circuit is designed to work with an input voltage from 3 V to 12 V and output voltage up to 20 V, while target switching frequency is in the order of few hundreds kilohertz.

B. *The Monitoring and Sensing Block*

The monitoring and sensing block allows to continuously evaluate the on-resistance of the monitored MOSFET (*MM*). The most critical task of this module is to track the current of *MM* without perturbing the operation and the efficiency of the converter. From a circuital point of view, many solutions have been studied to tackle this issue in several application fields, and in particular in DC/DC converters. A common approach is to use a shunt resistor in different configurations [10], however such technique introduces an unavoidable efficiency loss in the converter due to the additional resistive path, which can be critical in low-power applications. On the other hand, lossless techniques aiming at sensing the inductor current by integrating its voltage over time are gaining interest [11][12]. Finally, new solutions involving the use of on-chip sensors based on Hall effect are currently investigated which will may be profitably used in this kind of applications [13]. Within this scenario, the approach based on the integration of inductor voltage is currently an excellent trade-off between accuracy, complexity and efficiency. Concerning integration aspects, several topologies are currently available, with different numbers of capacitors involved. From a microfabrication point of view, particular attention must be paid on parasitic elements commonly associated with integrated capacitors. In particular considering the target BCD technology at 90 nm by STMicroelectronics, the equivalent circuit can be approximated as in Fig. 2, where they can be noticed at least two spurious R-C paths towards substrate and N-well nodes. In order to prevent these paths to add unwanted poles and zeros in the transfer function of the integrator, the minus pin of all capacitors should be shortened to ground. For this purpose, the integration architecture shown in Fig. 3 was chosen, which implies the use of a single capacitor on the feedback node.

The integrator circuit is made of an operational amplifier (*OPA*) with two integrated resistors R- and R_f- (respectively 10 MΩ and 10 kΩ) connected in feedback with the negative input

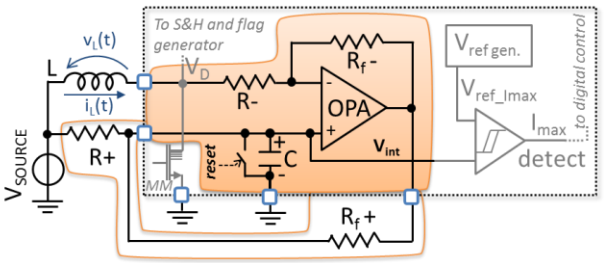

Fig. 3 Integrator circuit for inductor current sensing

of the OPA. Then, two external resistors R+ and R_f+ are connected in feedback with the positive input of the OPA, along with an integrated capacitor C (60 pF). The resulting signal V_{int} is proportional to the integral of the inductor voltage $v_L(t)$, and the overall transfer function in the Laplace domain is:

$$V_{int}(s) = \frac{L}{R^+ \cdot C} \cdot i_L(s) \cdot \frac{\delta \cdot s}{s + \frac{1-\delta}{R^+ \cdot C}} - \frac{V_{source}}{R^+ \cdot C} \cdot \frac{1-\delta}{s + \frac{1-\delta}{R^+ \cdot C}} \quad (1)$$

being $\delta = \frac{R_f^- R^+}{R_f^+ R^-}$ (2)

which in the time domain becomes

$$V_{int}(t) = \frac{L}{R^+ \cdot C} \cdot i_L(t) * \frac{\delta - 1}{R^+ \cdot C} \cdot e^{\frac{\delta-1}{R^+C}t} - \frac{V_{source}}{R^+ \cdot C} \cdot e^{\frac{\delta-1}{R^+C}t} \quad (3)$$

If the ratio δ is set to one, then the transfer function remains:

$$V_{int}(t) = \frac{L}{R^+ \cdot C} \cdot i_L(t) \quad \leftrightarrow \quad = \frac{R_f^- R^+}{R_f^+ R^-} = 1 \quad (4)$$

so that the V_{int} signal is proportional to the flowing current i_L. The drawback of using external resistors could be the presence of the parasitic capacitances associated with the pads, but with this configuration the only effect would be to change the overall value of C, without affecting the linear correlation between V_{int} and i_L. On the other hand, the external R+ can be used to set the value of peak current I_{MAX}, which can be calculated with:

$$R^+ = \frac{L}{V_{ref\_I_{MAX}} \cdot C} \cdot I_{MAX} \quad (5)$$

In fact, when V_{int} reaches the value of the reference signal V_{ref_Imax} (= 1.05 V) a control signal is generated which enables the sampling of the drain voltage of the monitored MOSFET and kicks off the OFF phase of the conversion cycle, as described in (B). The drain voltage is therefore always evaluated at a constant predefined value of the current I_{MAX}, so that it is directly proportional to the on-resistance R_{on} of the MOSFET. The sampled value is available at a dedicated pin of the chip to be estimated during normal operation, but an additional comparator is also included which generates a specific flag signal if the R_{on} exceeds a reference value which must be provided externally. Finally, a specific reset circuit is designed which completely discharges capacitor C at the end of each integration period (i.e. the ON phase), in order to guarantee the initial condition of the consequent period and to erase the incremental error typically associated with integration operations. The waveforms of involved signals are depicted in Fig. 4. In the first row, the drain voltage of the monitored MOSFET is shown, along with its sampled value. It is also shown how the sampling event always occurs when the current is equal to I_{MAX}, both before and after

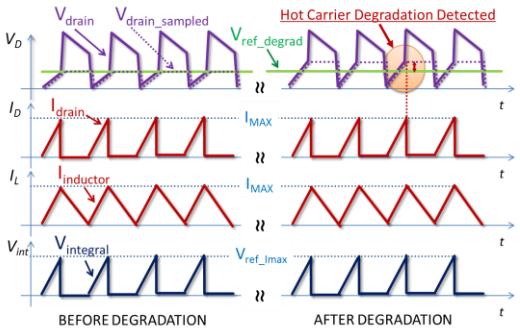

Fig. 4 Waveforms of main integration and control signals

degradation, as already explained. Therefore, after degradation the sampled value exceeds the nominal reference (V_{ref_degrad}) due to the increased on-resistance of the power MOSFET, and an alert flag is issued.

The sensitivity of the alert signal is substantially dependent on the sensitivity of the circuit which compares the sampled voltage with the reference one, and on the maximum current I_{MAX}. Indeed, it's worth noting that a positive effect of sampling the drain voltage when current is at its maximum is that the voltage difference due to degradation is maximum too, since

$$\Delta V_d(degrad) = \Delta R_{on}(degrad) \cdot I_{MAX} \quad (6)$$

The designed comparator has a simulated sensitivity of ≈ 3mV (V_{ref_degrad} = 0.5 V), so if we consider a I_{MAX} current of 50 mA as an example, the maximum detectable increase of R_{on} is about 60 mΩ. However, the sampled voltage is also available outside the chip through a dedicated pin, so it is exploitable for further elaboration on-board.

Finally, for testing purposes, a dedicated operating mode was implemented in order to speed up the hot-carrier degradation process of the monitored MOSFET by forcing constant high values of gate-source (3-5 V) and drain-source (12-15 V) voltages at the same time. This is necessary because in normal condition HCD can be observed within time windows in the order of years, while with this test mode we are able to produce a degradation effect in terms of hours. When in this test mode, the digital control block is disabled and both gate and drain pins of the MOSFET are directly driven by external signals. A side-effect of this choice is that if we adopt a standard power package with thermal resistance of about 25 °C/W, the maximum acceptable dissipated power is about 5W, and the subsequent minimum on-resistance of the MOSFET is 7.34 Ω.

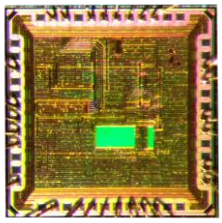

Fig. 5 Microphotograph of the implemented chip

III. RESULTS

The proposed solution has been implemented in a STMicroelectronics 90 nm BCD smart power technology in a

0.312 mm^2 area (4 mm^2 with pad-frame, mainly due to large number of test pads) (Fig. 5). Preliminary measurements were performed on single blocks of the circuit, including in particular the reference generator V_{REF} *gen.* described in section II.B, which is designed to generate a constant 1.05 V voltage. Experimental results show that the circuit correctly provides the required level with all acceptable supply voltages in the range 3-9 V. Then the sensing and monitoring architecture was tested with the setup parameters reported in Table 1.

TABLE I.-SETUP PARAMETERS FOR TESTING

Parameter	**Value**	***Unit***
Input Voltage	3 - 12	V
L	0.47 / 10	mH
R+	0.309 / 6.2	MΩ
R_f+	0.309 / 6.2	kΩ
Switching frequency	65 / 2	kHz
I_{MAX}	60	mA

In particular two sets of L, R+, R_f+ values were used to test the circuit with different switching frequencies. The measured waveforms of the sensing block are shown in Fig. 6. In particular it is possible to appreciate how the integrator signal (V_{int}) during the sample period, (ON phase of DC/DC conversion), linearly increase as it is proportional to the flowing current inside the inductor and the monitored MOSFET. In the same period the drain voltage (LDMOS drain voltage) slightly increases due to its on-resistance. As V_{int} reaches the reference value (V_{ref_Imax} = 1.05 V), the current is exactly at the predefined maximum value (60 mA), and the conversion toggles to the OFF phase. As a consequence, the drain voltage immediately raises to approximately the output voltage (out of the scale of the image), but its previous value is held by the sampling signal (Sampled drain voltage), so that it can be used for estimating the degradation level of the MOSFET. Simultaneously, V_{int} signal is reset to zero in order to be ready for the next integration period. In Fig.7 it is possible to appreciate the effect of an additional external 1 Ω resistance on the source node of the MOSFET, leading to an increase of $I_{MAX} \cdot 1\ \Omega = 60$ mV as expected.

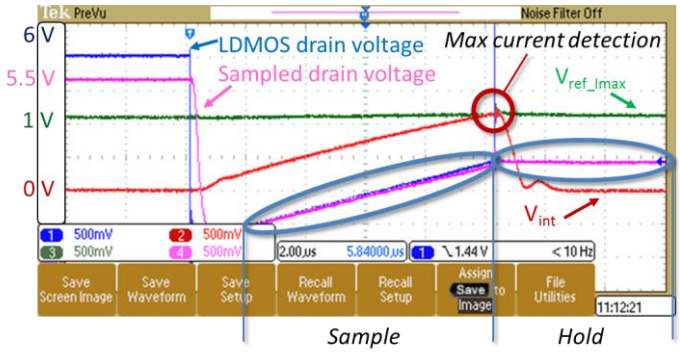

Fig. 6 Test chip measured waveforms – drain voltage sampling

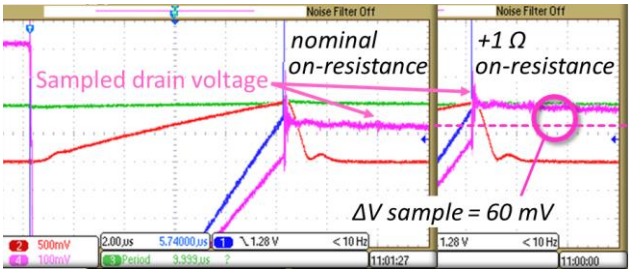

Fig. 7 Measured effects of a 1 Ω increase in on-resistance (60 mA I_{MAX})

IV. CONCLUSIONS

In this paper we present an integrated solution for online monitoring of the degradation level of power MOSFETs due to hot-carrier injection, specifically for DC/DC conversion circuits. To this extent a current and voltage sensing structure is added to a conventional boost converter aiming at continuously sampling the on-resistance of the MOSFET, which is strongly correlated with its degradation. For current sensing, a non-invasive lossless architecture is adopted which integrates the voltage across the external inductor in order to know the flowing current when it is equal to the one inside the MOSFET. The sampling of the on-resistance is always performed when the current is maximum, so that it is also maximum the effect of the degradation, in order to obtain the highest possible sensitivity.

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