Threshold Voltage Instability in SiC Power MOSFETs

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The Power Point Presentation will be available after the conference.

Abstract

Charge trapping and de-trapping phenomena in SiC power MOSFETs were investigated by performing two different types of electrical characterization: hysteresis and positive bias temperature instability (PBTI) measurements. A positive stress voltage to the gate results in positive threshold voltage shift (ΔV_T), which can be fully recovered by applying a small negative voltage. This fully recoverable ΔV_T behavior is ascribed to the trapping and de-trapping of electrons from the SiC layer into the pre-existing interface or oxide traps and vice versa. The apparent anomalous decrease of the trapped charge with temperature is ascribed to the faster de-trapping which occurs at higher temperature during the measurement delay between the stress and the sense phase. The trapping rate exhibits a universal decreasing behavior as a function of the trapped charges, independently of stress voltage and stress temperature.

1 Introduction

Silicon Carbide (SiC) is emerging as the most viable technology alternative to existing Si-based technology for the next generation of high efficiency power MOSFETs, due to its superior performance in terms of breakdown voltage, operating electric field, operating temperature and switching frequency. In order to increase the market growth of SiC technology, it is mandatory to rapidly improve our understanding of the corresponding reliability issues. In particular, several experimental studies have shown that power MOSFETs based on wide bandgap semiconductors, such as SiC and GaN, exhibit larger and faster threshold voltage (V_T) instability compared to their Si counterparts [1-8]. In the attempt to improve our understanding of this reliability issue in SiC MOSFETs, we report an experimental study based on hysteresis and positive bias temperature instability (PBTI) measurements.

2 Experimental details

The investigated devices are SiC power MOSFETs, characterized by a breakdown voltage of 1200 V and R_{DSon} at V_{GS}=20V equal to 50mΩ. Fig.1 shows the temperature dependence of I_D-V_{GS} curves. A significant decrease of the threshold voltage is observed by increasing the temperature.

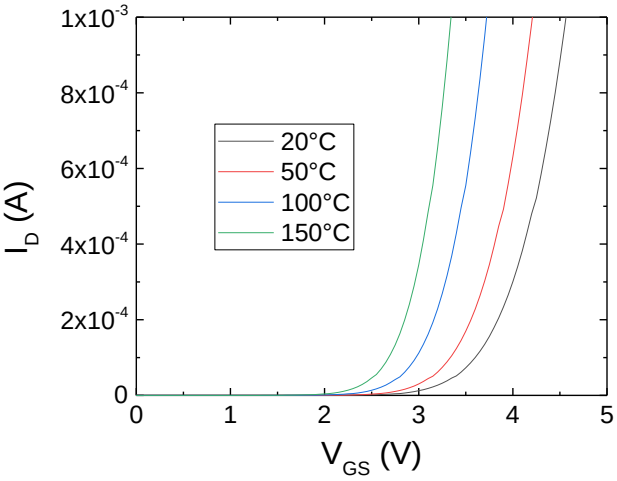

Fig. 1: Typical I_D-V_{GS} curves at V_{DS}=50mV for different temperatures in SiC power MOSFET.

Charge trapping phenomena were investigated by performing two different types of electrical characterization: hysteresis and PBTI measurements. Both measurements were done by using the parameter analyzer Keithley 4200-SCS. The hysteresis measurements have been obtained at room temperature by sweeping the V_{GS} from a minimum voltage of -5V up to a maximum voltage varying from 5V to 15 V and vice versa, at V_{DS}=50mV. The minimum voltage was fixed at -5V, in order to reset the device characteristics by de-trapping the charge.

PBTI stress measurements were done by applying different V_{GS} and temperatures and with V_{DS} = 50mV (Fig.3). Before performing PBTI stress, an initial stabilization phase was done. This phase consists of applying a negative gate voltage (typically -5V) for 10s, with the purpose of releasing the charges originally contained in trapping centers. The stabilization allows the device to reach a reproducible reference state for the subsequent experiments. After this phase, we measured a complete I_D-V_{GS} curve by sweeping V_{GS} from -5V to 3.5V. In order to monitor the evolution of the stress-induced degradation, the stress was interrupted at fixed time intervals and I_D at V_{GS}=3V was measured and compared with the reference curve obtained in the stabilization step to calculate the threshold voltage shift (ΔV_T). Immediately after the stress phase, we executed the recovery phase, by biasing the device with a zero or negative gate voltage. Also in this phase, in order to monitor the recovery evolution, we interrupted the recovery at fixed time intervals and I_D at V_{GS}=3V was measured and compared with the initial reference curve.

3 Results and discussion

The I_D-V_{GS} hysteresis observed in a typical sample is reported in Fig. 2. We observe a significant hysteresis, in the order of a few hundreds of millivolts, in spite of the low applied gate voltages. The observed shift behavior is ascribed to the trapping and de-trapping of electrons from the SiC layer into the pre-existing interface traps and vice versa. As highlighted in the inset, the shift amplitude increases by raising the maximum applied gate voltage, since it allows filling the traps at higher energy levels. Moreover, the inset shows that all the I_D-V_{GS} curves overlap in the initial ascending part, thus confirming that the starting bias at -5V allows resetting the device characteristics by releasing the previously trapped charge.

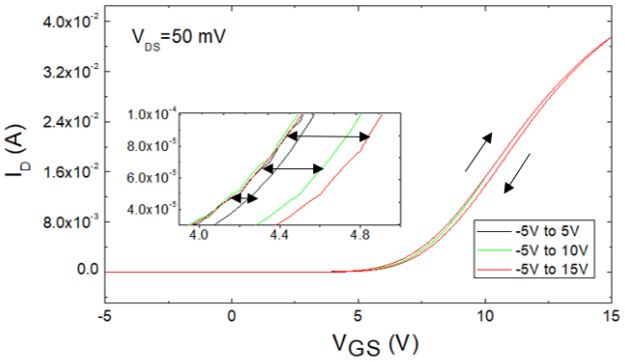

Fig. 2: A clear hysteresis is observed in the I_D-V_{GS} curve.

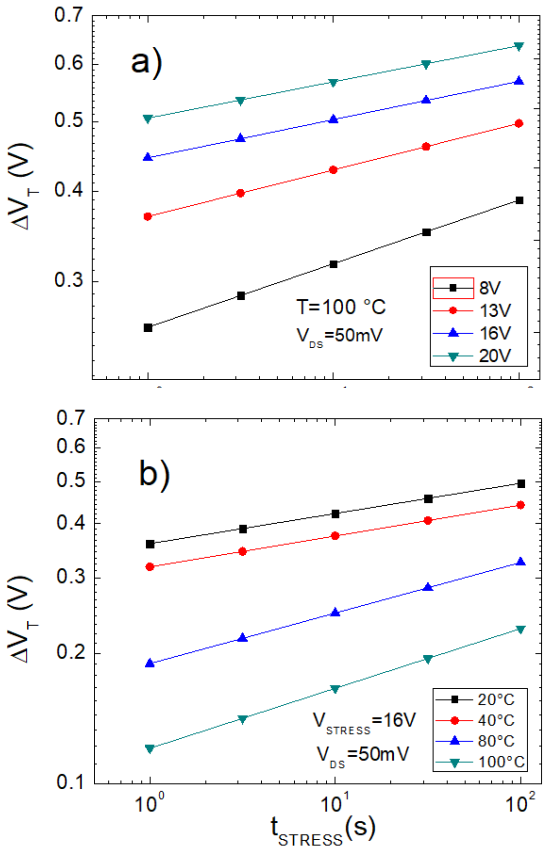

Fig. 3: ΔV_T evolution during the stress phase for different stress voltages (a) and temperatures (b).

Fig. 3 shows the typical time evolution of the stress-induced ΔV_T for different stress voltages and temperatures. We ascribe this observed ΔV_T to the trapping of electrons from the SiC layer into interface and border traps. In order to evaluate the rate of the charge trapping, we evaluated the

trapping rate parameter defined as $b=d(\log\Delta V_T)/d(\log t)$ (Fig.4). As expected, the observed ΔV_T increases with the stress gate voltage, while it exhibits an anomalous decrease with temperature. According to [1], although charge trapping during the stress phase is of course thermally activated, charge de-trapping is even more thermally activated, so the remaining ΔV_T after a measurement delay is lower at higher temperature.

As shown in Fig. 4, the trapping rate parameter considerably decreases by increasing the stress voltage and by reducing the temperature. By plotting the trapping rate parameter b as a function of the threshold voltage shift, which is a measure of trapped charges, for different experimental conditions (see Fig. 5), we observe a universal decreasing behavior of the charging rate as a function of the number of filled traps independent of stress conditions. In other words, the probability of charging traps is associated with the number of available empty traps.

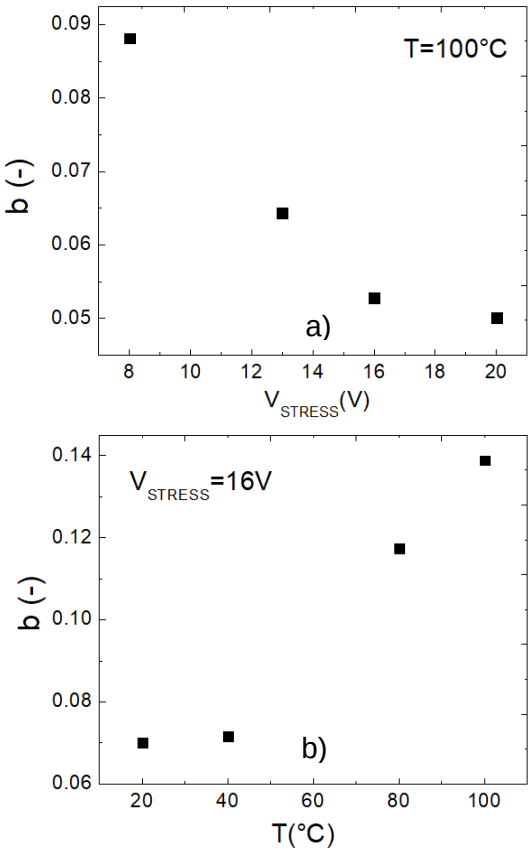

Fig. 4: Trapping rate parameter as a function of stress voltage (a) and temperature (b).

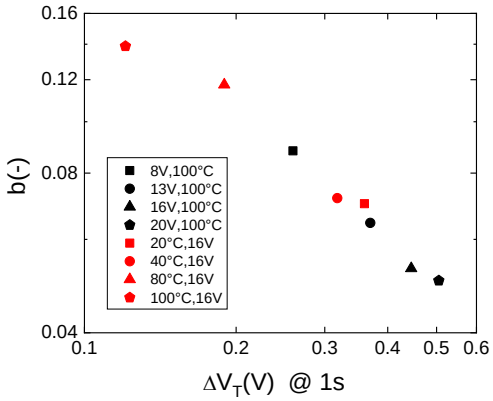

Fig. 5: Trapping rate parameter as a function of initial ΔV_T (after 1s stress).

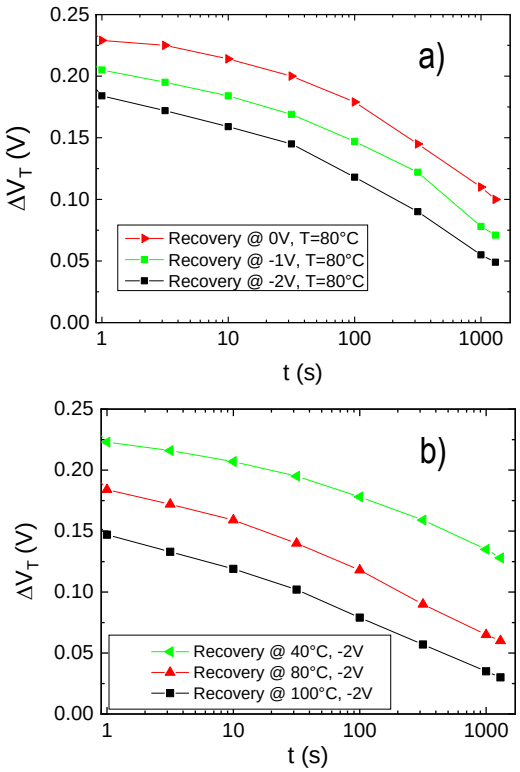

Fig. 6: ΔV_T evolution during the recovery phase for different recovery voltages (a) and temperatures (b).

Fig. 6 shows the relaxation data measured after PBTI stress for different temperatures (same temperature for stress and recovery) and recovery voltages. For a sufficiently high recovery time, ΔV_T tends to zero, thus indicating that in our experimental conditions no permanent damage

was introduced during the stress phase. A faster recovery is observed for higher negative gate voltages and higher temperatures, since the electron de-trapping is accelerated by a reverse electric field and by temperature.

4 Conclusions

This paper has examined the large shift of the threshold voltage in SiC power MOSFETs, induced by positive gate bias.

We observe hysteresis in the I_D-V_{GS} curve in the order of a few hundreds of millivolts, even at low applied gate voltages. This phenomenon is mainly ascribed to electron capture at interface traps.

Before performing PBTI stress, an initial stabilization phase was implemented, in order to allow for a reproducible reference state. PBTI stress causes a significant ΔV_T, which is ascribed to the trapping of electrons from the SiC layer into interface and border traps. The observed PBTI ΔV_T increases with the stress gate voltage, while it exhibits an anomalous apparent decrease with temperature, because charge de-trapping is more thermally activated than charge trapping, so the remaining ΔV_T after a measurement delay is lower at higher temperature. The PBTI trapping rate decreases as a function of the trapped charge, independently of stress conditions.

In the investigated stress conditions, the PBTI induced ΔV_T is fully recoverable. ΔV_T recovery is accelerated by a reverse electric field and by temperature.

Acknowledgements

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5 References

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