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Threshold Voltage Instability in GaN HEMTs with p-type Gate: Mg Doping Compensation

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Abstract—In this letter, we present an analysis of the threshold voltage shift induced by positive bias temperature instability stress in GaN-based power HEMTs with p-type gate, controlled by a Schottky metal/p-GaN junction. In particular, we show the positive effect of the magnesium compensation process in the p-GaN layer on the long-term threshold voltage instability. When a relatively high positive gate bias is applied (Schottky junction reverse-biased), holes generated by impact ionization in the high-field depleted p-GaN region are accelerated towards the AlGaN layer, where, combined with the high temperature effects, create defects in the AlGaN or at its interface with p-GaN, causing a long-term positive threshold voltage shift. A process variation in the p-GaN layer is introduced which promotes a wider depletion region near the Schottky interface with the metal, lowering the electric field and reducing the generation of holes due to impact ionization. As a result, the long-term threshold voltage instability is improved without altering the DC transistor parameters such as threshold voltage, trans-conductance, subthreshold slope, etc.

Index Terms— Positive bias temperature instability, threshold voltage instability, breakdown voltage, magnesium compensation process, doping concentration, p-type GaN gate, power HEMTs.

I. INTRODUCTION

RELIABILITY, together with performance and cost, is among the most important features required for the adoption of GaN power devices in areas of increasing interest such as renewable energy, electric vehicles, data centers, industrial motors and consumer electronics [1, 2]. To date, a broad range of suppliers such as EPC, Infineon, Transphorm, Panasonic, GaN Systems, Dialog and Navitas produce GaN-based devices, characterized by different combinations of process and design options [3], to address several different power applications. Overall, the power electronics market strongly prefers enhancement mode transistors for reasons related to cost, size, safety and power consumption [4, 5].

CMOS-fab compatible power HEMTs with a p-type gate, grown on 200 mm Si-substrates [6], is among the most interesting solutions to achieve normally-off device operation, offering a good trade-off between reliability

and cost [7].

The impact of the gate metallization and, in general, of gate design parameters on the performance of p-GaN HEMTs has been extensively investigated in [8-10].

Several reliability studies focused on the p-GaN gate have been carried out over the last few years [11-25]. First, we proposed the equivalent circuit of the p-GaN gate, consisting of two back to back connected junctions (i.e. a Schottky and PiN diode formed by metal/p-GaN and p-GaN/AlGaN/GaN, respectively), and an empirical relationship between gate leakage and gate time-to-failure (TTF) guiding device optimization [14]. Then, in agreement with [14], a temperature dependent TTF, with an activation energy of 0.48-0.50 eV, has been reported in [15]. Finally, we demonstrated that the characteristics of the percolation path, leading to time dependent gate breakdown, significantly depend on the concentration of magnesium (Mg) in the p-GaN layer and on the aluminum (Al) concentration in the barrier layer [16, 17].

In addition to the failure due to gate breakdown events, another important mechanism limiting the device reliability is the threshold voltage (V_{TH}) instability during high temperature gate bias (HTGB) tests, also named positive bias temperature instability (PBTI) stress [18-25]. In particular, in [18] we investigated the role of the aluminum concentration in the AlGaN barrier on the V_{TH} instability occurring during PBTI stress, proposing the presence of two competing trapping mechanisms: i) holes filling of pre-existing defects located in the AlGaN, causing a short-term negative and recoverable V_{TH} shift; ii) creation of defects filled with electrons, inducing a positive and permanent (or slowly recoverable) V_{TH} degradation. The latter mechanism, occurring at large positive gate biases, has been attributed to holes generated by impact ionization in the high-field depleted p-GaN region and accelerated towards the AlGaN layer [18].

The results of experimental analysis reported by several authors [19-24], based on constant voltage and/or pulsed/transient stress, seem to confirm the presence of two mechanisms occurring in the p-GaN/AlGaN stack, i.e. holes injection and electrons trapping, although the details of temperature and gate bias dependence are related to the specific stress technique and device process adopted in each study [18-24].

Finally, Tajalli et al. recently demonstrated the suppression of the negative V_{TH} shift by optimizing the etching and passivation of the p-GaN sidewalls [25].

In this letter, which is complementary to [18], we further validate the theory proposed in our previous study and propose a possible solution aimed at reducing the long-term positive V_{TH} degradation occurring during PBTI stress. It consists of a magnesium compensation process implemented in the p-GaN layer in the vicinity of the gate metal interface.

II. DEVICES CHARACTERISTICS

Enhancement-mode GaN-HEMTs with p-type gate, fabricated at imec on 200 mm Si-substrate using an Au-free CMOS-compatible process flow [26] are considered in this study. The top layers, grown on a super lattice buffer, consist of a 400 nm-thick GaN channel, a 12.5 nm-thick AlGaN barrier with 22.5 % aluminum concentration, an 80 nm-thick p-type GaN layer doped with magnesium and a 30 nm-thick TiN metal.

The devices under test (DUT) feature a symmetric structure with a gate length (L_G) of 0.8 μm, gate-source/drain spacing length ($L_{GD} = L_{GS}$) of 0.85 μm, and gate width of 100 and 500 μm. The adoption of different gate widths is motivated by the limited availability of the devices on-wafer. However, it is worth noting that different gate widths have been adopted only for the evaluation of the threshold voltage instability during PBTI stress, because, as well known for CMOS technology, and confirmed in Fig. 4 for p-GaN HEMTs, the underlying mechanisms are independent of gate area.

Two devices groups, named process 1 and 2, have been adopted. It is worth noting that the devices of these two groups are identical concerning materials, dimensions, etching, passivation, etc., except for the doping profile of the p-GaN layer. In particular, process 2 features a Mg compensation option, aimed at reducing the active P-doping concentration close to Schottky interface with the metal, thus widening the depletion region and reducing the maximum electric field in the p-GaN layer, while limiting the impact on threshold voltage [27].

As a matter of fact, on one hand the controlled Mg compensation process step has no impact on the transfer characteristics of the transistors in both sub-threshold and linear regions, as shown in Fig. 1. On the other hand, by observing Fig. 2, a clear impact can be observed on the gate leakage characteristics measured at different temperatures. As expected, independently of the temperature, process 2 shows a lower gate leakage at relatively high gate biases (solid lines). In particular, the reduction of the active doping concentration close to the Schottky junction, promotes a wider depletion region when a positive bias is applied on the gate, and the Schottky metal/p-GaN junction is reverse biased. As a result, for the same gate voltage (V_{GS}), the electric field is lower in process 2 and a lower gate leakage is attained for V_{GS} larger than 2 V (Fig. 2), i.e. the bias condition for which the Schottky barrier is limiting the leakage, as discussed in [16]. Moreover, in [16] it has been also shown that the gate leakage for V_{GS} lower than $\approx$ 1.5 V is mainly dominated by the p-GaN/AlGaN/GaN diode. Since the latter, is exactly the same for the two processes, the same gate leakage is attained for V_{GS} lower than $\approx$ 1.5 V (Fig. 2), without any modification of sub-threshold region (Fig. 1). This confirms that the adopted Mg-compensation option only impacts the Schottky interface region while the p-GaN/AlGaN/GaN diode is unaffected.

Fig. 3 shows the gate breakdown voltage (BV) extracted from the ramp voltage tests in Fig. 2. Two features can be noticed: i) a positive temperature

dependence occurs only in process 1. This behavior is ascribed to a dominant role of impact ionization as discussed in [18]. The lower the temperature, the higher the impact ionization generation, the lower the breakdown voltage of the metal/p-GaN Schottky junction. Furthermore, the higher impact ionization occurring at lower temperatures, speeds up the creation of defects in the depleted region of the Schottky junction, thus accelerating device failure as reported in [18]; ii) BV is temperature independent in process 2 and its mean value (exponential fitting in Fig. 3) is close to the highest BV mean value attained at 150 °C for process 1, confirming the reduced role of impact ionization. These results confirm the positive impact of increasing the depletion length and decreasing the electric field though the Mg-compensation option.

III. Threshold Voltage Instability

Fig. 4 shows the threshold voltage shift as a function of gate stress voltage and temperature on devices featuring different p-GaN processes.

The trapping mechanisms behind the dynamic of the V_{TH} instability has been discussed and detailed in [18], by analyzing devices with different processes. In particular, the initial temperature independent (or very small dependent) negative ΔV_{TH} is ascribed to filling by holes of pre-existing defects, located in the AlGaN barrier, through temperature independent elastic tunneling. The positive ΔV_{TH} occurring at long stress times is explained by thermally activated creation of defects by hot holes. Because of the impact ionization mechanism occurring in the high-field depleted region of the p-GaN layer close to metal/p-GaN interface, holes can be generated and then accelerated in the valence band toward the AlGaN barrier where they release their energy to the lattice and combined with the phonon energy (high temperature), can create deep defects in the AlGaN barrier or at the p-GaN/AlGaN interface. In particular, by increasing the temperature, a lower hole kinetic energy is needed to create/activate a defect. Hence, although hot-hole energy is lower at higher temperatures, due to higher energy dissipation through hole-phonon scattering, the released energy can be still sufficient to create a defect. Once defects are created, dependently on their energy position inside the bandgap, they can be filled by electrons coming from the 2DEG or from the AlGaN valence band, causing a positive ΔV_{TH}.

The relevance of impact ionization in process 1 devices is confirmed by the positive temperature dependence of the breakdown voltage shown in Fig. 3 (process 1). Moreover, impact ionization at lower gate voltages (from ≈ 6 V to BV) can be confirmed by roughly estimating the electric field in the case of an abrupt one-dimensional Schottky junction (metal/p-GaN). In particular, thanks to the back-to-back diode model proposed in [16], where the voltage drop across the Schottky junction is calculated as a function of the gate bias, a maximum electric field of the same order of magnitude of the GaN critical field (3.3 MV/cm) is estimated for gate biases higher than ≈ 6 V, hence confirming the presence of impact ionization.

As improving solution, process 2 reduces the active Mg concentration near the Schottky interface, promoting a wider depletion region and a lower electric field when a positive gate bias is applied. The lower the electric field, the lower the amount of holes generated by impact ionization and consequently the lower is the positive ΔV_{TH} due to deep defects creation (Fig. 4, process 2).

IV. Conclusion

In this letter, the effect of the magnesium doping compensation on the threshold voltage instability induced by PBTI stress has been investigated in e-mode GaN-on-Si HEMTs. The theory behind the positive V_{TH} drift proposed in [18] has been further validated and, based on it, a viable process solution aimed at reducing the long-term positive V_{TH} shift has been proposed. In addition to [18], where the role of the aluminum concentration in the AlGaN barrier on the V_{TH} instability was investigated, the role of the active magnesium profile in the p-GaN layer has been analyzed in this letter. In particular, by reducing the active doping (Mg) concentration in the p-GaN layer, only relatively close to metal interface, a more robust device to V_{TH} instability is attained without altering import transistor parameters such as threshold voltage, trans-conductance and sub-threshold slope.

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