A CMOS RF-Powered Tag with Sensing and Localization Capabilities

Cinzia Tamburini, Matteo Pizzotti, Michele Dini,
Marco Crescentini, Marco Tartagni, Aldo Romani
Advanced Research Center on Electronic Systems
University of Bologna
Cesena, Italy

Federico Alimenti, Marco Virili, Paolo Mezzanotte,
Luca Roselli
Department of Engineering
University of Perugia
Perugia, Italy

***Abstract*— This paper presents a battery-less CMOS integrated RF tag with sensing and localization capabilities. In order to allow tag addressing, communication, and localization by external readers, the IC performs a back-scattering modulation of a sequence of received UWB pulses according to specific spreading codes. For this purpose a UWB RF switch is designed and connected to the UWB antenna. The adoption of backscattering is integral to achieve ultra-low power wireless communication. The use of quasi-orthogonal spreading codes allows communication and localization with multiple tags at the same time. The IC includes a low-power sensing interface suitable for internal temperature sensing or external capacitive sensors. The power required for operation is scavenged from an UHF signal and converted by means of an internal RF rectifier and of a dynamically reconfigurable charge pump circuit. An on-chip micropower oscillator clocks a digital control circuit. The circuit is implemented in a 0.18 µm CMOS process. The architecture of the IC and preliminary test results are disclosed.**

Keywords*— *backscattering, charge pump, CMOS, energy harvesting, low-power oscillators, RFID, UWB localization, sensors

I. INTRODUCTION

A vast consent is developing around the vision of imminent and pervasive deployment of sensing nodes [1]. Sensors are expected to gather and transmit many and different types of data. A relevant contribution is expected in the field of energy efficiency and in the reduction of peak consumption from energy networks: scientific literature has demonstrated that informed users and more efficient in energy usage, with an estimated decrease of 9% [2] even without price incentives. However, in order to fully benefit of this technology, it is essential to devise strategies for seamless installation and powering of sensing nodes. As the use of batteries or of dedicated electric lines may be time-consuming for replacement and installation, new paradigms of RF-powered sensor nodes are emerging [3]. Sensors are powered and read on-demand by the users. Moreover, the localization of sensing nodes in space along with the possibility of embedded sensing through cheap tags, represents an extremely appealing feature in future logistics, biomedical applications, surveillance, indoor navigation systems. Several localization techniques are currently available [4]. Among them, those exploiting short UWB radio pulses and based on time-of-arrival measurements have the potential of discriminating positions with accuracies in the order of few cm even in harsh conditions [5] due to the intrinsic fine delay resolution of UWB signals. The use of CMOS integrated circuits [7] achieves notable performance in terms of operating distance of sensor tags.

This paper describes the design of a battery-less CMOS micropower implementation of a sensor tag embedding RF energy harvesting capabilities, a temperature sensor, a generic capacitive sensing interface, and a localization sub-system. The structure of the paper is the following: Section II introduces the architecture of the integrated circuits and provides an overview of the internal blocks; Section III provides figures of merit and a preliminary characterization of the IC performed on individual blocks.

II. IC ARCHITECTURE

The block diagram of the proposed IC is reported in Fig. 1. The RF sub-circuits integrate an UHF RF front-end that includes a rectifier for energy harvesting (EH) purposes and an ASK demodulator for synchronization with external readers, as well as an UWB switch for backscattering communication. The power management section (PwrMgmt) implements an inductor-less DC/DC converter based on a reconfigurable charge-pump and an ultra-low-voltage low dropout regulator, with the purpose of generating a stable supply voltage from the output of the UHF rectifier. The analog front-end integrates an ultra-low power oscillator and a sensing interface for

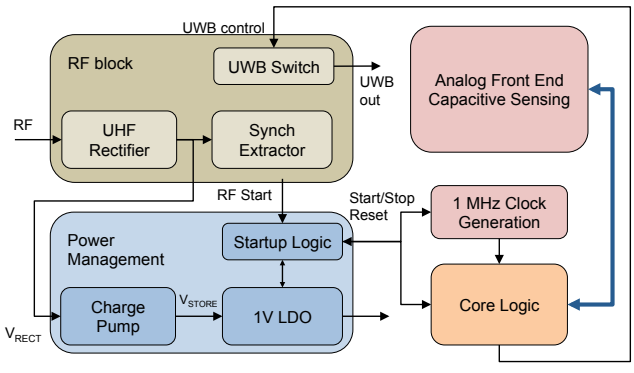

Fig. 1. Block diagram of the designed ASIC.

This research has received funding from the Italian Ministry of University and Research through the national PRIN project GRETA (2010WHY5PR) and from the ECSEL JU under grant agreement No. 737434. This JU receives support from the European Union's H2020 research and innovation programme and Germany, Slovakia, Netherlands, Spain, Italy.

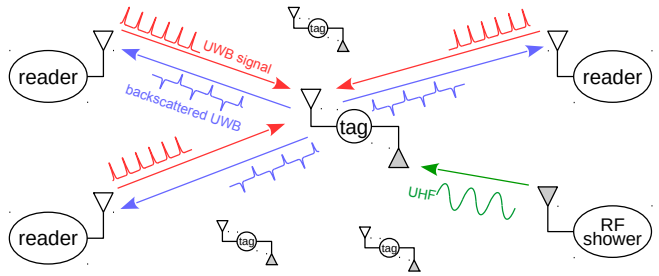

Fig. 2. Reference architecture of the localization system. UWB signals sent by readers are non-overlapping.

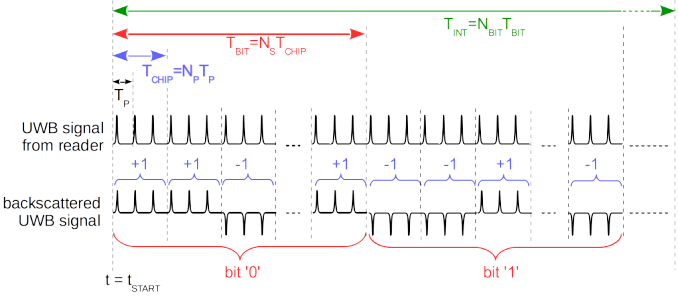

Fig. 3. Reference waveforms of UWB communication and localization. At time $t = t_{START}$, synchronization is sent by the UHF transmitter. N_P is the number of pulses per chip, N_S the length of the spreading sequence, T_{INT} the total tag interrogation time, N_{BIT} the number of transmitted bits. The spreading sequence used in the figure is {-1,+1, -1, …, +1}.

temperature and external capacitances. Digital control includes: a UWB switch gate drive, the logic for controlling backscattering according to the chosen spreading code, a SPI interface for interacting with external components, a read-only memory containing 8 pseudo random 1024-bit sequences to realize quasi-orthogonal spreading codes.

In the envisaged applications, nodes are placed in the environment and powered by radiating a dedicated UHF signal (RF shower), in a way similar to RFID tags, when the user desires reading sensor data (Fig. 2). Concerning tag communication and localization, multiple reference nodes, or readers, transmit UWB radio signals and monitor the corresponding waveforms backscattered by mobile tags. UWB backscattering has significantly looser power requirements than active RF transmission. A comprehensive theoretical description of the adopted architecture, protocols and signals for communication and localization is reported in [8]–[10]. To summarize, the reference nodes sample and process in a coordinated fashion backscattered UWB signals, extract the data transmitted by tags by means of their orthogonal codes, and compute the current tag position by means of time-of-arrival or time difference-of-arrival measurements. In order to fully take advantage of this technology, power consumption of the tag must be carefully minimized in order to guarantee operating distances of at least several meters from the RF source.

The proposed architecture does not require anti-collision protocols for UWB communications, since a CDMA-based scheme allows every reader to access simultaneously multiple tags. As shown in Fig. 3, when tags are fully powered by a UHF shower, a reader sends a synchronization signal on the UHF channel at time $t = t_{START}$ by modulating its amplitude, and starts emitting a sequence of UWB pulses, with a repetition period T_P. At this stage, as a response to the synchronization signal, every tag activates its internal UWB backscatter modulator, which updates its state every N_P pulses, and generates a reflected signal based on an individual unique spreading code. The backscattered signal has two antipodal configurations +1 and –1, which are obtained by applying an open or a short circuit condition to the UWB antenna. The spreading sequence is composed of N_S symbols. Since all spreading codes are quasi-orthogonal, the reader can recover every individual backscattered signal. Besides being used by readers for time-of-arrival measurements, the UWB backscattered signal is also used for data communications from tag to readers: a bit is transmitted by backscattering a regular or an inverted full spreading sequence. The total interrogation time for localizing the tag and transmitting N_{BIT} bits is $T_{INT} = N_{BIT}N_SN_PT_P$.

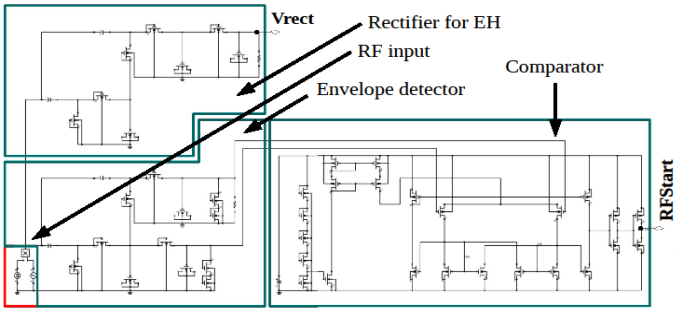

Fig. 1. Transistor-level schematic of the UHF front-end.

III. IC SUB-SYSTEMS

A. *UHF RF Front-end*

Fig. 4 illustrates the rectifier and the ASK demodulator circuitry. The rectifier is designed to harvest power from an UHF antenna implemented on paper substrate [9]. It exploits a 2-cell voltage multiplier architecture based on low threshold voltage transistors (LVT) in a diode configuration. Metal-Insulator-Metal (MIM) capacitors (2 pF) and MOSFET capacitors (3 pF) were adopted as DC blocks on the RF side and as charge storage on the DC side, respectively. The simulated RF input impedance of the rectifier is approximately 100 - 300j Ω for an available input power of -10dBm.

The ASK demodulator extracts the synchronization signal sent through the UHF link by the reader to align the respective clocks and to instruct tags to start the backscattering sequence. The demodulator shares the same RF input with the EH rectifier and is composed of an envelope detector and a threshold comparator. The envelope detector is based on a 2-cell voltage multiplier with diode-connected LVTs. However, here two RC low-pass filters are connected at the output of the first and of the second cell. These filters have different time constants and are used to extract the envelope signal (output of the second cell, low time constant) and the average signal level (output of the first cell, high time constant); the latter acts as a reference level. These two signals are then fed into

the threshold comparator working as an output pulse shaper. The nominal comparator threshold is around 25 mV with 150 nA current biasing, whereas its nominal sensitivity is -27 dBm, corresponding to an RF input voltage of about 150 mV. The overall power consumption of the ASK demodulator is about 200 nW (worst case simulations).

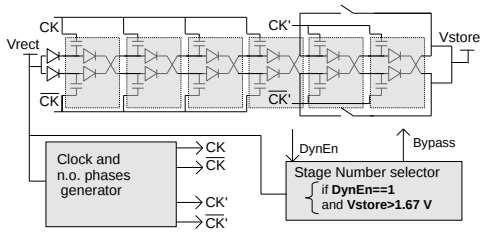

Fig. 2. Block diagram of the charge pump.

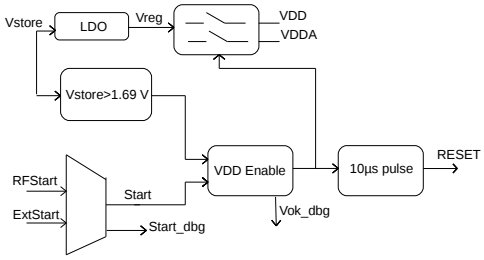

Fig. 3. Block diagram of LDO and StartUp circuit.

B. *Start Up and Power Management*

The block diagram of the charge pump is shown in Fig. 5. The DC-DC converter includes a voltage bias generator, a block for the clock generation, and a block that dynamically modulates the number of the active stages of the charge-pump based on the received power, in order to better track the maximum power point. When a configuration bit DynEN is high, and the value of the voltage exceeds 1.67V (dynamically triggered), the number of the active stages of the charge pump switches from 6 to 4. The charge pump is driven by a local oscillator generating two non-overlapping clock signals running at a 556 kHz frequency when the input voltage is 400 mV. In the PwrMgmt section, a low drop-out regulator (LDO) providing a $V_{DD} = 1$ V supply is included. A Start-Up circuit distributes the on-chip supply voltage when the output voltage V_{STORE} of the charge pump exceeds 1.69V and a start condition is received either from the UHF front-end (RFStart) or from an external signal (ExtStart). On these conditions, a reset signal is also generated in order for internal voltages to settle to a stable condition. The structure and interactions of these blocks are reported in Fig. 6.

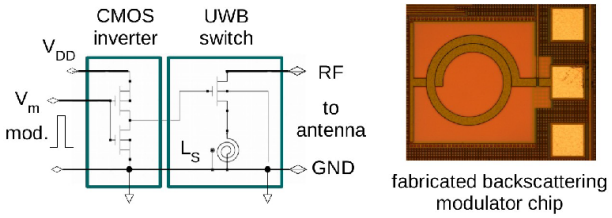

Fig. 4.. Transistor-level schematic and layout of the backscatter modulator. V_m is the control voltage.

C. *Backscattering modulator and UWB switch*

The backscattering modulator is shown in Fig. 7 and is composed of a CMOS inverter acting as a driver and an UWB switch performing the modulation by acting as an open or short circuit load for the UWB antenna, referred to as {+1} or {-1} configurations, respectively. The switch is based on a very simple MOSFET operating in off and on (triode region) states. The circuit operates in the frequency band between 3.1 and 4.8 GHz and the transistor has been sized considering an antenna impedance of 50Ω. The source inductor L_S adjusts to 180° the phase difference between the two modulator states. L_S consists of a 1.5 turns spiral with a diameter of 126 µm and was designed by following the procedure reported in [10]. The simulated energy required by the backscattering modulator is around 0.96 pJ per bit in the low-to-high transition and about 0.25 pJ per bit in the high-to-low transition.

D. *Digital Control*

Besides controlling the UWB switch, the digital part is in charge of: (i) controlling all the interactions between all the subsystems of the ASIC, (ii) providing synchronization and hand-shaking, (iii) managing spreading codes and transmission of sensor data either through the UWB or the wired SPI interface. A read-only memory stores predefined pseudo-random Gold sequences that can be selected and used by the backscatter modulator. The allowed configurations include the choice between: 3 pseudo-random 1024-bit Gold sequences, 1 pseudo-random 128-bit sequence, or 4 periodic sequences alternating {+1, -1} configurations at different rates. Every tag should be associated with a unique spreading code, according to the adopted CDMA architecture. With a 1 MHz clock, the lowest power consumption of roughly 2 µW is achieved with the simplest {512×(+1), 512×(-1)} periodic sequence applied to the UWB switch. Using 1024-bit pseudo-random Gold sequences requires 13 uW.

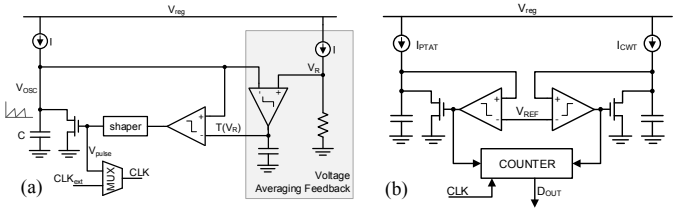

Fig. 5. (a) Architecture of the relaxation oscillator generating the clock signal. (b) Architecture of the read-out interface for temperature sensing.

E. *Ultra-low power oscillator*

The IC integrates a low-power, 1-MHz, relaxation oscillator generating the clock signal for the digital section (Fig. 8a). A constant DC current is injected into a polysilicon capacitor so as to create a ramp-up voltage V_{OSC}. This voltage is compared against a dynamic threshold $T(V_R)$ to generate a 10 ns pulse when $V_{OSC}>T(V_R)$. This pulse forces the discharge to ground of the oscillator capacitor C, and then the ramp-up starts again. The architecture also implements a voltage averaging feedback that dynamically changes the threshold $T(V_R)$ so as to desensitize the oscillating frequency to circuit non-idealities [7]. An external clock can also alternatively be used for testing purposes. Simulated figures of merit are:

(i) 1 MHz nominal oscillation frequency; (ii) 560-nW power consumption; (iii) line sensitivity lesser than 4%/V.

F. Analog Front End

The sensing interface manages either an internal temperature sensor or an external capacitive sensor (Fig. 8b). The read-out architecture is based on impedance/current-to-time conversion. Temperature sensing is performed by internally generating two bias currents: one proportional to absolute temperature (PTAT) current I_{PTAT}, and a second one constant with temperature (CWT) I_{CWT}. I_{PTAT} and I_{CWT} are then integrated onto matched capacitors until they both reach a reference voltage V_{REF}. This generates pulse events at the output of the comparators. A differential counter estimates the delay between the two pulse events with a nominal resolution of 8 bit. The nominal total power consumption of the analog interface (read-out circuit and current sensor) is less than 1 µW with a temperature sensitivity of 0.3 nA/ºC.

Sensing external capacitive sensors works similarly, but the injected current on the two branches is always a CWT current so that the delay relies only on mismatches between the capacitive sensor and a reference capacitor.

IV. Preliminary Test Results

The prototype of the CMOS RF tag was realized in a UMC 0.18 µm CMOS technology, in a 4.5 mm^2 area, corresponding to two blocks of a multi-project wafer. The unused area was filled with on-chip capacitors. A microphotograph of the IC is shown in Fig. 9. Preliminary tests were conducted on individual sub-circuits.

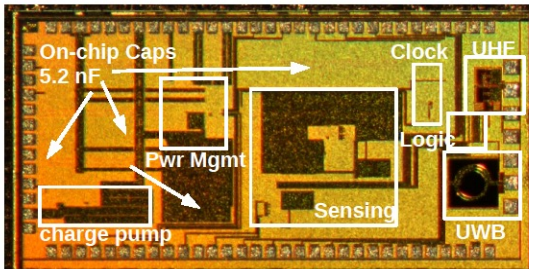

Fig. 6. Microphotograph of the designed ASIC.

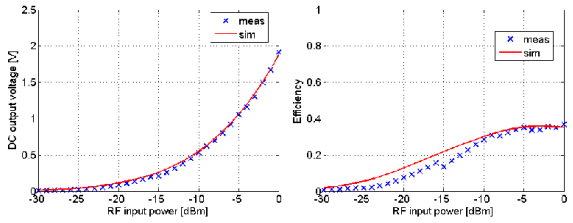

Fig. 7. Measured and simulated performance of the EH rectifier: output voltage (top) and conversion efficiency (bottom) versus the input power. The results are obtained with a 10kΩ output load and using an external matching network (L=33nH, C=3pF).

The EH rectifier performance was determined at a frequency of 900 MHz by measuring the output voltage as a function of the RF available power at the input. An input matching network was designed in order to improve the power transfer between an external RF generator and the chip. The measured output rectified voltage (with 10 kΩ output load) and the conversion efficiency are shown in Fig. 10. As expected, the circuit is able to provide a voltage greater than 500 mV with a RF input power equal to -10 dBm. In these conditions, the conversion efficiency is around 30%.

In order to characterize the ASK demodulator, the 900 MHz input carrier was modulated with a 1 kHz square wave (modulation index 90%). Simulations and measurements show that the minimum detectable variation in input signal amplitude is 120 mV.

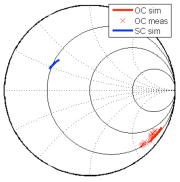

Fig. 8 Measured and simulated reflection coefficients of the backscattering modulator. Open Circuit (OC) state: V_m=0V, MOSFET off. Short Circuit (SC) state: V_m=1V, MOSFET in triode region

The last test of the RF section concerned the reflection coefficients of the backscattering modulator. The measurements were performed with a Vector Network Analyzer (Anritsu MS4623B) after de-embedding the main parasitics, at both PCB- and package-level. The obtained results are reported in Fig. 11 showing the operation of the modulator.

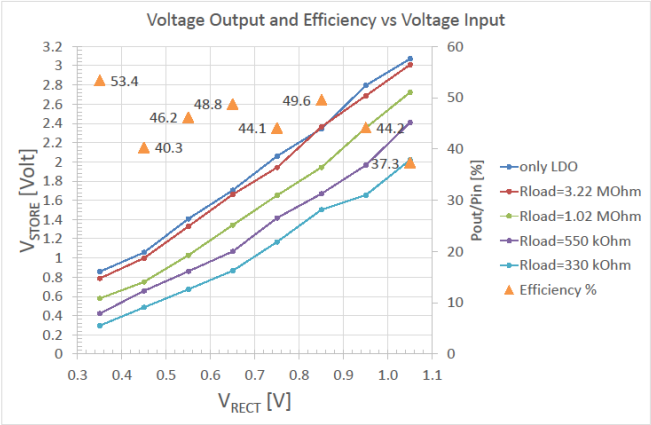

Fig. 9. Measured output voltage and efficiency of the charge pump circuit

In order to test the charge pump, a supply voltage ranging from 300 mV to 1 V was used to feed its input. A parallel circuit composed of a 100 nF capacitor and a variable resistor, was connected to the output port of the charge pump in order to estimate the available output power in different conditions. Measured voltages at the output of the charge pump, as well as the measured efficiency (P_{OUT}/P_{IN}), are reported in Fig. 12 as a function of the rectified voltage V_{RECT}. In this test, dynamic configuration of the number of the active stages of the charge pump was disabled. P_{OUT} was calculated as the sum of the power dissipated in the variable resistor and the power dissipated in the internal LDO.

Concerning the digital control and the backscatter modulator, tests confirm the application of the correct

configurations of the UWB switch. More specifically, it was observed that the produced bit stream corresponds to the selected pseudo-random sequence, which is managed with proper timings and inverted when required.

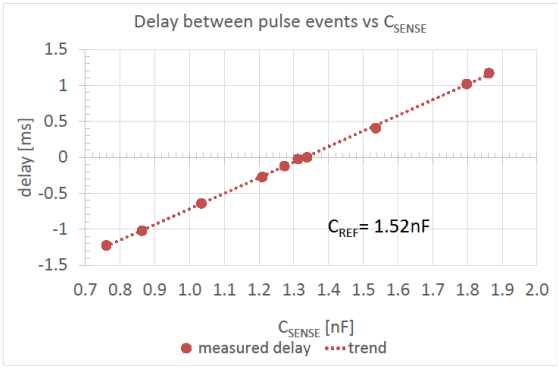

Fig. 10. Measured delay between pulse events in the analog read-out produced by C_{REF}=1.52 nF and variable C_{SENSE}.

For simplicity purposes, the sensing read-out interface was tested only against external capacitive sensors. A 1.52-nF capacitor was used as reference impedance while the capacitive sensor was emulated by using different capacitors of values ranging from 760 pF to 1.862 nF. Fig. 13 shows the results of single measurements on the different sensed capacitors. The standard deviations resulting from repetitions of the above measurements are lower than 25µs.

V. CONCLUSIONS

The developed IC has a very limited area, and the preliminary characterization results make it a suitable candidate for implementing battery-less RF-powered sensor tags. The additional feature of UWB localization grants additional application opportunities. The architecture is compatible with external capacitive sensors, and an internal temperature sensor i s included. Concerning the application to ubiquitous power metering, such architecture is complementary to contact-less Hall current sensors for achieving seamless installation in existing electric systems and appliances without additional wiring. Users might power the system by radiating RF and, when the system has collected sufficient energy, request a current measurement. The strict power budgets imposed by RF power transmission make such system suitable for single measurements rather than for continuous monitoring of electric appliances, which is still sufficient for increasing power-awareness of users and reducing energy consumption.

REFERENCES

[1] Y. D. Marinakis, S. T. Walsh, and V. A. Chavez, "Here there be dragons: The TSensors systems technology roadmap," in *2016 Portland International Conference on Management of Engineering and Technology (PICMET)*, 2016, pp. 2736–2750.

[2] A. Faruqui, S. Sergici, and A. Sharif, "The impact of informational feedback on energy consumption—A survey of the experimental evidence," *Energy*, vol. 35, no. 4, pp. 1598–1608, 2010.

[3] S. Gollakota, M. S. Reynolds, J. R. Smith, and D. J. Wetherall, "The Emergence of RF-Powered Computing," *Computer*, vol. 47, no. 1, pp. 32–39, Jan. 2014.

[4] D. Dardari, P. Closas, and P. M. Djuric, "Indoor Tracking: Theory, Methods, and Technologies," *IEEE Trans. Veh. Technol.*, vol. 64, no. 4, pp. 1263–1278, Apr. 2015.

[5] D. Dardari, A. Conti, U. Ferner, A. Giorgetti, and M. Z. Win, "Ranging With Ultrawide Bandwidth Signals in Multipath Environments," *Proc. IEEE*, vol. 97, no. 2, pp. 404–426, Feb. 2009.

[6] J. Kang, S. Rao, P. Chiang, and A. Natarajan, "Design and Optimization of Area-Constrained Wirelessly Powered CMOS UWB SoC for Localization Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1042–1054, Apr. 2016.

[7] M. Pizzotti, L. Perilli, M. Del Prete, D. Fabbri, R. Canegallo, M. Dini, D. Masotti, A. Costanzo, E. Franchi Scarselli, and A. Romani, "A long-distance RF-powered sensor node with adaptive power management for IoT applications," *Sensors (Switzerland)*, vol. 17, no. 8, 2017.

[8] F. Guidi, N. Decarli, S. Bartoletti, A. Conti, and D. Dardari, "Detection of Multiple Tags Based on Impulsive Backscattered Signals," *IEEE Trans. Commun.*, vol. 62, no. 11, pp. 3918–3930, Nov. 2014.

[9] N. Decarli, F. Guidi, and D. Dardari, "Passive UWB RFID for Tag Localization: Architectures and Design," *IEEE Sens. J.*, vol. 16, no. 5, pp. 1385–1397, Mar. 2016.

[10] F. Guidi, N. Decarli, D. Dardari, F. Natali, E. Savioli, and M. Bottazzi, "A Low Complexity Scheme for Passive UWB-RFID: Proof of Concept," *IEEE Commun. Lett.*, vol. 20, no. 4, pp. 676–679, Apr. 2016.