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Dynamic R_{ON} Characterization Technique for the Evaluation of Thermal and OFF-State Voltage Stress of GaN Switches

Tommaso Cappello, *Member, IEEE*, Alberto Santarelli, *Member, IEEE*, and Corrado Florian, *Member, IEEE*

***Abstract*—GaN power switches provide remarkable performance in terms of power-density, reduced parasitics, and high-thermal handling capability that enable the realization of very efficient and compact dc/dc converters. Despite exhibiting state-of-the-art channel conductivity, GaN high electron mobility transistor (HEMT) devices are affected by the degradation of the dynamic ON-Resistance (R_{ON}) at increasing OFF-state voltages and operative temperatures. In this paper, a novel laboratory setup and characterization procedure for the dynamic R_{ON} of GaN HEMT switches in the presence of thermal- and trapping-effects is presented. The proposed setup allows the study of R_{ON} transients after the switching event at variable OFF-state voltages and temperatures. The use of custom-designed differential amplification stages and a voltage-controlled current source enables the accurate characterization of R_{ON} even on large periphery devices. At first, the proposed setup is tested with a well-established and mature device technology such as a Si MOSFET. Degradation of the R_{ON} up to 120% due to temperature variation is observed with the presented setup. The setup is then used for the characterization of commercial-grade GaN-on-SiC and GaN-on-Si HEMTs. For both technologies dynamic R_{ON} degradations up to 75% and 20% are observed for temperature and OFF-state voltage variations, respectively. These characterization data are fundamental for the accurate estimation of conduction losses during the design of switching-mode power converters.**

***Index Terms*—Buck converter, characterization, dispersive effects, dynamic R_{ON}, GaN HEMT, pulse measurements, switching converter, trapping effects.**

I. Introduction

THE remarkable intrinsic characteristics of gallium nitride have enabled the development of GaN transistor technologies that set new targets in terms of efficiency and power density in several power electronic applications [1]–[3].

The well-known properties of wide-bandgap semiconductors and the characteristics of HEMT devices with lateral (rather than vertical) highly conductive channels implemented by means of AlGaN/GaN heterostructures are exploited for the production of compact and fast transistors with high breakdown voltage and very low losses [1]–[3]. While initially developed solely for radio frequency (RF) and microwave applications, GaN technologies have been recently proposed also for the power electronic market, with several commercial GaN switches already available [2].

These devices can be operated at higher switching speed compared to Si devices with comparable voltage and current capabilities (Si power MOSFET), due to lower switching and conduction losses [1]–[3].

Highly efficient switching-mode dc/dc converters have been reported in [4]–[6]. The high switching frequency enables compact designs and consequent improvements of the power density. Besides the increased power density, the fast switching performance of GaN has also been exploited for the design of power supplies with very fast dynamic response, to be used for example for the supply modulation of RF and microwave power amplifiers (PA) [7]–[11]. In such applications (e.g., envelope tracking [12]–[14]), the power supply output voltage follows the envelope of the signal (typically telecom) to be amplified by the RF PA, thus addressing multi-MHz instantaneous bandwidths.

In this context, Zhang *et al.* [10] reported synchronous buck converters with 88% total efficiency at 100-MHz switching frequency. These converters [10], [11] are designed with the same 0.15-μm AlGaN/GaN process of the RF PA for a perspective integration with the power supply.

Despite offering clear advantages with respect to their silicon counterparts for the design of highly efficient switching converters, AlGaN/GaN HEMTs suffer from a degradation mechanism of the dynamic ON-resistance (R_{ON}), which is different from Si power MOSFETs. The application of high electric fields to the device conductive channel created by the AlGaN/GaN heterostructure grown over SiC or Si substrates makes GaN HEMT prone to nonnegligible charge trapping phenomena. While in Si power MOSFET technologies trapping phenomena have been practically eliminated by the optimization of the passivation processes, the same cannot be done for GaN traps, since they are

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located in different regions of the device, rather than in the superficial passivation interfaces [18], [19]. The presence of traps in GaN devices is related to the intrinsic device structure and working mechanism, and thus it cannot be completely eliminated, but only limited to a certain extent by means of technological solutions as field plating [18], [19]. As a consequence, even mature, state of the art, commercial GaN devices suffer from this phenomenon (as it will be shown also in this paper), though with less deterioration in the dynamic performance with respect to early research-level devices [15]–[23].

It has been observed that the amount of trapped charge in GaN devices increases with the voltage applied (i.e., electric field stress) to the device channel and that there is a substantial asymmetry between the time constants associated to charge capture (almost instantaneous) and release (up to several seconds) [16]–[20] and [26].

From an application point of view (switching-mode converters), these phenomena induce a degradation of the device dynamic R_{ON} with increasing OFF-state voltages and increasing switching frequency.

Since the precise knowledge of the switch dynamic R_{ON} at different operating regimes (i.e., voltage, frequency, and temperature) is fundamental for an accurate computation of conduction losses in switching-mode converter design, suitable setups, and techniques for the characterization of dynamic R_{ON} of GaN device are of great interest.

In this paper, we propose a novel setup and characterization technique for the dynamic R_{ON} of GaN HEMT switches of GaN-on-SiC and GaN-on-Si technologies in the presence of thermal- and trapping-effects.

Section II provides an introduction to commercial and research-level I/V characterization systems. In Section III, the proposed setup is presented and further details are given in the Appendix. Section IV briefly describes two different GaN switch technologies that have been tested with the presented setup. Section V shows the characterization results under controlled thermal- and trap-state. Section VI concludes the paper.

II. State-of-Art and Commercial I/V Pulsers

In the literature, the characterization of the dynamic R_{ON} of GaN devices is carried out by exploiting two different types of setups:

1) commercial pulsed I/V characterization system (e.g., [16]–[18]);
2) research-level setups based on a standard electronic laboratory equipment and custom fixtures for R_{ON} characterization under a switching operation (e.g., [15], [20]–[23]).

As described in [16], [17], [28], [29], and [39], commercial pulsed I/V setups can be used for the characterization of the dynamic R_{ON} at variable OFF-state voltages, by successively switching the devices under test (DUT) from an OFF-state to an ON-state in the ohmic region of a device operation: this is done by the simultaneous switching of V_{GS} from complete pinch-off to maximum conductance and V_{DS} from the selected OFF-state to values in the range 0.1–1 V. The switching pattern features a very low duty cycle to control the thermal regime of the DUT.

The exploitation of these systems for dynamic R_{ON} characterization can have some drawbacks. The position of the voltage and current probes is usually not very close to the DUT, so that complex calibration procedures are needed to minimize measurement errors. The parasitics of the access networks to the DUT can cause not negligible voltage ringings that may set the device trapping state with a different peak voltage than the expected OFF-state voltage.

With modern pulsed I/V setups, the evolution of R_{ON} after the switching event can be also obtained by sampling the device voltage (and current) with high-resolution/high-dynamic range digitizer (e.g., 16–18 bit), that need to be capable to avoid saturation in correspondence of the high OFF-state voltages, while maintaining good resolution for sampling low V_{DS} in the device ohmic region. To cope with digitizer speed limitation (tradeoff with the required dynamic range), hundreds of measurements are performed for each data point and then averaged to enhance the characterization accuracy [16], [17].

Since these systems offer several additional features (pulsed IV curves, pulsed *S* parameters, pulsed load pull . . .) they are typically very expensive. Given these considerations, research-level custom setups may become a preferable solution.

Custom setups as the ones described in [15], [20]–[23] typically exploit a fast oscilloscope equipped with voltage and current probes to characterize the dynamic R_{ON} at variable voltage stress and its time evolution after the switching event.

With this approach, given the high dynamic range of the drain voltage of the DUT (from tens/hundreds of volts in the blocking state to few millivolt in conduction), a severe tradeoff between the oscilloscope saturation limit and its resolution at small voltages is encountered [15], [20]–[22] if the voltage probe is directly connected at the DUT drain terminal. Indeed, general-purpose oscilloscope samplers have typically a resolution in the range of 8–12 bits, due to higher importance of bandwidth rather than dynamic range of these products. In order to overcome this limitation, diode- and transistor-based clamping circuits are inserted between the oscilloscope probe and the sensed voltage node [15], [20]–[22].

Optimized clamping circuits enable the characterization of V_{DS} (and thus R_{ON}) starting right after the voltage stress (delay times between hundreds of ns to few μs) [15], [20]–[22]. The drawback of these solutions is a partial loss of accuracy, due to the need to de-embed the clamp electrical characteristic from the measurement.

Additional limitation in custom setups may arise from the types of probes adopted for voltage and current sensing. Depending on the DUT R_{ON} value (i.e., DUT periphery) and the amount of drain current during the characterization, the use of passive high-impedance voltage probes may limit the accuracy of the measurement of very low V_{DS}, whereas the use of typical magnetic-coupled probes may limit the accuracy in the acquisition of the current.

Finally, one additional characteristic that is valuable for a test setup is the possibility to characterize the R_{ON} of the DUT working in a switching condition similar to the final application. This is not always achieved by the setups commercially available or proposed in the literature. The novel setup and characterization technique presented in this paper address the described issues.

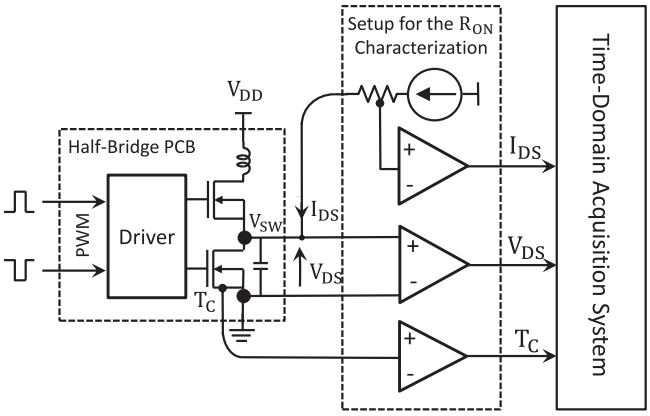

Fig. 1. Block diagram of the presented setup for the characterization of the dynamic R_{ON} in GaN HEMTs.

III. Setup for the Dynamic R_{ON} Characterization

As schematically depicted in Fig. 1, the proposed setup exploits a custom designed current source, active voltage and current probes, and a digital oscilloscope for the characterization of the DUT under real operative conditions.

With the proposed setup, implemented with standard laboratory equipment and COTS components, the characterization of the device R_{ON} is carried out at variable OFF-state voltages, temperatures, and dissipated powers. The observation of the entire evolution of the R_{ON} transient after the switching event enables the identification of the trapping mechanism time constants that directly correlate the R_{ON} behavior with the device switching frequency.

A. Working Principle

As described in Fig. 1, with the proposed technique, the DUT is tested when operating in the final circuit synchronous half-bridge, which is representative of a large number of switching-mode converters. This half-bridge can be either a section of an actual converter, or a printed circuit board (PCB) board suitably developed for the DUT R_{ON} characterization.

The DUT is the low-side switch of the half-bridge, whereas the high-side transistor is used to apply the OFF-state voltage stress V_{DD}. In both cases, the operating conditions are very similar to the ones in the final application in terms of thermal behavior, PCB parasitics, and driving waveforms.

With reference to Fig. 2, during the T_{OFF} part of the period T, the high-side device applies a V_{DD} voltage to the DUT drain. As discussed in [15]–[23], for GaN HEMT, the level of this OFF-state voltage stress induces a proportional amount of trapped charges which degrade the R_{ON}. During the T_{ON} part of the period, the DUT is turned-ON (and the high-side switch is turned-OFF) and a "measuring" current pulse $I_{\mathrm{CS}} = I_{\mathrm{DS}}$ is injected into the DUT by a current source.

The DUT current $I_{\mathrm{DS}}(t)$ and the voltage drop $V_{\mathrm{DS}}(t)$ are amplified and acquired by the instrumentation and the dynamic R_{ON} calculated as

$$R_{\mathrm{ON}}\ (t) = \frac{V_{\mathrm{DS}}\ (t)}{I_{\mathrm{DS}}\ (t)}. \tag{1}$$

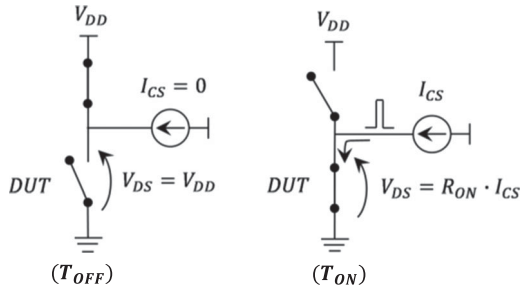

Fig. 2. Working principle of the setup. T_{OFF}: the high-side switch of the half-bridge applies a voltage stress $V_{\mathrm{DS}} = V_{\mathrm{DD}}$ to the DUT. T_{ON}: The DUT is turned-ON and R_{ON} is measured by the setup.

The evolution of $R_{\mathrm{ON}}(t)$ during T_{ON} describes its recovery, due to charge detrapping, to its nominal value of $R_{\mathrm{ON,DC}}$ observed before the OFF-state voltage stress.

As will be described in the following, the setup allows to observe this detrapping evolution of $R_{\mathrm{ON}}(t)$ in the range $T_{\mathrm{ON}} \in [t_D,\ t_{\mathrm{ON,MAX}}]$, where t_D is the delay of the beginning of the observation interval with respect to the switching event (DUT from OFF to ON).

B. Current Source

A voltage-controlled current source (VCCS), specifically developed to drive low-impedance loads (i.e., R_{ON}), is used to inject a current I_{CS} into the DUT and is controlled by a V_{CS} voltage. The VCCS shown in Fig. 3 is implemented with a cascode circuit: two high-power Si P-MOSFETs (Infineon SPB80P06P) are selected for this purpose. The cascode topology has been chosen to improve the output impedance with respect to the solution based on a single device (simulation results shows hundreds of k Ω) [31]. A 0.2-Ω source resistor improves the large-signal linearity of the VCCS by reducing its transconductance gain from 37 A/V (with $R_S = 0\ \Omega$) to 3.8 A/V (with $R_S = 0.2\ \Omega$) at $V_{\mathrm{CS}} = 3$ V.

A high-breakdown voltage (600 V) protection Schottky diode (Cree C3D10060G) has also been placed in series to the cascode to avoid the conduction of the body diode of the P-MOSFETs, when the switching node V_{SW} goes at V_{DD} voltage, which is typically higher than V_{CC}. The breakdown voltage of this diode sets the highest V_{DD} voltage stress that the setup could withstand without any damage.

The I_{CS} current generated by the VCCS is measured with a high-precision (0.1%) and high-thermal stability (15 ppm/°C) current-sensing resistor, provided with 4-wire Kelvin sensing terminals (Vishay CSM3637P, 20 − m Ω model). These terminals are connected to an opamp voltage amplifier, which provides the signal to be measured to the oscilloscope/digitizer. Details on current sensing are given in the following section.

The simulated and measured pulsed I/V characteristics at 25 °C of the VCCS are shown in Fig. 4 at different V_{CC} supply voltages. The simulation has been carried out in OrCAD PSPICE using Infineon nonlinear model comprising thermal effects.

The VCCS control voltage V_{CS} is generated by an arbitrary waveform generator (AWG-VCCS) and synchronized with the half-bridge driver through another AWG (AWG-HB). The

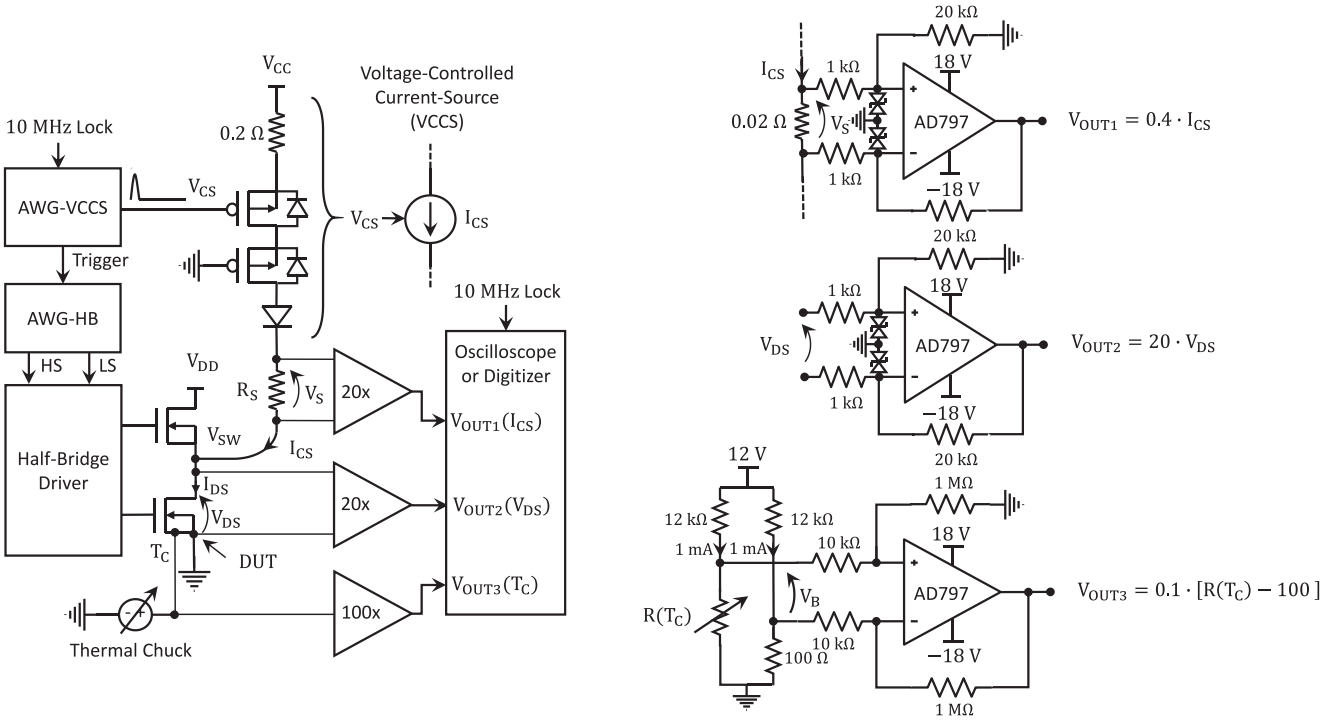

Fig. 3. Schematic of the setup for the characterization of the dynamic R_{ON} in GaN switches. The extraction is directly performed in the final circuit half-bridge (left block diagram). The high-side switch applies a voltage stress to the low-side (DUT) degrading its R_{ON}. When the low-side is ON, a current $I_{\mathrm{CS}} = I_{\mathrm{DS}}$ is injected and the V_{DS} voltage drop is measured by the setup. The case temperature T_C is controlled by means of a thermal chuck. The V_{DS}, the I_{DS} and T_C signals are amplified (right) and digitized by an oscilloscope.

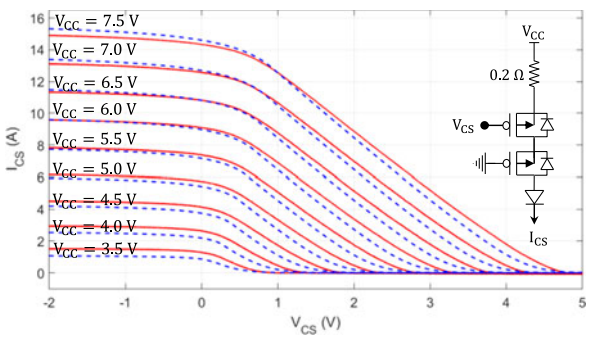

Fig. 4. Simulated (dashed blue line) and measured (continuous red line) I/V pulsed characteristic at 25 °C of the VCCS at different supply voltages $V_{\mathrm{CC}} =$ 3.5–7.5 V.

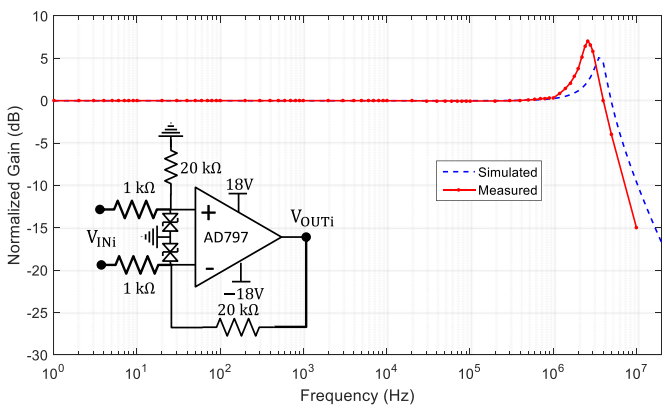

Fig. 5. Simulated (dashed blue line) and measured (continuous red line) small-signal gain (normalized) of a 20 × voltage amplifiers. The –3-dB bandwidth is about 6 MHz and the in-band ripple is lower than 0.03 dB up to 1 MHz.

AWG-VCCS generates a control signal between $V_{\mathrm{CS}} \cong V_{\mathrm{CC}}$ (VCCS OFF) and a lower voltage (VCCS ON) that can be selected depending on the requested output current I_{CS} (see I/V characteristics in Fig. 4).

The current I_{CS} generated by the VCCS is injected at the switching node of the half-bridge in order to measure the R_{ON} of the DUT by producing a V_{DS} voltage drop by means of a known current I_{DS}.

The current source as well as the amplification stage has been implemented on a single-layer FR4 board (see Fig. 6). The entire setup is controlled by a MATLAB script for automated measurements.

C. I_{DS} and V_{DS} Sensing and Measurement

The voltage drop V_S across the current-sensing resistor and the V_{DS} voltage on the DUT are amplified by two operational amplifiers in a differential to single-ended topology. The schematic is shown in the inset of Fig. 5. This circuit provides conversion from the floating voltage across the I_{DS} sensing resistor to a single-ended signal suitable for the oscilloscope acquisition. It is also useful to point out that this current sensing technique is not affected by common mode measurements errors typical of high-side resistive current sensing.

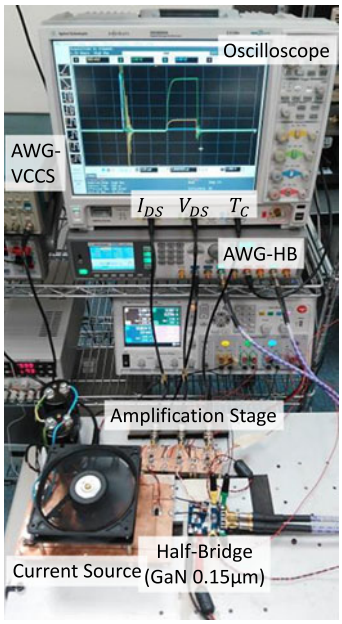

Fig. 6. Photograph of the setup for the dynamic R_{ON} characterization.

The V_{DS} sensing of the amplifier has been realized as close as possible to the switch package in order to minimize the resistance and the parasitics of the PCB traces.

A low-offset and low-noise operational amplifier (Analog Devices AD797) with a gain-bandwidth of 80 MHz (at 10× gain) has been employed for this purpose. The gain of the two amplifiers is set with the input (1 kΩ) and feedback resistances (20 kΩ), which are selected with low tolerances (0.1%) for accuracy. With such resistance values, the input impedance of the voltage amplifiers is high compared to the source impedance (R_S and R_{ON} are less than 1 Ω) and a negligible current will flow at the input of these circuits.

With the selected voltage gain of 20, the measured small-signal bandwidth is 4 MHz (see Fig. 5). The in-band distortion of both the amplifiers has been experimentally verified resulting in a gain ripple of 0.03 dB up to 1 MHz (see Fig. 5).

The V_{DS} voltage across the DUT can be obtained from the output V_{OUT2} of the amplifier by means of

$$V_{\mathrm{OUT2}} = \frac{20\ \mathrm{k\Omega}}{1\ \mathrm{k\Omega}} \cdot V_{\mathrm{DS}} \quad \rightarrow \quad V_{\mathrm{DS}} = \frac{V_{\mathrm{OUT2}}}{20}. \tag{2}$$

Similarly, the I_{CS} current generated by the VCCS can be computed from the output V_{OUT1} of the amplifier by considering

$$V_{\mathrm{OUT1}} = \frac{20\ \mathrm{k\Omega}}{1\ \mathrm{k\Omega}} \cdot 20\ \mathrm{m\Omega} \cdot I_{\mathrm{CS}} \quad \rightarrow \quad I_{\mathrm{CS}} = \frac{V_{\mathrm{OUT1}}}{0.4}. \tag{3}$$

The selection of a voltage gain of 20 and a 20-mΩ current-sensing resistor sets the maximum current measurable by the setup to approximately 40 A (pulsed). In fact, for $I_{\mathrm{CS}} = 40$ A and by considering (3), the output of the amplifier results in $V_{\mathrm{OUT1}} = 16$ V, which is still in the linear amplification region (2 V of margin on the supply rail of 18 V). Similarly for (2), the maximum V_{DS} value linearly amplified by the bench is 0.8 V.

Thus, by selecting $I_{\mathrm{CS}} = 1$ A and $I_{\mathrm{CS}} = 40$ A, two devices with very different R_{ON} of 800 and 20 mΩ, respectively, can be characterized with the same sensing accuracy of V_{DS}, which is for both 0.8 V at the input of the opamp and 16 V at the oscilloscope port. Different combination of opamp resistors and current sensing resistor could be also selected if different maximum rating of measuring current and voltages were needed. With this technique, the setup is capable to observe the R_{ON} evolution starting from 2 μs after the switching event and the saturation of the oscilloscope during the DUT blocking state is avoided (more details in the Appendix).

D. T_C Measurement

The case temperature T_C is monitored with a PT100 temperature-sensitive resistor (US-Sensor PPG101A6) with fast response (time-constant of 1.2 s in air) and high accuracy (±0.15 °C).

As shown in Fig. 3 (bottom-right), the PT100 resistor is inserted in Wheatstone bridge for a balanced reading by comparison with a fixed 100-Ω resistor. The upper resistors (12 kΩ ± 0.1%) and the 12-V supply voltage of the Wheatstone bridge are selected to feed a bias current of about 1 mA to the PT100, as suggested by the sensor manufacturer.

The differential voltage V_B of the bridge, which is proportional to the PT100 resistance, is amplified by 100 with another AD797 amplifier. All the gain-setting resistances of the amplifier are chosen with low tolerances (0.1%). The input resistors (10 kΩ) of the amplifier have been selected to provide a high-impedance input versus the Wheatstone bridge nodes. The feedback resistors (1 MΩ) have been chosen accordingly to obtain a gain of 100. With such gain, the bandwidth of the amplifier in closed-loop drops to 1 MHz but it is large enough for an accurate amplification of the case temperature, which is expected to vary in the Hz range.

The PT100 resistance $R(T_C)$ can be obtained from the output V_{OUT3} of the amplifier by means of

$$V_{\mathrm{OUT3}} = \frac{1\ \mathrm{M\Omega}}{10\ \mathrm{k\Omega}} \cdot 1\ \mathrm{mA} \cdot [R(T_C) - 100\ \ \Omega] \tag{4}$$

$$R(T_C) = 100 + 10 \cdot V_{\mathrm{OUT3}}. \tag{5}$$

During the characterization, the DUT (the entire half-bridge) is mounted over a temperature-controlled chuck. Thus, the case temperature T_C of the DUT can be controlled within a large range (25–440 °C), enabling R_{ON} characterizations at different operating temperatures.

IV. Devices Under Test (DUTs)

Two different GaN technologies and a Si MOSFET have been tested with the presented setup. These technologies are commercial products exhibiting the state-of-art performance in their fields of application. This makes the measured results more significant, since they represent real product performance rather than very particular behaviors (though still interesting) of not optimized experimental processes still in the development phase.

A. Si Power MOSFET

A Vishay SiR698DP has been selected as a reference benchmark for the setup. This power switch belongs to a very mature Si power MOSFET technology developed by Vishay (TrenchFET architecture) [41]. The DUT is mounted in a half-bridge configuration on an evaluation board [42]. The switching node of the half-bridge is directly accessed by the setup, as shown in Fig. 1. A discrete-component driver commutates the DUT between $V_{\mathrm{GS}} = 10\,\mathrm{V}$ (DUT ON) and $V_{\mathrm{GS}} = 0\,\mathrm{V}$ (DUT OFF).

B. AlGaN/GaN on Si HEMT

This technology developed by efficient power conversion [33] offers different families of normally OFF (enhancement mode) HEMT power switches grown on silicon substrates. The different families of products have breakdown voltages ranging from 15 to 300 V. The devices tested with the proposed setup are the following:

1) EPC 2014: 40-V, 10-A continuous current switch with a nominal maximum R_{ON} of 16 mΩ [34];
2) EPC 2007: 100-V, 6-A continuous current switch with a nominal maximum R_{ON} of 30 mΩ [35].

The first DUT was tested directly within the multilevel power converter described in [13], by disconnecting the load, whereas the second DUT was measured exploiting the evaluation board provided by the vendor [36]. In both cases the DUTs are always inserted in a half-bridge, as described in Fig. 1, and controlled by the same Texas Instruments LM5113 driver [40], which commutates the DUT between $V_{\mathrm{GS}} = 5\,\mathrm{V}$ (DUT ON) and $V_{\mathrm{GS}} = 0\,\mathrm{V}$ (DUT OFF).

C. AlGaN/GaN on SiC HEMT

This device belongs to a 0.15-μm gate length process by Qorvo [37], primarily developed for the design of monolithic microwave integrated circuit PAs at X, Ku, and Ka bands. In many applications, the efficiency of the RF/microwave PA is enhanced by means of supply modulation [12]–[14]. The highly desirable integration of the microwave PA and the supply modulator in the same chip can be exploited with this AlGaN/GaN on SiC technology that, despite the very short channel length, features good power switches with nominal breakdown voltage of 50 V and 2.1-Ω·mm R_{ON}.

The DUT is a 4-mm periphery device tested directly within the synchronous buck converter described in [10], by simply disconnecting the output filter and accessing the converter switching node, as described in Fig. 1. The driver is integrated with the monolithic half-bridge [10] and is designed to commutate a normally ON device by applying $V_{\mathrm{GS}} = -5\,\mathrm{V}$ (DUT OFF) and $V_{\mathrm{GS}} = 0\,\mathrm{V}$ (DUT ON).

V. Experimental Results

A. Dependence of the R_{ON} on T_J

The resistance R_{ON} of the DUTs in the half-bridge has been first measured with a multimeter provided with a 4-wire sensing capability (Agilent 34 401 A). We define this resistance as the dc ON-Resistance $R_{\mathrm{ON,DC}}$ at room temperature (25 °C) and any variation due to dynamic effects will be normalized to this value. The measured $R_{\mathrm{ON,DC}}$ for the considered DUTs are reported in Table I.

Let us now consider a switch model of the DUT in which the R_{ON} is a function of the junction temperature T_J and of the trapped charge state $X(t)$. The corresponding I/V model of the DUT in the ohmic region can be written in this form:

$$V_{\mathrm{DS}} = R_{\mathrm{ON}}\left[T_J, X\left(t\right)\right] \cdot I_{\mathrm{DS}}. \tag{6}$$

In this section, the R_{ON} variation due to the junction temperature T_J of the power switches will be investigated by means of pulsed measurements. In such measurements, the high-side switch of the half-bridge is constantly turned-OFF and only the low-side switch (DUT) of the half-bridge is considered (see example waveforms of Fig. 15 in the Appendix).

During this measurement, the acquired drain-source voltage of the DUT is between zero and a small voltage, the actual V_{DS} (i.e.,$<$ 0.8 V), during the injection of the current by the VCCS. In this operating regime, no degradation of the R_{ON} occurs due to trapping effects, since no OFF-state voltage stresses are applied and the V_{DS} in conduction is very low as observed ($<$ 0.8V). Thus, during this measurement, only thermal effects can induce variations of R_{ON} (no trapped charge, $X(t) \equiv 0$), and the R_{ON} depends only on the junction temperature T_J

$$V_{\mathrm{DS}} = R_{\mathrm{ON}}\left(T_J\right) \cdot I_{\mathrm{DS}}. \tag{7}$$

In order to extract the R_{ON} dependence on T_J, iso-thermal pulsed measurements are performed. A short current pulse (i.e., 5 μs) has been selected to minimize the self-heating during the current injection. This assumption can be quickly verified considering the device junction-to-case thermal resistance R_{JC}.

For a short current pulse (i.e., 5 μs), the junction-to-case temperature difference during the I_{DS} current injection can be written as

$$T_J - T_C \leq R_{\mathrm{JC}} \cdot P_D = R_{\mathrm{JC}} \cdot R_{\mathrm{ON}}\left(T_J\right) \cdot \ {I_{\mathrm{DS}}}^2 \tag{8}$$

where the dissipated power P_D in the DUT has been expressed by means of (7).

The Qorvo 0.15-μm process parameters were used for the following evaluation, but the same computations have been verified also with the other DUTs. Let us assume the worst case scenario in which for a short current pulse (i.e., 5 μs) the thermal impedance equates the thermal resistance $R_{\mathrm{JC}} = 1.8\,^{\circ}\mathrm{C/W}$ and the R_{ON} does not change significantly ($R_{\mathrm{ON}} \cong R_{\mathrm{ON,DC}} = 525$ mΩ). Thus, considering a measuring current $I_{\mathrm{DS}} = 1.1$ A, (8) provides that the temperature rise is negligible during the current pulse (i.e., $T_J - T_C \leq$ 1.1 °C). Same results apply also to the SiR698DP, EPC 2014, and EPC 2007: their worst case temperature rise is 0.7, 0.8, and 1.1 °C, respectively. Thus, there is no significant self-heating during the pulse and the T_J is iso-thermal with the case temperature T_C

$$T_J \approx T_C \quad \rightarrow \quad R_{\mathrm{ON}}\left(T_J\right) = R_{\mathrm{ON}}\left(T_C\right). \tag{9}$$

Therefore it is possible to extract the R_{ON} at different T_J by characterizing the DUT at different chuck temperature (T_C).

TABLE I
INVESTIGATED DUTS PARAMETERS

Device	Substrate	$V_{DS,MAX}^{**}$	$R_{ON,DC}$ *Condition	C_{GS} ** Condition	C_{DS} ** Condition	R_{JA} **
Vishay SiR698DP (normally-OFF)	Si	100 V	**136 mΩ** $T_J = 25\,°C$, $V_{GS} = 10\,V$, $I_{DS} = 2.5\,A$	195 pF $V_{DS} = 50\,V$, $V_{GS} = 0\,V$	20 pF $V_{DS} = 50\,V$, $V_{GS} = 0\,V$	75 °C/W
Qorvo 0.15 μm (normally-ON)	SiC	50 V	**525 mΩ** $T_J = 25\,°C$, $V_{GS} = 0\,V$, $I_{DS} = 1.1\,A$	6 pF $V_{DS} = 20\,V$, $V_{GS} = 0\,V$	1.6 pF $V_{DS} = 20\,V$, $V_{GS} = 0\,V$	17.5 °C/W
EPC 2014 (normally-OFF)	Si	40 V	**14 mΩ** $T_J = 25\,°C$, $V_{GS} = 5\,V$, $I_{DS} = 2.9\,A$	290 pF $V_{DS} = 20\,V$, $V_{GS} = 0\,V$	140 pF $V_{DS} = 20\,V$, $V_{GS} = 0\,V$	80 °C/W
EPC 2007 (normally-OFF)	Si	100 V	**20 mΩ** $T_J = 25\,°C$, $V_{GS} = 5\,V$, $I_{DS} = 2.9\,A$	198 pF $V_{DS} = 50\,V$, $V_{GS} = 0\,V$	111 pF $V_{DS} = 50\,V$, $V_{GS} = 0\,V$	80 °C/W

*Measured with the setup. **From DUT datasheets.

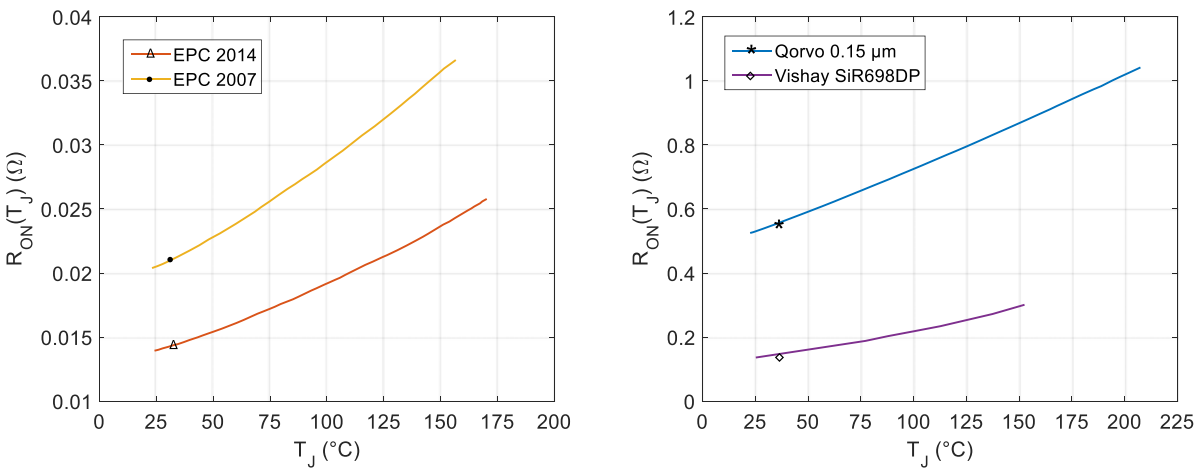

Fig. 7. Measured R_{ON} versus junction temperature T_J for the considered DUTs. Left: EPC GaN-on-Si HEMTs. Right: Qorvo 0.15 μm and Vishay SiR698DP.

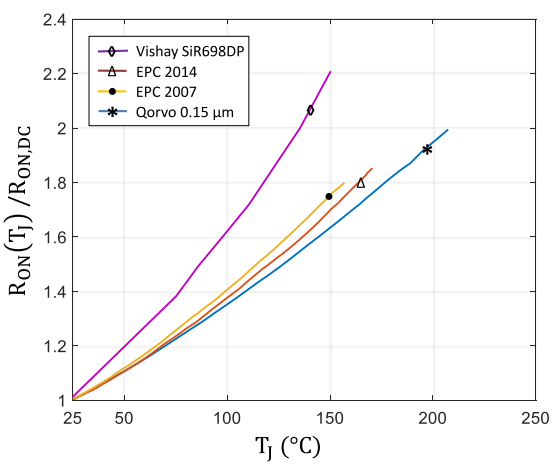

Fig. 8. Normalized R_{ON} versus junction temperature T_J for the considered DUTs.

The results of this characterization are reported in Fig. 7. In order to highlight the variation due to the junction temperature and allow a comparison between the considered DUTs, each $R_{ON}(T_J)$ has been normalized to the corresponding $R_{ON,DC}$ at 25 °C and the results are plotted in Fig. 8.

The R_{ON} temperature dependence shows a positive temperature coefficient for all the considered devices, as should be expected by their MOSFET-like conduction mechanism [43]. A weak nonlinearity over the tested temperature range is also evident in all the considered DUTs, as also reported in [43]. The normalized increase of R_{ON} for the GaN-on-Si HEMT at 150 °C are 1.75 and 1.7 times their $R_{ON,DC}$ at 25 °C, while the Si MOSFET at 150 °C shows an increase up to 2.2 times its $R_{ON,DC}$ at 25 °C. Almost coincident results are provided by the vendor in the datasheets of the EPC 2014, EPC 2007, and SiR698DP [34], [35], [41], [43]. Very similar results are also reported in [22] for normally-OFF GaN-ON-Si devices in which the normalized increase of the resistance at 150 °C is between 1.56 and 1.73 times with respect to their $R_{ON,DC}$ at 25 °C (= 150 and 65 mΩ, respectively).

As expected, the R_{ON} temperature sensitivity is higher in the Si MOSFET compared to the GaN devices [43]. Between the GaN devices, the R_{ON} temperature sensitivity is also slightly higher in the DUTs with the Si substrate compared to the SiC substrate. It is fair to notice that this is not in contrast with the well-known nonlinear behavior of SiC thermal resistance [27], since the measurement in Fig. 7 are performed at controlled T_J with negligible power dissipation. If the same devices were

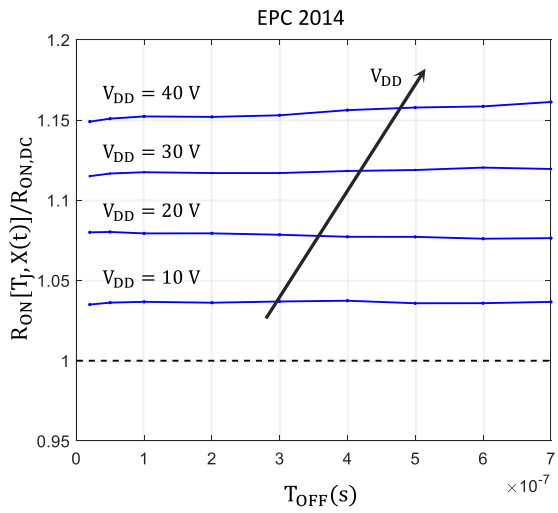

Fig. 9. Measured R_{ON} after different voltage stresses pulse lengths T_{OFF} in the EPC 2014 starting from 20 ns up to 700 ns.

operated at fixed base plate temperature with nonnegligible power dissipation, the nonlinearity of the SiC thermal resistance would contribute to the device channel heating and thus the R_{ON} of GaN-on-SiC devices would have an higher degradation rate at increasing base plate temperature.

B. Dependence of the R_{ON} on T_J and on X(t)

In this section, the R_{ON} dependence on the thermal-state T_J and on the trapped-charge state $X(t)$ is investigated and the complete switch model (6) will be considered.

Due to short current pulses, and low duty cycles, the DUT R_{ON} characterization is carried out with negligible dissipated power and thus in the same iso-thermal conditions described in Section IV-A that ensure $T_J \approx T_C$.

This time, the DUT R_{ON} is measured (i.e., V_{DS} and I_{DS} sensing) right after its commutation from the OFF-state V_{DD} (synthetized with the high-side switch of the half-bridge) to full conduction (see example waveforms in Figs. 16 and 17 in the Appendix).

Due to the very fast charge capture time-constants of GaN HEMT technology [24]–[26], an OFF-state voltage pulse duration $T_{\mathrm{OFF}} = 100$ ns can be considered long enough to activate fast charge capture mechanisms. This has also been experimentally verified on the EPC 2014 with the results shown in Fig. 9. In such experiment, the R_{ON} has been measured immediately after ($t_D = 2\,\mu$s) an OFF-state voltage stress of different V_{DD} amplitudes and at different T_{OFF} pulse lengths. The R_{ON} shows a substantial independence from the duration of the voltage stress between 20 and 700 ns. Therefore, a V_{DD} pulse length $T_{\mathrm{OFF}} = 100$ ns has been selected for the characterization.

The iso-thermal R_{ON} at different OFF-state voltages V_{DD} and T_{ON} are reported in Fig. 10 for two of the considered DUTs (Qorvo 0.15 μm and EPC 2014). After the DUT switching, the R_{ON} is sampled by the setup at a variable time T_{ON} from the voltage stress, enabling the observation of the $R_{\mathrm{ON}}[T_J, X(t)]$ evolution due to trap release.

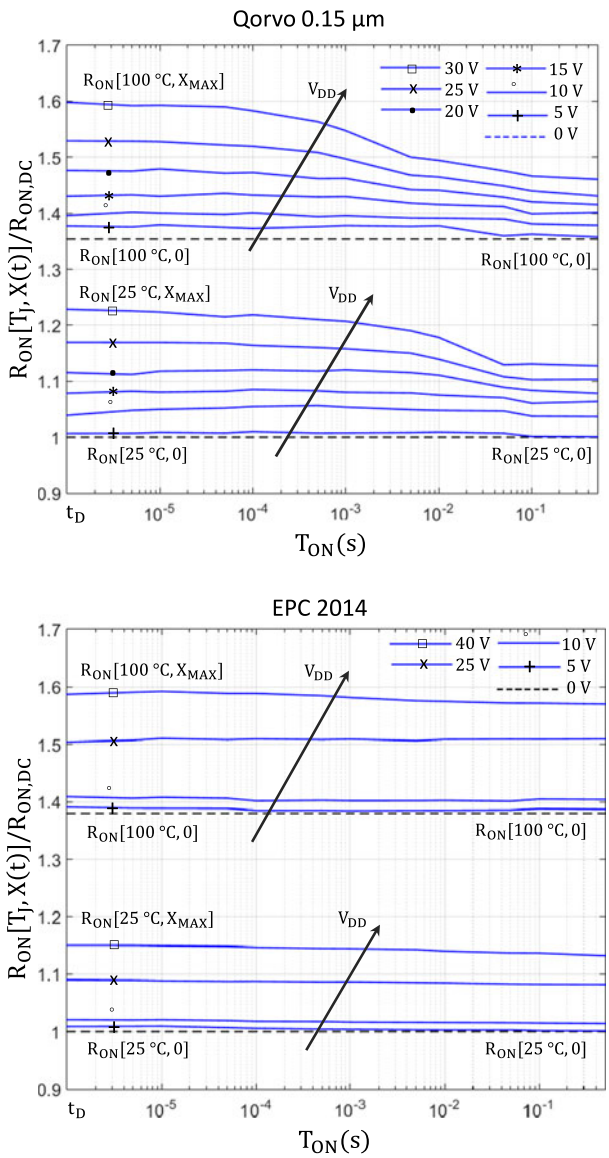

Fig. 10. Dynamic R_{ON} versus T_{ON} for Qorvo 0.15 μm (up) and for EPC 2014 (down).

The $R_{\mathrm{ON}}[T_J, X_{\mathrm{MAX}}]$ measured after switching from an OFF-state voltage V_{DD} is higher compared to the static value $R_{\mathrm{ON}}[T_J, 0]$, even for an OFF-state voltage as low as $V_{\mathrm{DD}} = 5$ V From voltages higher than $V_{\mathrm{DD}} = 10$ V, R_{ON} starts to increase more significantly, showing a relative increment of about 20% and 14% for the SiC and Si substrate GaN HEMT, respectively, only due to trapping effects (i.e., at a fixed temperature).

Observing the transient of $R_{\mathrm{ON}}[T_J, X(t)]$ for the GaN-on-SiC device, it can be observed that, after the voltage stress, the dynamic R_{ON} is approximately constant for T_{ON} lower than 100 μs: after that time, the device starts to recover likely due to charge releases.

After one second the device is still very far from a complete recovery, especially for higher OFF-state voltages. This is an indication that some relatively "fast" time constants of the detrapping mechanism are present in the range [100 μs $-$ 1 s],

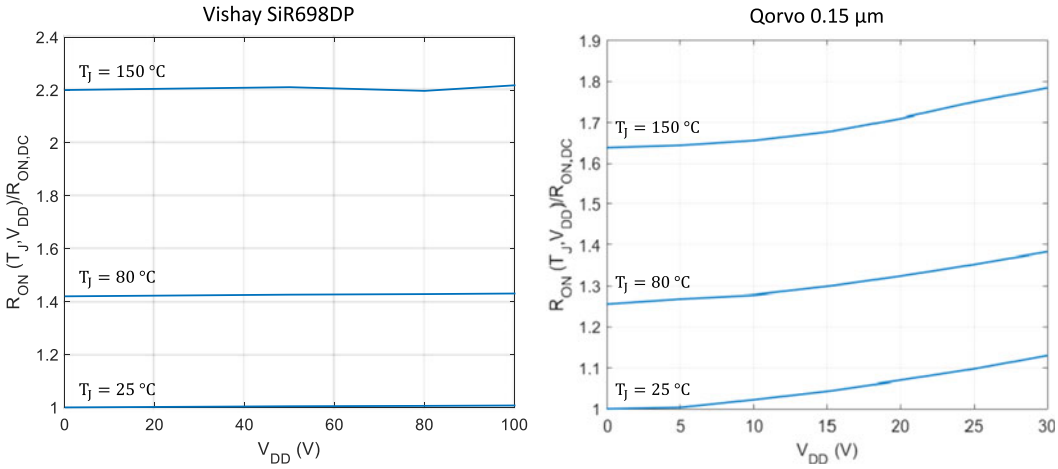

Fig. 11. Measured dynamic R_{ON} versus the drain voltage stress V_{DD}, parametrized at three different T_J junction temperatures (25, 80, and 150 °C) for the DUTs (left: Vishay SiR698DP, right: Qorvo 0.15 μm) at $t_D = 2\,\mu$s.

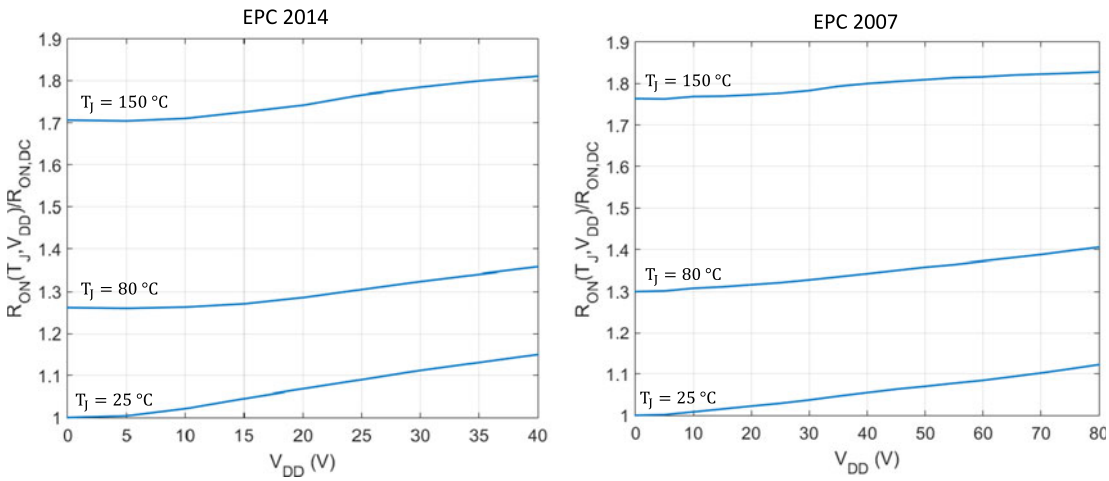

Fig. 12. Measured dynamic R_{ON} versus the drain voltage stress V_{DD}, parametrized at three different T_J junction temperatures (25, 80, and 150 °C) for the DUTs (left: EPC 2014, right: EPC 2007) at $t_D = 2\,\mu$s.

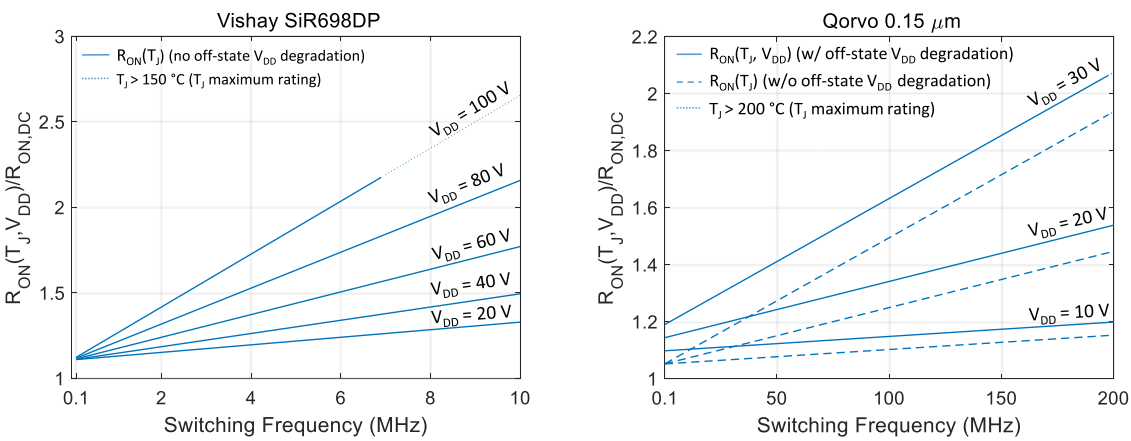

Fig. 13. Predicted dynamic R_{ON} versus the switching frequency, parametrized at some V_{DD} voltage stresses for the Vishay SiR698DP (left) and EPC 2007 (right).

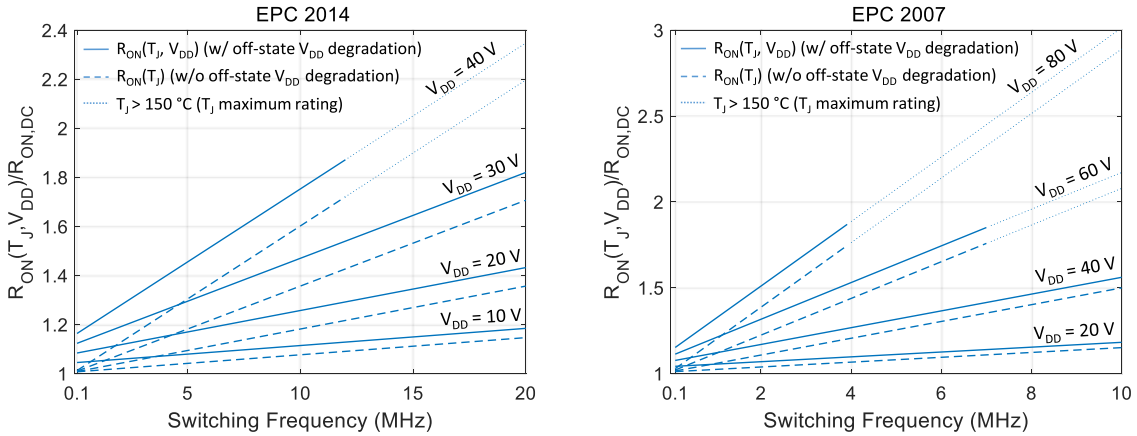

Fig. 14. Predicted dynamic R_{ON} versus the switching frequency, parametrized at some V_{DD} voltage stresses for the EPC 2014 (left) and Qorvo 0.15 μm (right).

while other longer time constants exist for a complete recovery of the device. A comparison between the measured data at 25 and 100 °C (and $V_{\mathrm{DD}} = 30$ V) for the GaN-on-SiC device suggests a temperature dependence of the trap time constants, with R_{ON} that recovers faster at higher junction temperatures. Similar results have also been observed in [16]–[18].

The same observation of the R_{ON} transient for the GaN-on-Si devices reveals almost no recovery in the observation window of 1 s (see Fig. 10), indicating the presence of longer time constants. We verified a complete recovery of both devices between two experiments that took places some hours apart. Though the complete monitoring of the trap recovery transient (hours) can be interesting for a deeper insight and speculation on the trapping/detrapping mechanism as in [16] and [17], it does not have practical interest in actual applications.

C. Dependence of the R_{ON} on T_J and on V_{DD}

Since the PWM switching frequencies of dc/dc converters are typically in the hundreds of kHz or low-MHz range, especially with GaN technology, the R_{ON} of the measured devices does not have time to any degree of recovery: for 100 kHz switching frequency the period is 10 μs, which is largely lower than the observed 100 μs of no-recovery.

The trap-state $X(t)$ of the GaN switch is thus frozen to the maximum value $X(t) = X_{\mathrm{MAX}}$. This value X_{MAX} is set by the operating OFF-state voltage V_{DD} and therefore it is possible to express the R_{ON} dependence directly from the OFF-state voltage V_{DD}

$$V_{\mathrm{DS}} = R_{\mathrm{ON}}\left[T_J, V_{\mathrm{DD}}\right] \cdot I_{\mathrm{DS}}. \tag{10}$$

In Figs. 11 and 12, the R_{ON} with the frozen trap-state, measured at three different junction temperatures (25, 80, and 150 °C) and V_{DD} voltages, are reported for comparison between the considered DUT technologies. The R_{ON} has been measured immediately after the switching event ($t_D = 2\,\mu$s).

The practically constant temperature sensitivity (i.e., spacing between plots at different temperatures) observed for different OFF-stage voltage levels at $t_D = 2\,\mu$s suggests a substantial independence between the trap-assisted and temperature-assisted R_{ON} degradation until the start of detrapping mechanism (as observed, Fig. 10 suggests a temperature dependence of the trap release mechanism). Thus, since no recovery is observed for the initial 100 μs for both technologies, a prediction of the device operating dynamic R_{ON} in any practical application (switching frequencies higher that 1/100 μs = 10 kHz and $T_J < 150$ °C) can be performed by superimposing the measured trap- and temperature-assisted degradation rates.

Following this procedure, in Figs. 13 and 14, the predicted (measurement-based) variation of the normalized dynamic R_{ON} with respect to $R_{\mathrm{ON,DC}}$ at increasing switching frequency and variable OFF-state voltages is shown for all the considered DUTs. The device junction temperature T_J variation due to increasing switching losses is computed using the loss model presented in [8] and by substituting the $R_{\mathrm{ON}} = R_{\mathrm{ON}}[T_J, V_{\mathrm{DD}}]$ values extracted with the proposed technique.

In such model, we assume a rms current $I_{\mathrm{DS,rms}} = 1$ A for all the considered DUTs, and the gate and switching node capacitances reported in Table I. Regarding the thermal network, we assume a worst case scenario in which the thermal junction-to-ambient impedance equates the thermal resistance R_{JA} (see Table I). The dynamic R_{ON} variation reported in Figs. 13 and 14 are only for junction temperatures within the limits of the considered technologies (150 °C for Si, 200 °C for SiC).

Fig. 13 shows the dynamic R_{ON} plot for the considered Si-MOSFET benchmark DUT. Given the resulted insensitivity of this device to V_{DD} voltage stresses (see Fig. 11), the R_{ON} degrades only due to the self-heating caused by the conduction and switching losses. The plots in Figs. 13 and 14 clearly show that, even for well-assessed commercial GaN devices, the degradation of the dynamic R_{ON} is also caused by the R_{ON} degradation due to the OFF-state voltage stress (dashed line versus continuous line).

This degradation cannot be overlooked for a precise computation of the converter conduction losses. High switching frequency converter design would benefit from the availability of such characterization data, rather than typical static R_{ON} values measured at 0 V OFF-state voltage, that can underestimate the conduction losses up to 100% (see Figs. 13 and 14).

VI. Conclusion

In this paper, a novel laboratory setup along with a characterization procedure for the dynamic R_{ON} extraction in presence of thermal- and voltage-stress has been presented. The power switch is directly characterized inside the final circuit half-bridge, which comprises the final application thermal network, PCB parasitics, and driving waveforms for an improved accuracy of the characterization. The presented setup allows the study of R_{ON} transients after the switching event at variable OFF-state voltages stress and operating temperature.

The setup was used for the characterization of a well-established and mature technology of a Si power MOSFET which showed no trap-induced degradation of the R_{ON} and a degradation up to 120% at 150 °C of operative temperature. Furthermore, two different technologies exhibiting state-of-art performance in their fields of applications were tested with the presented setup. For both technologies dynamic R_{ON} degradations up to 75% and 20% are observed for temperature and OFF-state voltage variations, respectively.

By means of these characterization data, it is possible to compute the dynamic R_{ON} at the operating switching frequency of the dc/dc converter, thus allowing an improved estimation of the conduction losses and efficiency. With the considered DUT GaN-on-Si and GaN-on-SiC technologies, an increase up to +100% has been experimentally verified when the devices is pushed to the limit of the switching frequencies and high OFF-state voltage stresses.

Appendix

In this section, explanatory waveforms at the output of the amplification stage are commented showing in detail how the R_{ON} of the DUT is measured by the presented setup.

In the measurement waveforms shown in Fig. 15, the high-side switch is constantly kept OFF, while the DUT (low-side switch) is always ON. No voltage stresses are applied to the DUT. The VCCS injects a 5 μs current pulse in the DUT and the oscilloscope samples the waveforms $V_{\mathrm{OUT}i}$ at the output of the voltage amplifiers. Thus, the $R_{\mathrm{ON}}(T_J)$ is calculated by considering (1)–(5) after the output $V_{\mathrm{OUT}i}$ reach a steady value. These waveforms are representative of the measurements performed in Section V-A.

If the commutation of the high-side switch is introduced imposing the voltage stress V_{DD} to the DUT, the switching node is raised to V_{DD} and thus it is necessary to protect the inputs of the opamps from over-voltages (V_{DD} generally higher than their rail voltage of $V_{\mathrm{RAIL}} = 18$ V).

Transient voltage suppression diodes (TVS, Littelfuse SMAJ5.0) are used to this purpose and the adopted configuration is shown in Fig. 3. The TVS diodes clamp the input nodes of the opamps to 5 V, while the V_{DD} voltage is still applied at the DUT drain. The selected TVS diodes feature a very fast response time (< ps) and their operation is shown in Figs. 16 and 17, which describe the evolution in the time of the measurement system when applying an OFF-state blocking voltage short pulse of amplitude $V_{\mathrm{SW}} = V_{\mathrm{DD}} = 80$ V at $t = 0$.

Within the short voltage pulse ($V_{\mathrm{SW}} = 80$ V, not shown in the plots), the input of the opamp is clamped to 5 V by the TVS

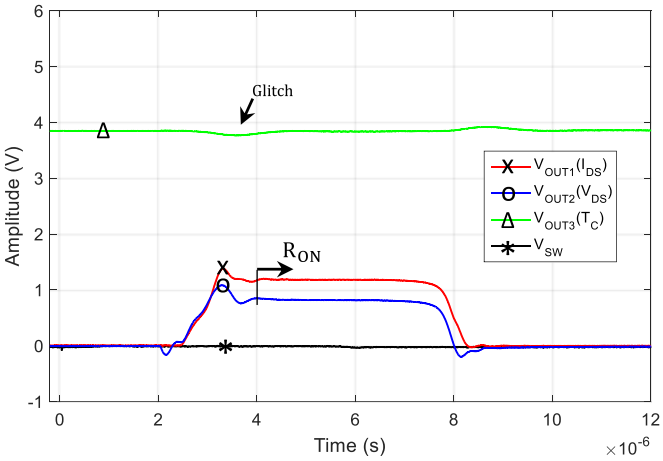

Fig. 15. Amplifiers response acquired by the oscilloscope to a 5 μs I_{CS} current injection with $V_{\mathrm{DD}} = 0$ V. The R_{ON} measurement becomes valid when V_{OUT1} and V_{OUT2} have settled down. The temperature measurement is performed on V_{OUT3}.

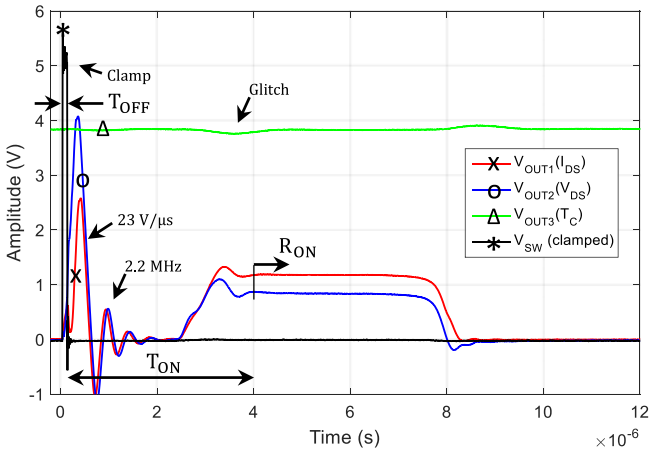

Fig. 16. Amplifiers response to a 100 ns OFF-state voltage pulse and to a measurement current injection after $T_{\mathrm{ON}} = 4\,\mu$s. Traps in the DUT are set with the OFF-state voltage pulse at $V_{\mathrm{DD}} = 80$ V without causing damage to the opamps by clamping their inputs to 5 V.

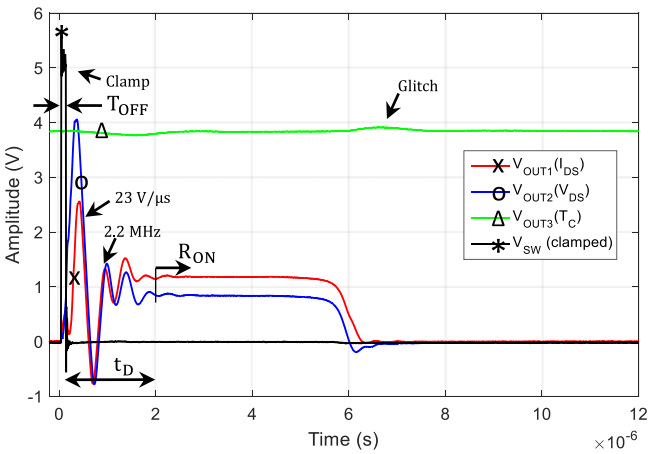

Fig. 17. Amplifiers response to a 100 ns prepulse and to a measurement current injection immediately after the voltage stress. The R_{ON} measurement is performed after $t_D = 2\,\mu$s from the voltage stress to let the ringing (2.2 MHz) settled down.

(waveform V_{SW} in Figs. 16 and 17). At the instant $t = T_{\mathrm{OFF}}$, the high-side switch is turned OFF and the DUT is turned ON after a minimal dead-time.

The TVS diodes provide electrical protection of the opamps, but do not prevent their saturation (they saturate for an input at $V_{\mathrm{RAIL}}/\mathrm{Gain} = 18/20 = 0.9$ V). Saturation should be avoided, since the opamp can require very long time to recover from this overdrive condition [32]. During the opamp overdrive recovery time, R_{ON} is not observable by the setup. In the proposed setup, the saturation of the opamps is avoided by limiting the T_{ON} pulse width of the high-side device. As can be appreciated in Figs. 16 and 17, when the high-side switch is ON (OFF-state voltage $V_{\mathrm{DS}} \cong V_{\mathrm{DD}}$), both the outputs V_{OUT1} and V_{OUT2} of the voltage amplifiers are slewing and, if T_{OFF} is short enough, they do not saturate at 18 V and slew down to 0 V when the V_{DD} voltage pulse is removed.

A slew-rate of 23 $\mathrm{V}/\mu\mathrm{s}$ has been experimentally verified at the outputs of the AD797 opamps which sets a maximum T_{OFF} of: 1 μs $\cdot$ 18 V/23 V μs without incurring in the saturation condition.

It is useful to notice that a short V_{DD} pulse width of hundreds of ns that avoid saturation of the opamp is still suitable to observe the trap-assisted degradation of R_{ON}, since the trap activation mechanism in GaN is extremely fast as it is experimentally verified in Fig. 9 and in [24]–[26].

However, even without saturating, the response of the amplifiers to a 100 ns OFF-state voltage pulse shows some ringing (2.2 MHz), which requires 2 μs to settle down (see Fig. 16). It is worth to point out, that this settling time is independent from the amplitude of the OFF-state V_{DD} pulse, since the opamp dynamic response (ringing) always starts from the same condition (5 V input clamping) for a $T_{\mathrm{OFF}} = 100$ ns.

In Fig. 16, the 2 μs needed for the stabilization of V_{OUT1} and V_{OUT2} are awaited before applying the current measurement pulse: as a result, the 2-μs duration of the current injection transient is added to the 2 μs of the postcommutation settling time and the delay time (t_D) between the switching event and the start of an accurate acquisition of waveforms (i.e., R_{ON} evolution) is about 4 μs.

Fig. 17 shows the strategy that we adopted for a further minimization of t_D: the measuring current pulse command V_{CS} is set just after the commutation from the OFF-state voltage stress. In this way the transients associated with the two events (voltage and current pulse) share the same time slot and the system is ready for a clear measure after a delay time of 2 μs.

This short time delay is in line with the results obtained by applying clamping circuit as in [15] and [19]. Some papers report also time delay below 1 μs, but in many cases the proposed measuring plots clearly show that the measure is still not reliable (clear ringing behavior) in the immediate proximity of the switching event, and become totally settled after 1 μs [15], [20]. Moreover the typical long time constants associated to trap release mechanism in GaN HEMT [19] do not probably require an observable starting time shorter than 2 μs as it is also shown in the presented measurements.

Acknowledgment

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References

[1] F. C. Lee and Q. Li, "High-frequency integrated point-of-load converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

[2] J. Millan, Member, P. Godignon, X. Perpina, A. Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[3] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC–DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151–5158, Sep. 2015.

[4] D. Costinett, H. Nguyen, R. Zane, and D. Maksimovic, "GaN-FET based dual active bridge DC-DC converter," in *Proc. IEEE 26th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2011, pp. 1425–1432.

[5] M. J. Scott, K. Zou, J. Wang, C. Chen, M. Su, and L. Chen, "A gallium nitride switched-capacitor circuit using synchronous rectification," *IEEE Trans. Ind. Electron.* vol. 49, no. 3, pp. 1383–1391, May/Jun. 2013.

[6] M. Chen, K. K. Afridi, S. Chakraborty, and D. J. Perreault, "A high-power-density wide-input-voltage-range isolated Dc-Dc converter having a multitrack architecture," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 2017–2026.

[7] S. Shinjo, Y.-P. Hong, H. Gheidi, D. Kimball, and P. Asbeck, "High speed, high analog bandwidth buck converter using GaN HEMTs for envelope tracking power amplifier applications," in *Proc. IEEE Wireless Sens. Sens. Netw.*, Jan. 2013, pp. 13–15.

[8] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High-frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462–2473, May 2014.

[9] P. F. Miaja, A. Rodrıguez, and J. Sebastian, "Buck-derived converters based on gallium nitride devices for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2084–2095, Apr. 2015.

[10] Y. Zhang, M. Rodriguez, and D. Maksimovic, "Very high frequency PWM buck converters using monolithic GaN half-bridge power stages with integrated gate drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7926–7942, Nov. 2016.

[11] A. Sepahvand, P. Momenroodaki, Y. Zhang, Z. Popovic, and D. Maksimovic, "Monolithic multi-level GaN converter for envelope tracking in RF power amplifiers," in *Proc. IEEE Energy Convers. Congr. Expo. Dig.*, Sep. 2016, pp. 1–7.

[12] F. Raab *et al.*, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[13] C. Florian, T. Cappello, R. P. Paganelli, D. Niessen, and F. Filicori, "Envelope tracking of an RF high power amplifier with an 8-level digitally controlled GaN-on-Si supply modulator," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 8, pp. 2589–2602, Aug. 2015.

[14] C. Florian, T. Cappello, D. Niessen, R. P. Paganelli, S. Schafer, and Z. Popovic, "Efficient programmable pulse shaping for X-band GaN MMIC radar power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 3, pp. 881–891, Mar. 2017.

[15] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of dynamic on-resistance in GaN transistors under soft- and hard-switching contitions," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, Oct. 2011, pp. 1–4.

[16] D. Jin and J. A. Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, Jun. 2012, pp. 333–336.

[17] D. Jin and J. A. Alamo, "Methodology for the study of dynamic ON-resistance in high-voltage GaN field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3190–3196, Oct. 2013.

[18] H. Huang, Y. C. Liang, G. S. Samudra, T-F. Chang, and C-F. Huang, "Effects of gate field plates on the surface state related current collapse in AlGaN/GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2164–2173, May 2014.

[19] M. Meneghini *et al.*, "Trapping and reliability assessment in D-mode GaN-based MIS-HEMTs for power applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2199–2206, May 2014.
[20] N. Badawi and S. Dieckerhoff, "A new method for dynamic ron extraction of GaN power HEMTs," in *Proc. IEEE Int. Exhib. Conf. Power Electr. Intell. Motion, Renew. Energy Energy Manag.*, May 2015, pp. 1–6.
[21] R. Gelagaev, P. Jacqmaer, and J. Driesen, "A fast voltage clamp circuit for the accurate measurement of the dynamic ON-resistance of power transistors," *IEEE Trans. Ind. Electron.* vol. 62, no. 2, pp. 1241–1250, Feb. 2015.
[22] N. Badawi, J. Böcker, O. Hilt, E. Bahat-Treidel, J. Würfl, and S. Dieckerhoff, "Investigation of the dynamic on-state resistance of 600 V normally-off and normally-on GaN HEMTs," *IEEE Trans. Ind. Appl.* vol. 52, no. 6, pp. 4955–4964, Nov./Dec. 2016.
[23] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON degradation and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017.
[24] O. Jardel *et al.*, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2660–2669, Dec. 2007.
[25] A. Santarelli *et al.*, "A double-pulse technique for the dynamic characterization of GaN FETs," *IEEE Microw. Compon. Lett.*, vol. 24, no. 2, pp. 132–134, Feb. 2014.
[26] C. Florian, D. Niessen, T. Cappello, A. Santarelli, F. Filicori, and Z. Popovic, "Pre-pulsing characterization of GaN PAs with dynamic supply," in *Proc. IEEE MTT-S Int. Microw. Symp.*, May 2016, pp. 1–4.
[27] C. Florian, A. Santarelli, R. Cignani, and F. Filicori, "Characterization of the nonlinear thermal resistance and pulsed thermal dynamic behavior of AlGaN–GaN HEMTs on SiC," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1879–1891, May 2013.
[28] Keysight, A. Wadsworth. (2014). Fundamentals of Fast Pulsed IV Measurements. [Online]. Available: http://www.keysight.com/upload/cmc_upload/All/9Feb14Slides.pdf
[29] AMCAD. (2016). Pulse IV System AM3200 Serie 3. [Online]. Available: http://www.amcad-engineering.com/assets/piv3200_brochure_rev4.pdf
[30] Keysight. Pulsed IV/RF Measurements for Compact Model Extraction. [Online]. Available: http://www.keysight.com/upload/cmc_upload/All/2_Pulsed_IV_RF_Measurements_for_Compact_Model_Extraction.pdf
[31] T. C. Carusone, D. A. Johns, and K. W. Martins, "Basic current mirrors and single stage amplifiers," in *Analog Integrated Circuit Design*, 2nd ed., Hoboken, NJ, USA: Wiley, 2012, pp. 131–135.
[32] Analog Devices. (2009). Using Op Amps As Comparators. [Online]. Available: http://www.analog.com/media/en/training-seminars/tutorials/MT-084.pdf
[33] EPC. (2016). Efficient Power Conversion Corporation Website. [Online]. Available: http://epc-co.com/epc/
[34] EPC. (2015, Sep.). EPC2014—Enhancement Mode Power Transistor. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2014_datasheet.pdf
[35] EPC. (2015, Jan.). EPC2007—Enhancement Mode Power Transistor. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2007_datasheet.pdf
[36] EPC. (2016). Development Board EPC9006 rev. 3.0 Quick Start Guide. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/guides/EPC9006_qsg.pdf
[37] Qorvo. (2016, Mar.). Field-Proven GaN Solutions from Qorvo. [Online]. Available: http://www.qorvo.com/docs/brochures/qorvo-field-proven-gan-solutions.pdf
[38] Y. Zhang, M. Rodriguez, and D. Maksimovic, "100 MHz, 20 V, 90% efficient synchronous buck converter with integrated gate driver," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2014, pp. 3664–3671.
[39] Auriga Microwave. (2013). Pulsed Measurement Theory of Operation. [Online]. Available: http://www.mrc-gigacomp.com/pdfs/AU4850_AppNote-PulseTheory.pdf
[40] Texas Instruments. (2016, Jan.). LM5113 100 V 1.2-A / 5-A, Half-Bridge Gate Driver for Enhancement Mode GaN FETs. [Online]. Available: http://www.ti.com/lit/ds/symlink/lm5113.pdf
[41] Vishay. (2011, Dec.). N-Channel 100 V (D-S) MOSFET. [Online]. Available: http://www.vishay.com/docs/67918/sir698dp.pdf
[42] Microchip. (2013, Nov.). MIC4605 Evaluation Board. [Online]. Available: http://ww1.microchip.com/downloads/en/DeviceDoc/MIC4605-1YM%20Evaluation%20Board%20User%20Guide.pdf
[43] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, "GaN transistor electrical characteristics," in *GaN Transistors for Efficient Power Conversion*, 2nd ed., West Sussex, U.K.: Wiley, 2015, ch. 2, sec. 2.2.2, pp. 24–26.

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