A 32 mV/69 mV input voltage booster based on a piezoelectric transformer for energy harvesting applications

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A 32 mV/69 mV Input Voltage Booster based on a Piezoelectric Transformer for Energy Harvesting Applications

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Abstract:

This paper presents a novel method for battery-less circuit start-up from ultra-low voltage energy harvesting sources. The approach proposes for the first time the use of a Piezoelectric Transformer (PT) as the key component of a step-up oscillator. The proposed oscillator circuit is first modelled from a theoretical point of view and then validated experimentally with a commercial PT. The minimum achieved start-up voltage is about 69 mV, with no need for any external magnetic component. Hence, the presented system is compatible with the typical output voltages of thermoelectric generators (TEGs). Oscillation is achieved through a positive feedback coupling the PT with an inverter stage made up of JFETs. All the used components are in perspective compatible with microelectronic and MEMS technologies. In addition, in case the use of a ~40 μH inductor is acceptable, the minimum start-up voltage becomes as low as about 32 mV.

Highlights:

- We use for the first time a piezoelectric transformer for ultra-low voltage step-up purposes
- The mathematical model of the system is verified by experimental measurements.
- We achieve a start-up voltage of 69 mV without magnetic components

Keywords:

Energy autonomous systems, energy harvesting, JFET circuits, Piezoelectric transformers, power management, step-up oscillators, ultra-low voltage.

1. Introduction

Dimension scaling in CMOS technologies has allowed a continuous reduction of the energy required by circuits for performing given tasks [1], which is an essential aspect for extending life of mobile, wearable, implantable devices supplied by electrochemical or biofuel cells [2] [3]. Although there is this relentless progress of technology, battery replacement would require a large maintenance effort if ubiquitous sensor networks or pervasive implantable sensors were deployed. It would be very useful if such systems could be fully autonomous by harvesting the energy available in the environment in several forms, e.g. light, heat, vibrations, etc. A great challenge is to exploit the often very low output voltage provided by energy harvesting transducers, and to boost it to a sufficient level (at least 0.6-0.8V) above the threshold voltage of semiconductor devices, so that a switching converter can be successfully activated. To cite an example, thermoelectric generators (TEGs) generally provide an output voltage of few tens of mV/K [4], whereas indoor solar cells can output down to 200mV in low illumination conditions [5]. These values are not sufficient to efficiently control the gate of power devices in switching DC/DC converters, or to exceed the diode threshold voltage in voltage multipliers, e.g. Greinacher topologies, which also require a transistor oscillator for operating. Currently, many works in literature presenting power converter circuits for low voltage energy harvesting applications do not face the problem of battery-less start-up, and require a supply voltage much higher than that available from the source: e.g. in [6] and [7] few tens of mV can be exploited, but an initial amount energy (pre-charged capacitor or battery) is necessary for power conversion.

A first approach to boost ultra-low voltages consists in the use of capacitive charge pumps, as in [8] [9]. Although specific circuit techniques [10] [11] can improve the performance, the activation voltage is still comparable with the threshold voltage of the FETs, and thus relatively high for handling TEGs. With threshold voltage adjustments the minimum activation voltage can be as low as 95 mV [12]. Another technique, with a limited applicability, is the use of a motion-activated switch to initially drive a boost converter [13], which allows input voltages down to 35 mV. Furthermore, very low activation voltages are provided by step-up oscillators based on magnetic transformers (MTs), a circuit topology known for long [14], and now used in commercial products [15]. In this type of circuits (**Fig. 1**), an amplifier stage based on a low threshold voltage FET is coupled on a feedback loop integrating a magnetic transformer. The amplifier should achieve a sufficient transconductance in order to start oscillation when biased by the low-voltage source. Once oscillation is started, a conventional passive voltage multiplier further boosts and rectifies voltage. Cascading multiple MTs [16] can further decrease the minimum start-up voltage at the expenses of system dimensions. In addition, the MT can also be re-used in a conventional DC/DC converter after start-up [17]. The main drawback of this approach is that MTs are difficult to shrink, since a high turn ratio is required for managing TEGs. In addition, MTs suffer from frequency limitations, core losses and saturation [18].

Generally, micro-fabricated magnetic transformers (MTs) are used for signal or power isolation [19] and not for step-up purposes, thus they have generally low turns ratio (generally 1-2), low gains (lower than 0 dB) and low magnetizing inductances (lower than 1μH). However, miniaturized MTs based on bonding wires [20] for step-up purposes [21] have been recently reported. In these cases, the constraints imposed by miniaturization significantly limit the quality factors. As an alternative, transformers based on silicon micro-mechanical resonators and piezoelectric materials have been already proposed [22], thus smoothing the way towards package-level integration of mixed microelectronic and MEMS systems. In general, energy conversion in piezoelectric transformers (PTs) is much more efficient than in MTs, because of the higher quality factors. This is mainly due to the low mechanical losses in MEMS oscillators. In fact, the quality factors (Q) of piezo-ceramics may be greater than 1000 [23].

This paper presents a novel battery-less step-up oscillator based on a piezoelectric transformer (PT), useful for kick-

starting, from fully discharged states, an efficient power conversion system based on TEGs subject to low temperature gradients (**Fig. 2**). The paper extends the results presented in a previous conference paper [24]. The purpose of the circuit is to initially provide a sufficient voltage for starting an external self-sustaining efficient power converter. Then, our main target is to achieve a very low start-up voltage, and not necessarily efficiency. To the best of our knowledge, for the first time this topology is exploited for these purposes, whereas similar applications in literature mainly rely on MTs or LC oscillators. We point out that the circuit is compatible with an inductor-less implementation. In perspective, the system is compatible with microelectronic and MEMS implementations integrated at package level. Additionally, it will be shown that lower start-up voltages can be achieved through the insertion of a tiny inductor in the input stage. In our specific implementation, which is based on a commercial PT designed for Cold Cathode Fluorescent Lamps (CCFL) or Liquid Crystals Displays (LCD) backlight, the system can pump voltages as low as tens of mV up to voltage levels suitable to control the power devices of a DC/DC converter.

2. Piezoelectric transformers and equivalent electromechanical circuit

The main purpose of this section is to briefly summarize the operation of the PT and to recall the equivalent electromechanical circuit used in circuit analysis.

2.1. *Piezoelectric transformers*

Piezoelectric transformers are resonant devices that exploit the direct and inverse piezoelectric effect of certain materials, e.g. PZT (Lead Zirconate Titanate), AlN (Aluminum Nitride) or ZnO (Zinc Oxide), that produce polarization charge on their electrodes when subject to a mechanical stress. A typical PT such as the step-up Rosen transformer [25], is built by coupling a transverse mode actuator at primary side (i.e. stress perpendicular to electric field and polarization) with a longitudinal mode transducer [26] at secondary side (i.e. stress parallel to electric field and polarization): when PTs are driven at a frequency near their resonance, an acoustic standing wave is produced with the generation of nodes and antinodes, so that a lumped electromechanical equivalent circuit [27] can be adopted. **Fig. 3** represents the equivalent circuit of a PT driven in proximity of a particular resonant frequency: C_{d1} is the input electrical capacitance, and in multi-layer transformers it is the sum of the capacitance of each input layer; the series of C_M, L_M and R_M represents the mechanical branch; N is the equivalent turn ratio related to the stress ratio from input to output; and C_{d2} is the output electrical capacitance, which, for discrete PTs, is generally several orders of magnitude lower than C_{d1} because the distance between the electrodes is higher and the number of electrodes is lower, typically two.

PTs are very load-dependent devices [28], and their electrical resonance never coincides with the mechanical resonance. Then, a vibrating force that causes the maximum displacement at a certain frequency will not generate the maximum output voltage, not even in an open circuit configuration because of the intrinsic output capacitor C_{d2}. If we consider the input impedance $Y_{IN}(\omega)$ of a piezoelectric device, the resonance frequency f_S is very close to the frequency f_r where $\mathrm{Im}\{Y_{IN}(\omega)\} = 0$, and to the frequency f_M where $|Y_{IN}(\omega)|$ is maximum. These three frequencies are not clearly distinguished in a Bode plot [29]. Furthermore, manufacturers usually insert PTs in a plastic case that becomes part of the resonant system, with rubber supports that allow the PT to vibrate regardless of the mounting. Then, the best way to choose a particular resonant mode without theoretically affecting performance [30] is to mechanically clamp a node.

2.2. *Identification of the electro-mechanical equivalent circuit*

To better predict device and circuit behaviour, a characterization of the PT electro-mechanical parameters is necessary,

because the actual behaviour may slightly differ from what the manufacturers state. Some methods for experimentally identifying the PT parameters have been developed both in time domain [31] and frequency domain [32]. Time domain methods rely on measuring decay time constants and the natural resonance frequency, and require standard equipment such as signal generators and oscilloscopes [31]. The frequency domain measurements are usually based on the admittance circle [32], and the only necessary instrument is an LCR meter. Admittance circle measurements basically rely on the similarity of a PT to the Butterworth-Van Dyke equivalent circuit for the quartz, when the PT input or output terminals are shorted. For a quartz crystal, plotting $\mathrm{Im}\{Y_{IN}(\omega)\}$ vs. $\mathrm{Re}\{Y_{IN}(\omega)\}$ yields to a circle. This means that we can adopt for PTs the same definitions used for quartz (e.g. resonance frequency, antiresonance frequency, etc.)
Table I reports the parameters obtained with the admittance circle method for the second mode of the adopted PT sample (SMMTF55P4S80 PT from Steiner & Martins Piezo**)** through an Agilent E4980A LCR meter, along with other characteristic parameters of the system.

According to the model in **Fig. 3**, for an unloaded PT the electric resonance frequency is:

$$f_S = \frac{1}{2\pi\sqrt{L_M C_{eq}}}, \qquad (1)$$

where $C_{eq}=C_M\cdot(N^2C_{d2})/(C_M+N^2C_{d2})$. The antiresonance frequency (or parallel resonance) is:

$$f_P = \frac{1}{2\pi\sqrt{L_M C_{eq2}}}, \qquad (2)$$

where $C_{eq2}=C_{eq}\cdot C_{d1}/(C_{eq}+C_{d1})$.
If the PT is loaded with a capacitor, in (1) and (2), the capacitance C_{d2} should take into account the total equivalent capacitance at the PT's output port.

3. Circuit schematic and behaviour

The schematic of the proposed start-up circuit is shown in **Fig. 4**. We can distinguish three different sections apart from the low voltage source, which in our case is a TEG source. The first part is a common source (CS) stage made of $(n + m)$ n-channel JFETs (MMBFJ201 from Fairchild Semiconductors) working in deep-triode (linear) region. The second part is the PT, and the third part is a voltage doubler made up of a 0.47 nF pump capacitor C_{PUMP}, BAS70 Schottky diodes $D_{1,2}$, and a 4.7 µF low-leakage storage capacitor C_{STORE}. The JFETs J_A and J_L are conductive even when their drain to source voltage is few tens of millivolts. The resistor R_F (≈ 140 MΩ) is required for draining part of the current at the output port of the PT, because if the amplitude of oscillations at node B exceeds ~0.5 V, the gate-source p-n junction of J_A will partially turn on causing the gate to lose its control over the channel, and consequently the transistor effect will be lost. R_F is also required to eliminate any possible bias charge on the gate capacitance of J_A that may cause the transistor to be completely off. At the same time, R_F has to be sufficiently high in order not to produce load effects at the PT output port, and not to decrease its voltage step-up ratio. The resistor R_T models the equivalent internal series resistance of the low voltage source V_{IN}. Only at the beginning of the oscillation, when node B is around 0 V, the load effect of the voltage doubler can be considered as a linear impedance. It is mainly caused by the intrinsic capacitances $C_{SCHOTTKY}$ of the Schottky diodes (less than 3pF/diode) because the parallel differential resistance of the diodes (≈ 10 MΩ), C_{PUMP}, and C_{STORE} present higher impedance at the frequency of interest. Hence, the series connection of more Schottky diodes reduces the load effects at the PT output port. In our implementation each Schottky diode in **Fig. 4** represents the series connection of four diodes: this configuration affects slightly the steady-state voltage

at C_{STORE}; however, thanks to the low currents involved (generally less than 100 nA), the voltage drop caused by each diode is perceptibly less than 100 mV, so the number of series diodes comes from a trade-off between minimum activation voltage and steady-state output voltage. It is worth to mention that, when oscillation is in a steady state, small signal analysis is not valid anymore because of the significant nonlinearities of rectifier diodes. **Fig. 4** also depicts the theoretical waveforms involved in the system: as soon as V_{IN} reaches the minimum activation voltage $V_{IN,MIN}$ that satisfies the Barkhausen gain criterion, an oscillation is triggered and the voltage doubler rectifies the amplified oscillation at the PT output port. Before the beginning of the oscillation, V_A follows V_{IN} with a scaling factor due to the voltage divider composed by the n amplifier JFETs (nJ$_A$) and the m load JFETs (mJ$_L$), whereas during oscillation, V_B is in opposition of phase with respect to V_A. The steady-state DC voltage of V_B depends on the type of transistor used in the CS stage. In case of JFETs, this DC voltage is lower than 0 V, because the system oscillates only if the gate-source p-n junction of the JFETs is not forward biased; in case of depletion MOSFET, this DC value is close to 0 V. V_{OUT} starts growing exponentially until the oscillation at node B reaches steady-state. After this, V_{OUT} follows the typical charging law of an RC circuit.

In order to determine the oscillation condition, it is useful to perform a small-signal analysis. In the initial condition, the DC voltage V_A depends on the number of amplifier and load JFETs, respectively n and m: $V_A = m / (n + m) \cdot V_{IN}$. It can be found out that the transconductance g_{mA} of each amplifier JFET is: $g_{mA} = \beta_n V_A = g_m \cdot m / (n + m)$, where $g_m = \beta_n V_{IN}$ is assumed as a reference value, and β_n is the gain factor of the JFET. For JFETs it holds that $\beta_n = 2I_{DSS} / V_P^2$, where I_{DSS} is the drain current at zero gate voltage and V_P is the negative pinch-off voltage. The transconductance g_{mL} of each load JFET is: $g_{mL} = \beta_n(V_{IN} - V_A) = g_m \cdot n / (n + m)$. The output conductance g_{dsA} of each amplifier JFET is $g_{dsA} = \beta_n (-V_P - V_A) \cong -\beta_n V_P$, under the reasonable assumption that $|V_P| >> V_{IN}$ in this application. The output conductance g_{dsL} of each load JFET is: $g_{dsL} = \beta_n (-V_P - V_{IN}) \cong -\beta_n V_P$. Then a unique symbol g_{ds}, defined as $g_{ds} = g_{dsA} = g_{dsL}$, can then be used. Furthermore, all the JFETs are assumed to work in deep triode region, hence, the small signal output conductance g_{ds} equals the large signal conductance G_{DS} of each device. Under the above assumption, it also holds that $g_{dsA,L} >> g_{mA,L}$. Then, the unloaded voltage gain A_{Vcs0} of the input stage with n parallel amplifier JFETs and m parallel load JFETs can be expressed as:

$$A_{Vcs0} = -\frac{n g_{mA}}{m g_{mL} + n g_{dsA} + m g_{dsL}} \cong -\frac{n g_{mA}}{(n+m) g_{ds}} = -\frac{n\,m}{(n+m)^2}\frac{g_m}{g_{ds}} = -\frac{n\,m}{(n+m)^2}\frac{V_{IN}}{|V_P|} \qquad (3)$$

In (3) the effect of R_T (typically few Ω in TEGs) is neglected, because it is generally significantly lower than the typical output resistance $1/G_{DS}$ of the load JFETs. In addition, at large signals, R_T does not affect perceptibly the differential parameters. From (3), it also descends that the maximum unloaded gain occurs when $n = m$.

The gain A_{VCS} of the loaded input stage can be calculated by considering that the input impedance $Z_{PT}(s)$ of the PT, which is loaded with the gate capacitance of the n amplifier JFETs, is connected in parallel to the output:

$$A_{VCS} \cong -\frac{n g_{m1}}{(n+m) g_{ds} + 1/Z_{PT}(s)} = A_{VCS0} \cdot \frac{Z_{PT}(s)}{r_{out} + Z_{PT}(s)} = A_{VCS0} A_L(s), \qquad (4)$$

where $1/r_{out} = (n + m)\, g_{ds}$, and $A_L(s)$ is the fractional term in the above expression.

The total capacitance C_{OUT} at the output port of the PT is $C_{OUT} = C_{d2} + n \cdot C_G + C_{VD}$, where C_{VD} is the total small-signal capacitance associated to the voltage doubler, and C_G is the overall input capacitance of a single amplifier JFET. C_G is the sum of the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD} because of the Miller effect. C_{OUT} can be equivalently brought into the primary section with a scaling factor N^2 and the ideal transformer can be substituted by a voltage controlled voltage source of gain equal to N. Then, the voltage gain of the PT is:

$$A_{VPT}(s) = \frac{C_{eq}}{NC_{out}(s^2 L_M C_{eq} + sR_M C_{eq} + 1)}, \qquad (5)$$

where $C_{eq} = N^2 C_{OUT} C_M / (N^2 C_{OUT} + C_M)$. The total loop gain A_{VT} is the product of the gain A_{VPT} and the gain A_{Vcs}. The Bode plots of the above mentioned voltage gains are depicted in **Fig. 5**.

The Barkhausen phase criterion requires a total phase shift of 360° around the loop to achieve a possible oscillation, and the unloaded input stage provides an initial phase shift of 180° (see (3)). From the point of view of its transfer function $A_{VPT}(s)$, the PT behaves like a second order system (see (5)): in a very small neighbourhood of the anti-resonance frequency f_P its phase shift is slightly less than 180° due to its very high Q factor. The residual few degrees to reach 360° are determined by $A_L(s)$ in (4), which introduces a negative phase shift of few degrees at a frequency extremely close to f_P. In order to determine the oscillation frequency f_{OSC}, it can be observed in **Fig. 5** that in proximity of f_P, the phase of the loop gain A_L shows an extremely steep slope: for the adopted sample the phase shift is about 0.21°/Hz around anti-resonance f_P, which occurs beyond 100 kHz in the adopted PT. At f_P the phase shift of A_{VPT}, from simulations, is about 178°. In order to reach 180°, the residual degrees are provided by A_L. Hence, the 360° required by the Barkhausen phase criterion do not occur precisely at f_P. It can be verified numerically that f_P and f_{OSC} are shifted by (180 – 178)°/ (0.21°/Hz) = 10 Hz. For this reason, and given that at f_P the phase of the loop gain is almost 360°, we may safely approximate $f_{OSC} \cong f_P$. Furthermore, it holds that $(f_P - f_{OSC})/f_{OSC} < 0.1\%$.

Now, with (2) and (5), we are able to calculate the modulus of the PT gain at the oscillation frequency:

$$\left|A_{VPT}(f_{OSC})\right| \cong \left|A_{VPT}(f_P)\right| = \frac{C_{eq}}{NC_{OUT}\left|-\frac{C_{eq}}{C_{d1}} + j\frac{R_M C_{eq}}{\sqrt{L_M C_{eq2}}}\right|} \cong \frac{C_{eq}}{NC_{OUT}\sqrt{\left(\frac{C_{eq}}{C_{d1}}\right)^2 + \frac{1}{Q^2}}} \cong \frac{C_{d1}}{NC_{OUT}} \qquad (6)$$

where $Q = \omega_s L_M / R_M$, and $\omega_s = (L_M C_{eq})^{-1/2}$ is the electric resonance pulsation. The approximation in (6) holds if $Q^2 >> (C_{d1}/C_{eq})^2$, which is a reasonable condition in multilayer PTs due to their very high quality factor. In our case, Q^2 is almost three orders of magnitude higher than $(C_{d1}/C_{eq})^2$. Then, the voltage gain of the PT at f_P does not depend on the quality factor.

The PT input impedance $Z_{PT}(s)$ can also be calculated:

$$Z_{PT}(s) = \frac{1}{sC_{d1} + \left(sL_M + R_M + (sC_{eq})^{-1}\right)^{-1}} = \frac{s^2 L_M C_{eq} + sR_M C_{eq} + 1}{s(C_{d1} + C_{eq})(s^2 L_M C_{eq2} + sR_M C_{eq2} + 1)} \qquad (7)$$

From (7), it can be observed that the poles are extremely close to zeros since $C_{eq2} \cong C_{eq}$. If (7) is switched to the frequency domain by posing $s = j2\pi f$, we can observe that the modulus of $Z_{PT}(s)$ is maximum when $(s^2 L_M C_{eq2} + sR_M C_{eq2} + 1)$ is minimum, that is extremely close to $f_P = 1/2\pi \cdot (L_M C_{eq2})^{-1/2}$. Then, considering that $C_{eq} \cong C_M$, and that the quality factor is extremely high, from (7) it can be found that $|Z_{PT}(s)|$ is maximum when $Z_{PT}(s)$ is almost real (see also **Fig. 5**):

$$\left|Z_{PT}(f_P)\right| \cong \left(\frac{QC_{eq}}{C_{eq} + C_{d1}}\right)^2 R_M \cong \mathrm{Re}\left\{Z_{PT}(f_P)\right\} \qquad (8)$$

By using (2), (4), (6), (8), we can now determine the total loop gain $A_{VT}(f)$ at the oscillation frequency:

$$A_{VT}(f_{OSC}) \cong A_{VT}(f_P) \cong \frac{V_{IN}}{|V_P|} \cdot \frac{n \cdot m}{(m+n)^2} \cdot \frac{C_{d1}}{NC_{OUT}} \cdot \frac{Z_{PT}(f_P)}{Z_{PT}(f_P) + 1/[(n+m)g_{ds}]} \qquad (9)$$

From (6) and (8) we see that a high C_{d1} is desirable for high gain. However, at the same time, a lower value of C_{d1} increases the PT input impedance and reduces the load effect on the previous stage. This means that, if a PT with an extremely high Q (i.e. around 1000) were available, the connection of an external capacitor in parallel to C_{d1} would decrease Z_{PT} according to (8), without affecting too much A_L according to (4), and would increase A_{VPT} according to (6). In this specific case, the value of (9) might be maximized by selecting a proper value of the additional capacitor.

If $|A_{VT}(f_{OSC})| \geq 1$, an oscillation can be triggered in accordance with the Barkhausen gain criterion. By solving (9) for V_{IN}, the minimum input voltage required to achieve oscillation is found to be:

$$V_{IN,MIN} > \frac{(m+n)^2}{m \cdot n}|V_P| \cdot \frac{NC_{OUT}}{C_{d1}} \cdot \left[R_M + \frac{1}{(n+m)} \frac{|V_P|}{2I_{DSS}} \frac{1}{Q^2} \left(1 + \frac{C_{d1}}{C_{eq}} \right)^2 \right] \qquad (10)$$

We point out that the both Barkhausen criteria were used for determining the oscillation condition, although these criteria have not a general validity, since they give only necessary but not sufficient conditions. In fact, they claim to determine the oscillation condition from steady state response, and not from transient response. As matter of fact, there are many linear systems that satisfy both Barkhausen criteria and do not oscillate [33]. Then, a more rigorous method, such as root locus, Routh criterion or Nyquist plots, should be adopted. In our case, the mathematical model of the system was implemented in Matlab, and the root locus showed two complex poles in the right half plane if $V_{IN} > V_{IN,MIN}$.

Moreover, an intuitive explanation on the fact that the system is unstable can be found in (7): $Z_{PT}(s)$ has zeros extremely close to the poles. Then, from a stability point of view, they almost cancel each other, in fact in the root locus the poles are attracted by the nearest zeros. Hence, in open loop, the system described by (9) is similar to a system with only complex poles that will be always unstable in a feedback loop if a proper gain is provided.

Furthermore, we have shown only the full wave mode. However, oscillation at the very beginning might occur simultaneously at first and second mode, if the voltage loop gains at both frequencies are greater than unity and comparable, and if the two modes are approximately separated by a factor of two. For the considered PT, we found the first electrical parallel resonance at about 55.117 kHz (accounting for the capacitive load effects of the amplifier JFETs and voltage doubler), whereas the second electrical parallel resonance occurred at 106.8 kHz. No other modes were found at higher frequencies. The oscillation can initially occur at the first mode, as predicted also by SPICE simulations performed with the corresponding equivalent circuit of the PT. However, when the amplitude of oscillation grows, the nonlinearities will produce a harmonic at a double frequency. Hence, the energy of the first mode will be split into two bands: the first is centred around the first mode of oscillation, while the second will be located in a band very close to the second mode. Hence, as the amplitude of oscillation grows and nonlinearities become significant, energy is progressively subtracted from the first mode, and injected into the second mode that gains more and more excitation. At the end of the transient, the system will be locked at the second mode. In general, it is not possible to predict the oscillation frequency with the Bode plots if the Barkhausen criteria are satisfied in more than one point. A low-pass or band-pass filter in the loop, as well as mechanically clamping some nodes, can help selecting the desired mode.

The values of the parameters of the PT and of the other circuit elements used in the calculations are reported in **Table I**. The JFET parameters were extracted from a single instance of the device.

Another point that worth mentioning is that variations of the parameters caused by environmental variations are not necessarily an issue as long as the loop gain is sufficient, since the circuit self-locks very close to the actual anti-resonance frequency. The system is intended for use in ultra-low power energy harvesting applications (in the order of tens of μW). Hence, there is not a problem of heat dissipation. However, temperatures above 110°C shift both the series and parallel resonant frequencies of the PT, and worsen the overall quality factor. At these temperatures, also JFETs

undergo parameter variations, and then $V_{IN,MIN}$ increases. It is also worth to mention that the adopted PT is designed to handle power levels in the order of Watts (e.g. backlight for LCD), with maximum input voltages of 18 V (rms) and maximum output voltages of 1800 V (rms). Hence, it is not optimized for ultra-low voltage micro-power operation, as this is not a typical application of PTs. A custom PT design is expected to obtain better performance and shrunk geometries. In addition, the maximum V_{GS} and V_{DS} of the adopted JFETs is 40 V. Hence, voltage limitations do not apply for the considered application.

4. Experimental measurements

Fig. 6 shows a prototype of the circuit used for model validation. An Agilent E3631A power supply was initially used instead of a real TEG, in order to have a better control of the input voltage. Data were acquired with a Tektronix MSO2024 digital sampling oscilloscope. The optimum configuration of amplifier and load JFETs was determined with the analytical model implemented in Matlab, and was numerically found to be $n = 3$ and $m = 5$. An external resistor $R_T = 2.4\ \Omega$ was connected in series to the power supply, in order to emulate the output resistance of a Multicomp MCPE-071-10-15 TEG source. However, it is worth to note that this is a relatively worst case; since TEGs with series resistances lower than 1 Ω [3] are relatively common. The voltage drop on R_T was estimated with an Agilent 34401A digital multimeter, and was found to be less than 0.5 mV for $V_{IN} = 69$ mV. The DC current at start-up was found to be about 180 µA. Such very low voltage drop affects perceptibly neither the differential parameters of JFETs, nor the initial bias point. Then, the assumption of safely neglecting R_T in (3) is acceptable.

Fig. 7a shows the measured waveforms during the start-up of the circuit when $n = 3$ and $m = 5$, that is in the optimum configuration: V_{IN} was increased very slowly in order to emulate a TEG subject to a slowly varying temperature gradient and an oscillation is triggered at node A when $V_{IN} \cong 69$ mV, whereas (10) predicts 70 mV as the minimum start-up voltage. However, we observed that when different sets of JFETs are used, the minimum activation voltage $V_{IN,MIN}$ can increase up to 81 mV because of variations in device parameters. Among the tested samples, R_{DS} ranged from 663 Ω to 731 Ω. The output capacitor gets charged to about 1.5 V with the output node in an open circuit configuration, emulated with high input resistance voltage probes based on Texas Instruments LMC6482A operational amplifiers in a buffer configuration. The JFET parameters used in the equations (Table I) were extracted from measurements performed on selected samples.

Fig. 7b reports the start-up waveforms obtained with a Multicomp MCPE-071-10-15 TEG source in the same optimum configuration. The TEG was placed in proximity of the air vent of a laptop. The external temperature was 26 °C, and the estimated temperature of the hot air was about 52 °C. C_{STORE} started being charged when the TEG voltage was about 79 mV, which is comparable with the previously obtained results.

Once oscillation has reached a steady state, the minimum voltage able to keep the system oscillating was found to be about 56 mV, which is lower than the start-up voltage. This happens because in steady-state the input stage acts similarly to a class AB amplifier with respect to large signals, since the gate signal at node B (see **Fig. 8**) falls below the JFET pinch-off voltage ($V_P \cong -0.85$ V), hence the device current is null for a large part of the oscillation period. The average current drained by the common source in steady state drops to about 117 µA.

Fig. 8 compares the measured voltage waveforms of V_A (PT input) and V_B (PT output): the measured phase shift of 178° confirms that the PT is oscillating in close proximity of antiresonance f_P, as discussed in Section III and as shown in **Fig. 5**. The oscillation frequency is 105.3 kHz, slightly different from model predictions. There are mainly two reasons:

(i) the model is valid at the beginning of the oscillation and not in the steady state; (ii) the few additional pF of the probes load the PT output (V_B) and increase C_{OUT}, and hence lower the oscillation frequency. Without probes at node B, the oscillation frequency measured at node A is about 106.4 kHz against the 106.8 kHz predicted by the model.

Fig. 9 presents a comparison between (10) and measurements, with different configurations of amplifier and load JFETs. It can be found out that all mismatches between model predictions and measurements are within 15%, and the root mean square error is 9.3 mV. Furthermore, in order to assess the behaviour of the system in presence of variations in device parameters, some corner simulations were performed with the assumption that V_P, β_n and C_G can have maximum relative variations of ±10% with respect to their nominal values. The results are shown in Fig. 9. It was found out in all configurations that the best condition in terms of minimum start-up voltage (bc curve) occurs when C_G is 10% lower, while $|V_P|$ and β_n are 10% higher. The worst condition (wc curve) is the dual form of the best condition and occurs when C_G is 10% higher, while $|V_P|$ and β_n are 10% lower. As can be noticed in Fig. 9, the curve obtained from measurements (meas curve) always lies between the bc and wc curves. The reference curve (ref) was obtained considering the parameters for all JFETs equal to the nominal ones reported in Table I. The measurements were repeated with different random sets of JFETs, and the measured $V_{IN,MIN}$ falls between the wc and bc curves. Additionally, a cause of the mismatches has to be found in the fact that certain configurations of n and m partially invalidate the first assumption of deep triode region for the JFETs. Given that $|V_P| = 0.85$V and that V_{GS} is assumed 0 V for both load and amplifier JFETs, for the optimum configuration ($n = 3$, $m = 5$) we have that $V_{DS1} = V_{IN}(m/(n+m)) = 44$ mV and $V_{DS2} = V_{IN}(n/(n+m)) = 36$ mV (both calculated at $V_{IN} = 70$ mV), so the relation $V_{DS1,2} << |V_P|$ is verified. However, for configurations such as [$n = 1$, $m = 5$], since the mathematical model predicts a minimum activation voltages of 179 mV, we have $V_{DS1} = 149$ mV and $V_{DS2} = 30$ mV. The n amplifier JFETs and m load JFETs cannot be considered anymore a voltage divider because only the load JFETs are in deep triode region. For a configuration like [$n = 5$, $m = 1$] it happens that most of the input voltage falls across the load JFETs drain and source terminals, hence only the amplifier JFETs are in deep triode region. The previous considerations can be applied also to configurations like [$n = 1$, $m = 4$]. In general the developed model cannot be applied to configurations far from the optimum in terms of minimum input voltage, because in these cases either the amplifier or load JFETs cannot be considered in deep triode polarization. In such cases the values predicted by the mathematical model are higher than expected, since the devices are slightly closer to the pinch-off region where the transconductance and output conductance are higher compared to the linear prediction. Based on these considerations, it can be observed that the mismatch is minimized around the optimum condition for n and m, and that the model correctly predicts the direction towards which to change parameters for reaching the optimum configuration.

Although for $m = 1$ it may seem that there is a less qualitative fit between the two curves, it is worth to note that both mathematical model and measurements predict the point of minimum activation voltage located at $n = 3$. For $m = 2$, it seems that the qualitative fit is not as good as the other cases, this could be caused as usual by a positioning of the devices close to a worst condition of device parameters.

We found that the value of the load resistance affects only the steady state value of V_{OUT}, while the charging time remains unchanged. **Fig. 10a** shows the output voltage as a function of the input voltage for various loads ranging from 10 MΩ to 1 GΩ (which approximates the unloaded condition). The 10 MΩ load corresponds to the current typically drawn by an ultra-low power voltage monitor circuit [8] [34] made with discrete components, which activates the main power converter when a sufficient voltage is reached. The higher resistances are achievable by integrated circuits. With the minimum voltage, at steady-state $V_{OUT} = 1.5$ V in the unloaded case, and drops to 0.55 V with 10 MΩ. As it can be

observed, the behaviour is almost linear with an average slope ranging from 18.3 mV/mV (10 MΩ load) to 25.6 mV/mV (1 GΩ load). Then, in order to achieve a 100 mV increase in V_{OUT}, the TEG voltage should be increased of about 4-5 mV in all cases.

Comparing the output power P_{OUT} with the maximum TEG power P_{MAX} and with the actual TEG power P_{TEG} is useful to assess the overall performance. P_{OUT} can be expressed as $P_{OUT} = P_{MAX} \cdot \alpha \cdot \beta$, where $\alpha = P_{TEG}/P_{MAX}$, and β is the electrical efficiency of the circuit. It holds that $0 < \alpha < 1$, $0 < \beta < 1$, and $P_{MAX} = V_{IN}^2 / (4R_T)$. In the condition $V_{IN} = 69$ mV, before the oscillation begins, the DC power consumed by the common source is $P_{TEG} = 12.76$ µW and the current is $I_{TEG} = 180$ µA (with $n = 3$, $m = 5$, $R_T = 2.4$ Ω, and $R_{DS} \cong 720$ Ω for each JFET). In steady-state, I_{TEG} drops to about 125 µA, and P_{TEG} to about 8.7 µW, due to the increased efficiency of the input stage. **Fig. 10b** shows the output power as a function of the load, for various input voltages. The power monotonically decreases with the input voltage; hence, the optimum load resistance is lower than 10 MΩ. Values lower than 10 MΩ were not considered because the corresponding V_{OUT} is not sufficient for our purposes. At the minimum input voltage, P_{OUT} ranges from tens to hundreds of nW, and we can estimate $P_{MAX} = 495$ µW. It turns out that $\alpha \cong 2\%$. However, α is necessarily low: it is mandatory that the loaded TEG provides the minimum operating voltage required by the circuit. Then, if the open-circuit voltage of the TEG is slightly higher than the minimum start-up voltage, the TEG should be necessarily biased in an almost open-circuit condition, i.e. far from its maximum power point (MPP). A TEG biased in the MPP would provide only half of its open-circuit voltage. In general, α can be increased provided that higher TEG voltages are available. However, in this case, start-up circuits are likely to be unnecessary. For the proposed circuit, it can also be verified that $\beta \cong 1\%$, and that bias currents are a major cause of power losses. In general, step-up oscillators are not easily tuned on the MPP. For this reason, dual architectures are usually proposed, as in [17]. In our case, the start-up circuit is used only for recovering from a fully discharged state and, from then on, the active converter should remain active. However, this may prevent all applications where a fast recovery time from long power outages is required. In order to decrease the recovery times, energy harvesting circuits with separate differently-sized capacitors for the power converter and the load have been recently reported [35].

5. Performance Improvement

Since our goal is to develop a start-up circuit compatible in perspective with microelectronic and MEMS technologies, PTs were primarily chosen in this work instead of MTs. The step-up Armstrong oscillator based on a MT (**Fig. 1**) allows the voltage source to directly bias the amplifier JFETs, whose g_m is proportional to V_{DS}. In fact, in DC the primary side of the MT is a short circuit, whereas JFETs used in this paper implement a voltage divider. In order to introduce the aforementioned advantage of the MT-based solution, we also propose to substitute the load JFETs with an inductor L_S as shown in **Fig. 11a**. Although this deviates from our primary goal of an inductor-less solution, in view of the introduced advantages, it may still be acceptable in specific applications because of the relatively low value of the required inductance. It is also worth to mention that the size of the required inductor is still much smaller than that of the MTs used in step-up oscillators. Tiny inductors can be also potentially integrated at package-level.

From (3), in the case $n = m$, we estimate that the unloaded voltage gain of the CS stage is a quarter of that of a CS with same n and an inductive load of proper value: in DC the inductor is a short and the amplifier JFET receives the whole source voltage; hence, the overall g_m is doubled; in addition, the output conductance of the CS stage is halved, given that this is only ng_{ds} and not $(n + m)g_{ds}$. However, in order not to alter the system behaviour at f_{OSC}, it is necessary that at

this frequency L_S has already resonated with the PT input capacitance C_{d1}, so that C_{d1} is prevalent with respect to L_S. Then, it should be verified that:

$$L_S > \frac{1}{(2\pi f_{OSC})^2 C_{d1}} \qquad (11)$$

At the measured f_{OSC} of 106.4 kHz, and with C_{d1} = 231 nF as reported in Table I, according to (11) we obtain L_S > 10 µH, so that roughly even 30 - 40 µH can be sufficient. If the quality factor of the inductor is high, at f_{OSC} the phase shift introduced by the first stage is practically 180°; hence, the system will oscillate at f_P. If the quality factor Q_L of the inductor is poor, the equivalent resistance of L_S will introduce losses, will lower the output resistance of the common source, and will shift the oscillation frequency far from f_P.

In the case of inductive load in the CS stage, the series resistance R_T of the TEG cannot be generally neglected. We can consider the effect of R_T together with the equivalent series resistance of L_S and call this global resistance R_S. It can be demonstrated that the series combination of L_S and R_S can be modelled at a particular frequency, e.g. f_{OSC}, as a parallel combination of an inductor L_P and a resistor R_P, as depicted in **Fig. 11b**:

$$L_P = L_S \cdot \left(1 + Q_L^2\right) / Q_L^2 \qquad (12)$$

$$R_P = R_S \cdot \left(1 + Q_L^2\right) \qquad (13)$$

where $Q_L = 2\pi f_{OSC} L_S / R_S = R_P / (2\pi f_{OSC} L_P)$. Hence R_P is a frequency dependent resistance. However, also R_S can in principle be frequency dependent, because of eddy currents and hysteresis losses in the core and of the skin depth in the windings. Hence, the choice of the inductor should not be based only on its DC resistance. From a practical point of view, if $Q_L > 4$, then $L_P \cong L_S$ and $R_P \cong R_S \cdot Q_L^2$. In order for R_P to be negligible in the small-signal circuit, it should be verified that $R_P >> 1/(n \cdot g_{ds})$. Then, R_S should verify the following condition:

$$R_S << \left(2\pi f_{OSC} L_S\right)^2 \cdot n g_{ds} \qquad (14)$$

If (14) is verified and L_S sufficiently high, in first approximation A_{Vcs} becomes independent from the number of the amplifier JFETs if n is chosen as high as possible. However, as an upper limit, the n parallel gate capacitances of JFETs should not increase significantly the PT output capacitance C_{OUT}, which affects A_{VPT} according to (6). When n is too high, the value of A_{VPT} drops. Increasing n also relaxes the condition about R_S. The same happens with L_S, if R_S is mostly due to the TEG. In order to adapt the mathematical model, it can be found out that:

$$A_{Vcs} = -\frac{g_m}{g_{ds}} \frac{Z(s)}{Z(s) + (n g_{ds})^{-1}}, \qquad (15)$$

where g_m and g_{ds} are the transcondutance and output conductance of a single JFET and $Z(s) = (1/Z_{PT}(s) + 1/R_P + 1/(sL_P))^{-1}$. If (11) and (14) are satisfied, the effect of L_P and R_P can be neglected.

Fig. 12a reports the simulated Bode plots of the loop gain obtained with V_{IN} = 70 mV (i.e. about the voltage required to start the inductor-less system) in different configurations. The loop gain with n = 3 and m = 5 reaches exactly 0 dB at 0° of phase shift. When L_S = 37 µH and R_S = 3.05 Ω, a maximum gain of about 4.8 dB is achieved when $4 \le n \le 6$ at the same V_{IN}. This means that $V_{IN,MIN}$ can be lowered from 70 mV down to about 40 mV, since $20\log_{10}(40 / 70) \cong -4.8$ dB. In experimental measurements, as it can be observed in **Fig. 12b**, with n = 4 we obtained a minimum start-up voltage of 40 mV, when using a Multicomp MCPE-071-10-15 TEG with ~ 2.4 Ω internal resistance, and a 37 µH inductor with ~0.65 Ω series resistance at 106 kHz. In this case the TEG was placed on the AC/DC adapter of a laptop, whose external temperature was measured to be about 42 °C.

In this case as well, if experiments are repeated with random selections of the n JFETs, the resulting variations in $V_{IN,MIN}$ are slightly higher than the deviations from the theoretical values. In this case, we measured 32 mV ≤ $V_{IN,MIN}$ ≤ 35 mV with n = 3 and R_S ≅ 0.65 Ω , whereas with n = 6 and R_S ≅ 1.2 Ω we measured 34 mV ≤ $V_{IN,MIN}$ ≤ 36 mV. Measurements performed with n = 3 and R_S ≅ 1.2 Ω showed that $V_{IN,MIN}$ can range from 48 mV up to 52 mV with random sets of JFETs. This also confirms that increasing n can compensate for higher R_S as predicted by (14), and that higher R_S for the same value of n could be very critical for the activation voltage.

Fig. 13a depicts the linear behaviour of V_{OUT} versus V_{IN} with an inductive load and n = 4. A slope of 35 mV/mV is obtained and this value is higher than in the inductor-less case. In this specific implementation R_S = 0.65 Ω is the limit value under which $V_{IN,MIN}$ does not decrease anymore, given that ng_{ds} is dominating the output conductance of the CS stage. **Fig. 13b** depicts V_{OUT} measured with V_{IN} = 32 mV, n = 4, and an inductor with L_S = 37 µH and R_S = 0.65 Ω, for various loads ranging from 1 MΩ to 50 MΩ. A maximum voltage of about 800 mV is obtained with a 50 MΩ load. The output power decreases if the load resistance increases and, once again, the optimum load is shifted towards lower values of load resistance.

Concerning the inductor, a first consideration is that it has a smaller size than the MTs adopted in conventional step-up oscillators. For example, the Coilcraft XFL2006 and LPO3010 series of inductors achieve inductances up to 100 µH with package dimensions of 2×2×0.6 mm^3 and 3×3×1 mm^3, respectively. The Coilcraft LPR6235, one the the smallest available MTs with turn-ratios up to 1:100 has a 6×6×3.5 mm^3 ,package. In addition, a single external inductor may be shared between the proposed start-up circuit and the DC/DC converter. Furthermore, at higher packaging costs, a small inductor might be integrated at package level, as in power-supply-in-package (PSIP) devices [36]. Finally, miniaturized TEG with footprints of 2 mm^2 are also available [37].

6. Conclusion

The main advantage of the derived model is the possibility of assessing and sizing system components in early phases of system design, once the thermal gradients and the TEG are known. In addition, the model allows to optimize design parameters and to determine the requirements for oscillation. For example, it predicts lower start-up voltages if PTs with higher quality factors are used. The influence of variations of transistor parameters on the start-up voltage was found to be limited, and comparable with the mismatch between model predictions and measurements.

One aspect that is worth discussing further is system integrability. In perspective, package-level integration of mixed microelectronic circuits and MEMS PTs can be envisaged. MEMS PTs can be implemented in areas as low as few mm^2 [38] [39]. However, storage capacitors in the order of µF should necessarily be off-chip. For this purpose, thin film supercapacitors are available for package-level integration [40] [41]. Conventional tiny SMD packages would also have a limited impact on area. The storage capacitor should be sized based on the current requirements of the application circuit. In general, in order to sustain a single packet transmission of a wireless node, i.e. roughly tens of mA for tens of ms, several µF are required. Another critical component for integrability could be the inductor, however a small inductance of few tens of µH is required to improve circuit performance, as well in the external DC/DC converter, and commercial solutions in fooprint area less than 10mm^2 are already available.

The presented circuit should be intended as a single building block of a more complex energy harvesting systems. Other design challenges should be faced. As a first requirement, a sub-µA voltage monitor should be implemented, with the purposes of: (i) activating the DC/DC converter, similarly to the circuits presented in [8] [9] [34], and (ii) of disabling

the start-up, which could be accomplished by pulling the gate of the load JFET above its pinch-off voltage. Another hurdle would be the design of a MPPT DC/DC converter able to operate with input voltages as low as tens of mV, as in [6]. Finally, in the inductor-based solution, it would be useful to share the inductor with the DC/DC converter.

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Legend & Figure Captions:

Table I: Parameters of the components used in this work.

Fig. 1. Structure of a conventional step-up oscillator based on a magnetic transformer.

Fig. 2. Block diagram of a battery-less energy harvesting system.

Fig. 3. Equivalent electro-mechanical circuit of a PT with lumped parameters around a given resonance.

Fig. 4. Circuit schematic and theoretical waveforms.

Fig. 5. Bode plots of the input impedance of the PT and of the voltage gains. The oscillation frequency f_{OSC} is extremely close to the parallel resonance f_P.

Fig. 6. Picture of the experimental setup.

Fig. 7. Measured start-up waveforms in the optimum condition ($n = 3$, $m = 5$) obtained with: (a) a power supply with a series resistance of 2.4 Ω; (b) a Multicomp MCPE-071-10-15 TEG source.

Fig. 8. Measured steady-state voltage waveforms of V_A (PT input) and V_B (PT output). The measured phase shift is $\Delta\varphi = -178°$.

Fig. 9. Comparison between model predictions and measured (meas) values of the minimum start-up voltage $V_{IN,MIN}$ for n and m ranging from 1 to 5. The reference curve (ref) was obtained considering the nominal JFET parameters reported in Table I. The best and worst case curves, respectively (bc) and (wc), case (bc) and worst case (wc) curves were obtained with a corner analysis considering ±10% variations of JFET parameters.

Fig. 10. (a) Measured steady-state output voltage V_{OUT} as a function of source voltage V_{IN} for various loads. (b) Measured output power P_{OUT} as a function of R_{LOAD} for various V_{IN}.

Fig. 11. (a) Replacement of the load JFETs with a generic lossy inductor L_S. (b) Equivalence of the series L_S-R_S with the parallel L_P-R_P at a given frequency.

Fig. 12. (a) Simulated loop gain at $V_{IN} = 70$ mV and $R_T = 2.4$ Ω with the load JFETs in the optimum condition ($n = 3$, $m = 5$) and with the inductor ($L_S = 37$ µH, $R_S = 0.65$ Ω) in various configurations of n. With load JFETs, the gain is exactly at 0 dB. A maximum additional gain of about 4.6 dB is obtained in case of inductive load with respect to the JFETs load. (b) Measured start-up waveforms obtained with a Multicomp MCPE-071-10-15 TEG source with an inductor of 37 µH and 0.65 Ω of series resistance.

Vitae:

Antonio Camarda received the M.S. degree in Electronic Engineering from the Politecnico di Bari, Italy, in 2010. He has then been a SAP IT Consultant for a year and a half. In 2011 he joined the research lab University of Bologna – STMicroelectronics as analog IC designer. Since 2012 he has been working towards the Ph.D. degree at the University of Bologna, Cesena, Italy. His research interests include integration of magnetic devices, design techniques for low-voltage converters, and low power IC design.

Aldo Romani received the Dr. Eng. degree in Electrical Engineering in 2001 and the Ph.D. degree in Electrical Engineering, Computer Science and Telecommunications in 2005 from the University of Bologna (Italy), where he currently serves as assistant professor. He's been working on CMOS integrated sensors, applications of piezoelectric materials, and energy harvesting systems. He is a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference and is author or coauthor of more than 40 international scientific publications.

Enrico Macrelli received the M.S. degree in Electronic and Telecommunications Engineering in 2009 and the Ph.D. degree in Information Technology in 2014, from the University of Bologna (Italy). In 2012 he joined the Tyndall National Institute (Cork, Ireland) as visiting researcher, and worked on design and fabrication of micro-magnetic components. He is currently Postdoctoral Researcher at the Department of Electrical and Computer Engineering of the National University of Singapore. He's currently working on miniaturized integrated carbon dioxide sensing platforms. His research interests include design techniques for micro-power energy harvesting systems and acoustic sensors.

Marco Tartagni received the M.S. and the Ph.D. degree in EE both from the University of Bologna (Italy). He joined the EE Department at the Caltech in 1992 and in 1994. Since March 1995 he has been with the EE Dept., University of Bologna, as Associate Professor. From 1996 to 2001 he has been team leader of the joint STM and University of Bologna lab and, since 2014, member of the scientific committee. He has been local and European coordinator of several FP5-6-7 projects. He was co-recipient of the 2004 IEEE Van Vessem Award. He is co-author of more than 100 peer-reviewed scientific publications and holder of more than 20 US/WIPO patents.

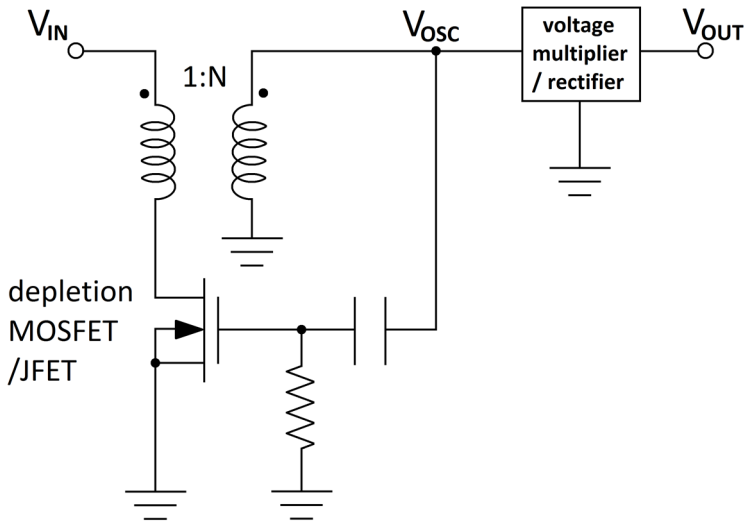


Fig. 1. Structure of a conventional step-up oscillator based on a magnetic transformer.

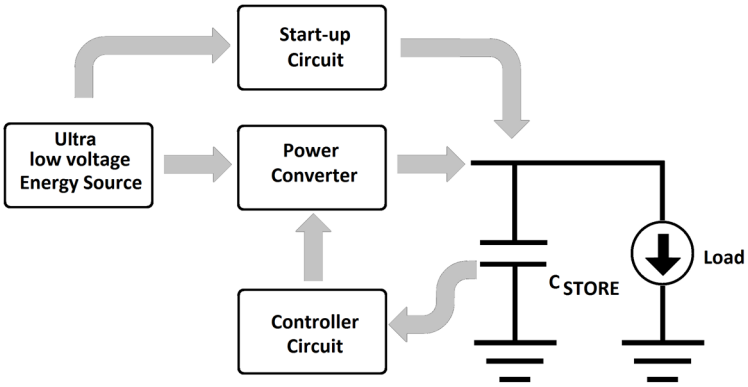


Fig. 2. Block diagram of a battery-less energy harvesting system.

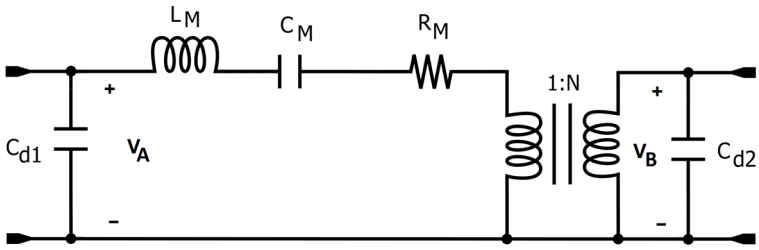


Fig. 3. Lumped equivalent electromechanic circuit of a PT around a certain resonance.

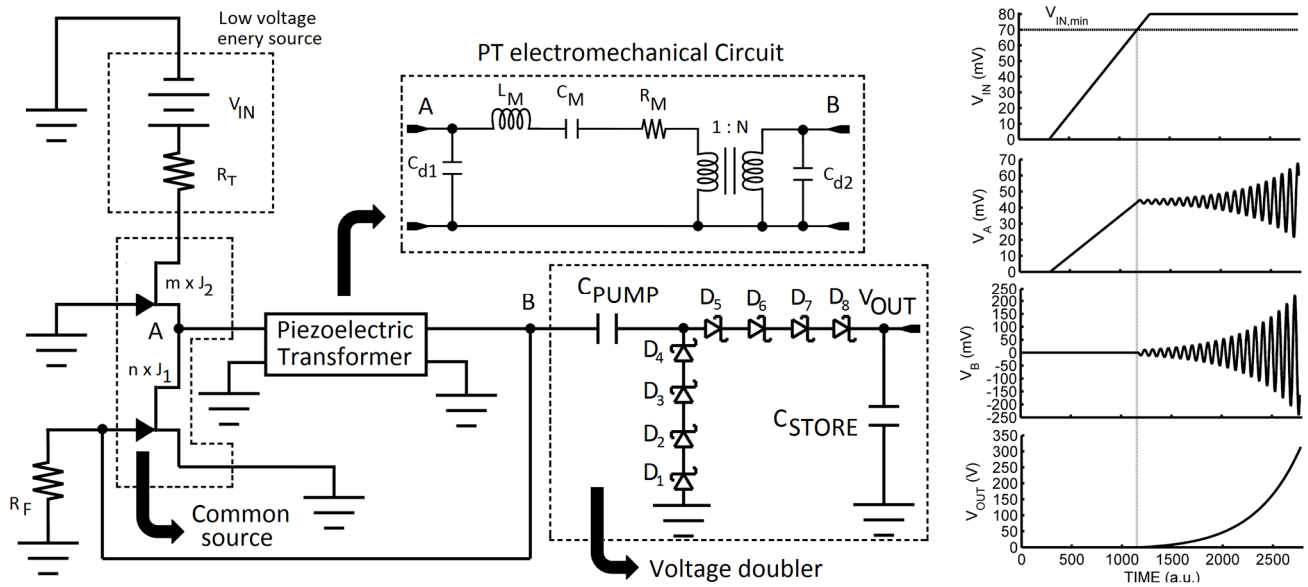


Fig. 4. Circuit schematic along with theroretical waveforms. The output of the PT is fed directly into the gate of the amplifier JFET J_1, whereas the voltage doubler boosts and rectifies the amplified oscillation at the PT's output. The DC voltage of the signal at node B depends on the used transistor: in case of JFET, this is lower than 0 V, in case of depletion MOSFET it could be around 0 V.

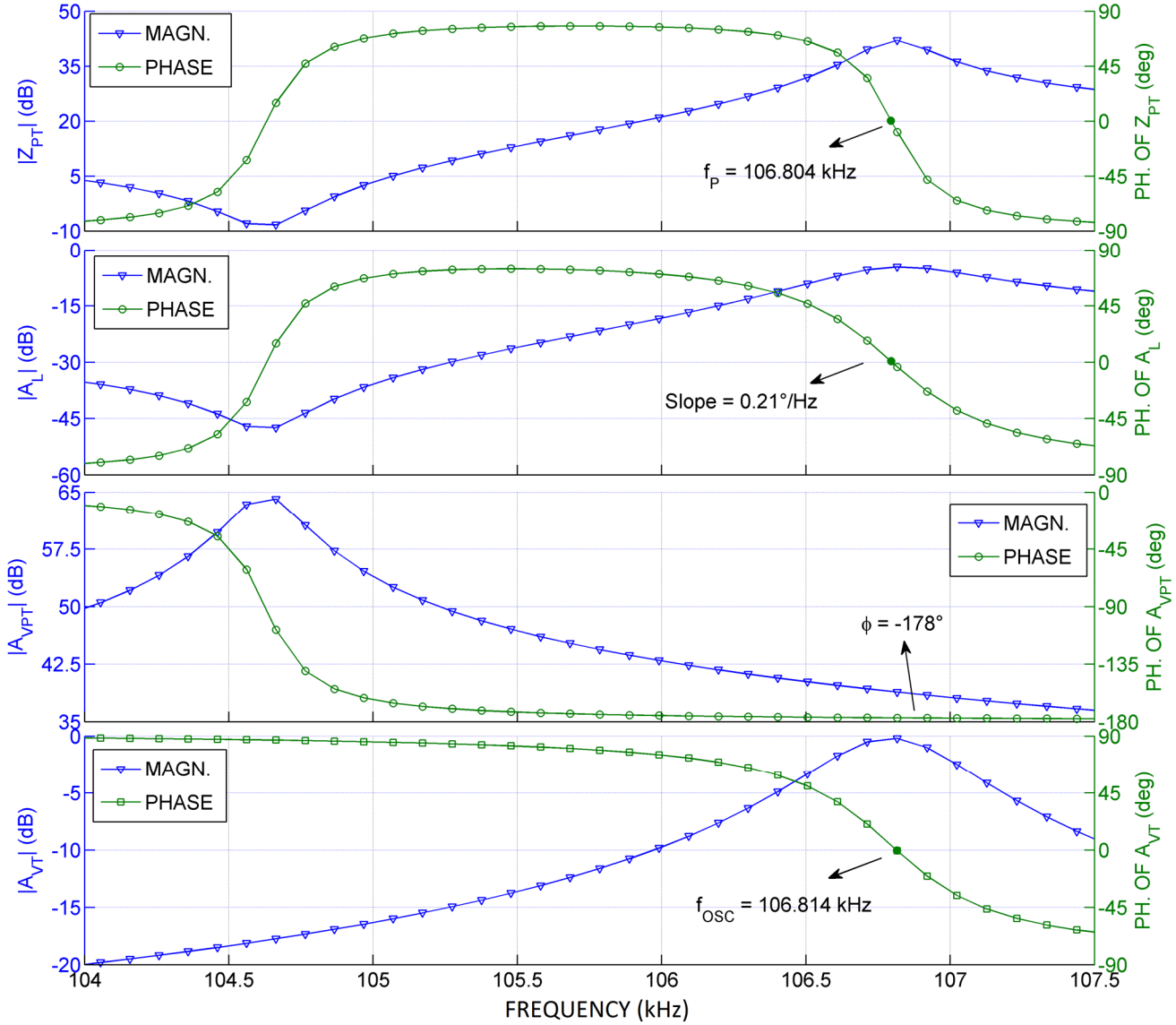


Fig. 5. Bode plots of the input impedance of the PT, and of the voltage gains. The oscillation frequency f_{OSC} is extremely close to the parallel resonance.

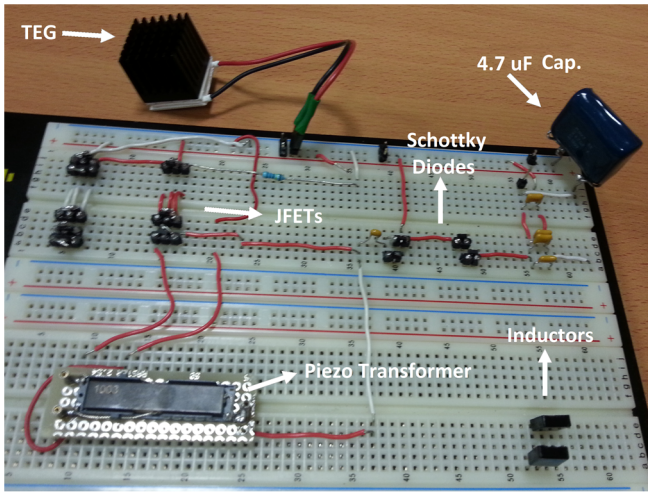


Fig. 6. Picture of the experimental setup.

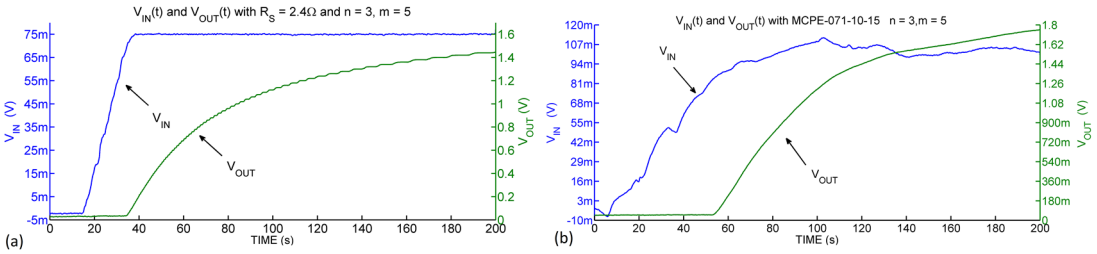


Fig. 7. Measured start-up waveforms in the optimum condition (n = 3, m = 5) obtained with: (a) a power supply with a series resistance of 2.4 Ω; (b) a Multicomp MCPE-071-10-15 TEG source. Data were smoothed in Matlab, in order to filter the high-frequency noise of the oscilloscope.

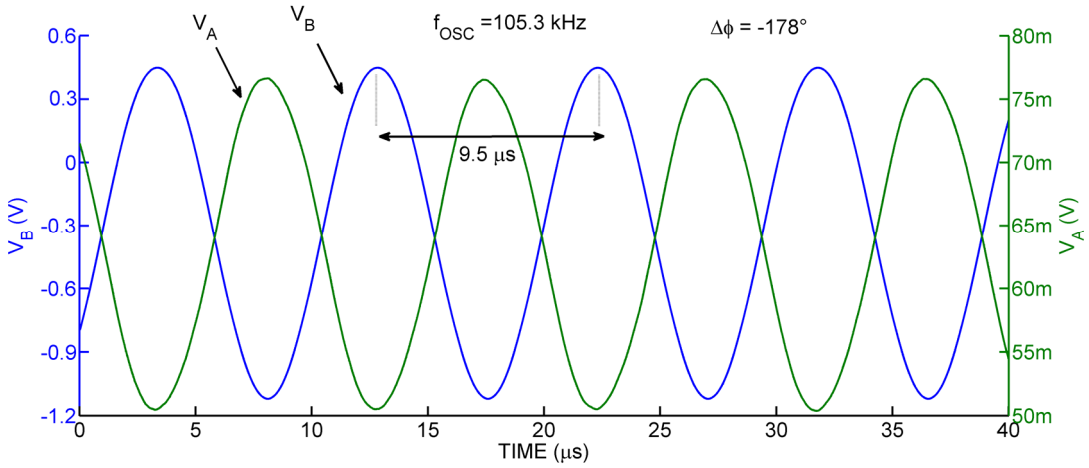


Fig.8. Measured steady-state voltage waveforms of V_A (PT input) and V_B (PT output). The measured phase shift is $\Delta\varphi = -178°$. Data were directly averaged through the oscilloscope, in order to eliminate high frequency noise.

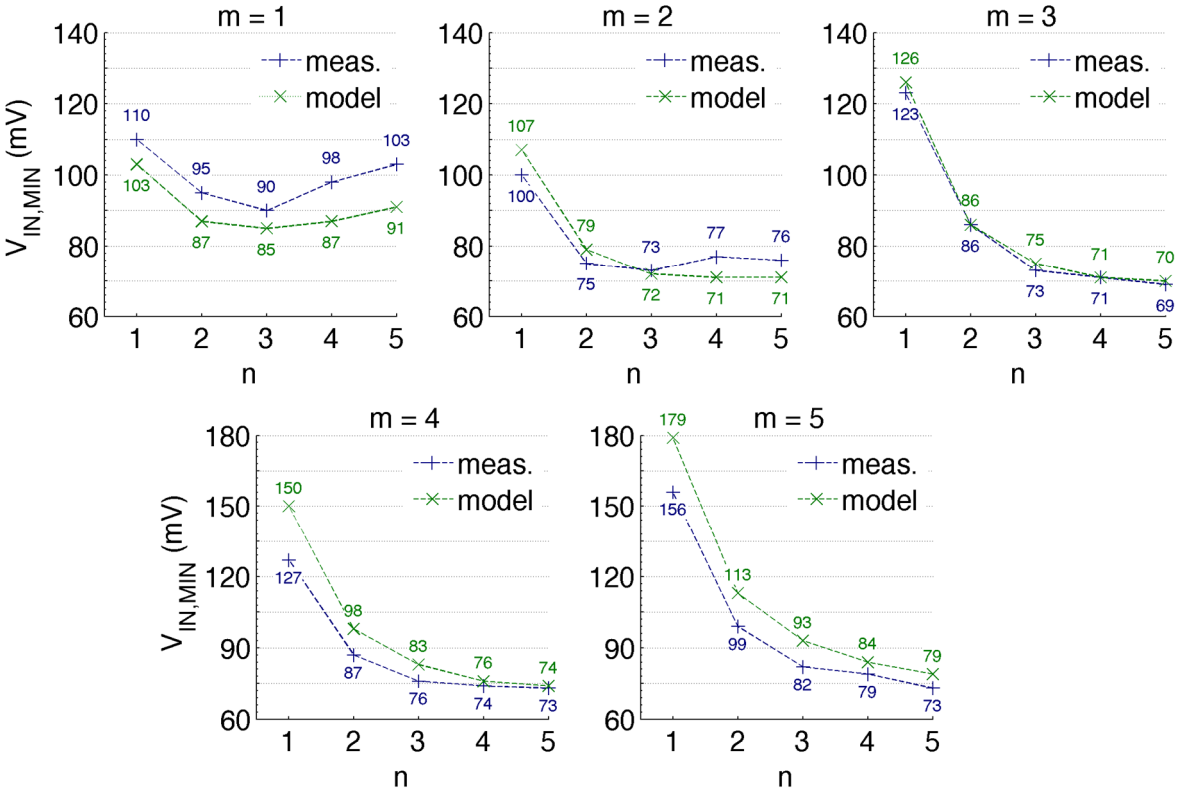


Fig. 9. Comparison between model prediction and measured value of the minimum start-up voltage $V_{IN,MIN}$ for n and m ranging from 1 to 5.

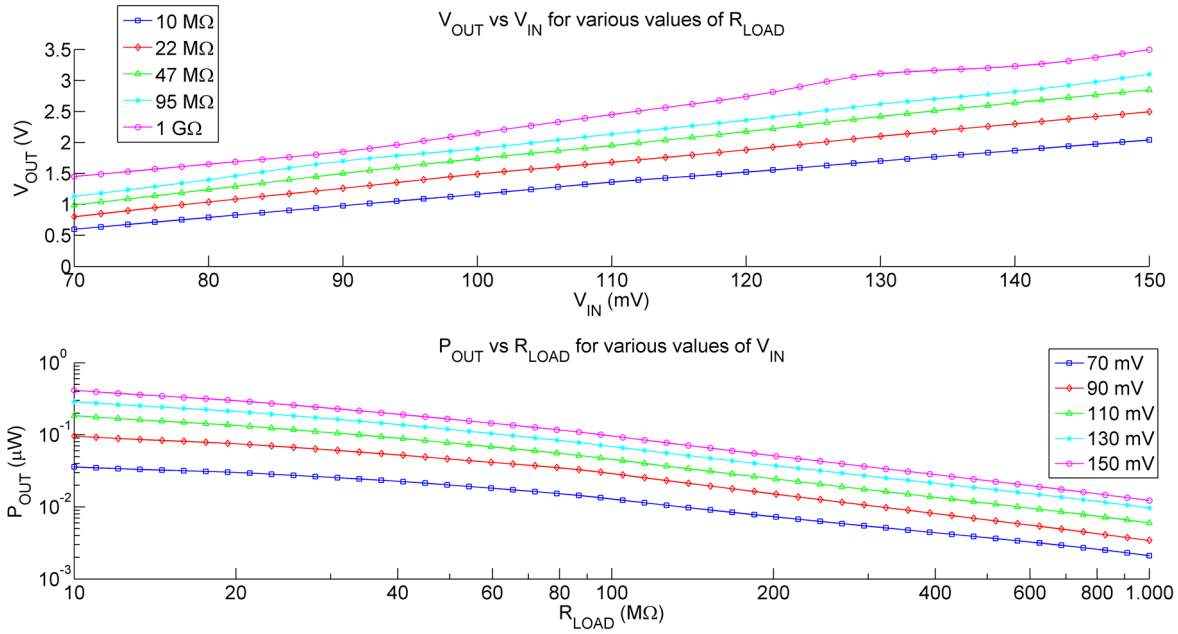


Fig. 10. (a) Measured steady-state output voltage V_{OUT} as a function of source voltage V_{IN} for various loads. (b) Measured output power P_{OUT} as a function of R_{LOAD} for various V_{IN}.

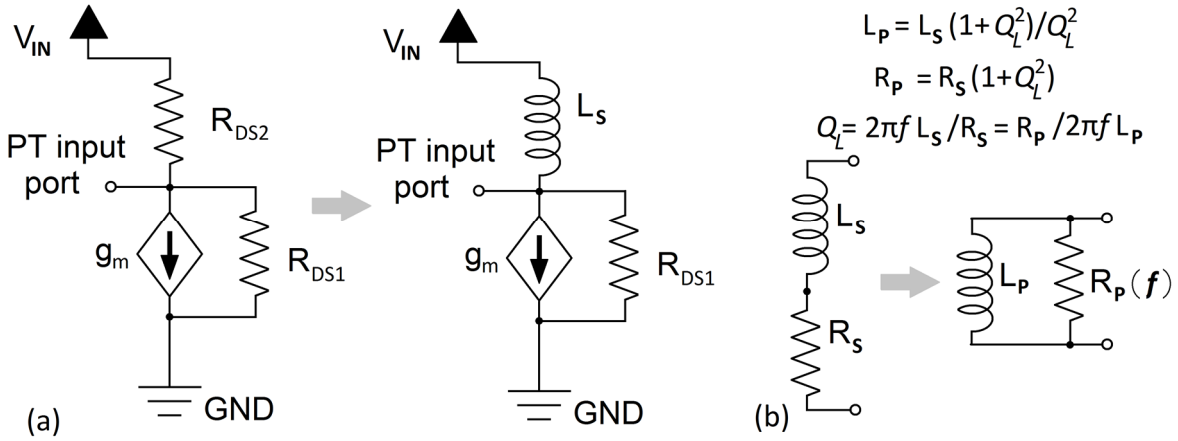
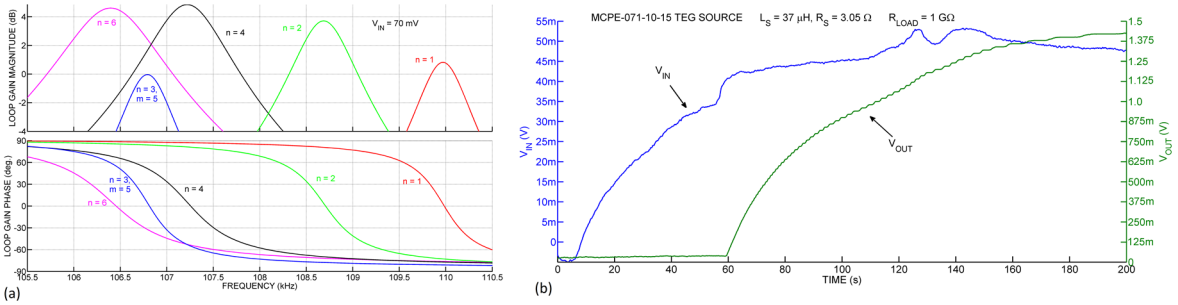


Fig. 11. a) Replacement of the load JFETs with a generic lossy inductor L_S. b) Equivalence of the series $L_S - R_S$ circuit with the parallel $L_P - R_P$ at a given frequency.



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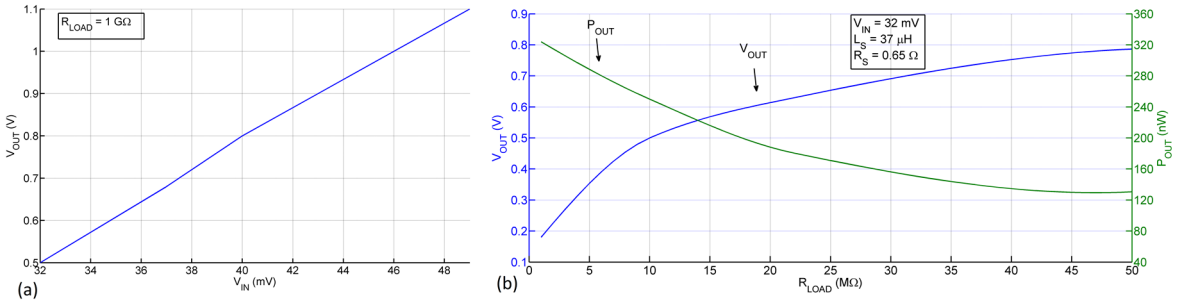

Fig. 13. (a) Measured steady-state output voltage V_{OUT} as a function of source voltage V_{IN}: the slope is 35.3 mV/mV, higher than the one obtained with load JFETs. (b) Measured V_{OUT} and P_{OUT} as a function of R_{LOAD}, with V_{IN} = 32 mV, L_S = 37 µH, R_S = 0.65 Ω. The optimum load resistance maximizing P_{OUT} is lower than 1 MΩ, whereas higher load resistances maximize V_{OUT}.

TABLE I: CIRCUIT SMALL SIGNAL PARAMETERS

Parameter	Value
C_{d1}	231 nF
C_M	11 nF
R_M	363 mΩ
L_M	0.247 mH
C_{d2}	19.2 pF
N	47.2
Q	453
$C_{GS} + C_{GD}$ (f = 100 kHz)	9 - 11 pF
V_P	~ – 0.85 V
R_{DS} (V_{DS} = 0.1 V)	663 - 731 Ω
g_m (V_{DS} = 0.1 V, V_{GS} = 0 V)	165 - 175 µA / V
I_{DSS}	~ 590 µA
$I_{leakage}$ (V_{DS} = 0.1 V, $V_{GS} = V_P$)	< 1 µA
$\beta_n = I_{DSS} \cdot V_P^2$	~ 426 µA / V^2
$C_{SCHOTTKY}$	~ 3 - 4 pF
C_{PUMP}	470 pF
C_{STORE}	4.7 µF

Table I: Small signal parameters involved in the mathematical model, useful to find minimum activation voltage of the converter.