Optimization of a Pocketed Dual-Metal-Gate TFET by Means of TCAD Simulations Accounting for Quantization-Induced Bandgap Widening

Optimization of a Pocketed Dual-Metal-Gate TFET by means of TCAD Simulations Accounting for Quantization-Induced Bandgap-Widening

Giovanni Betti Beneventi, *Member, IEEE,* Elena Gnani, *Member, IEEE,* Antonio Gnudi, *Member, IEEE,* Susanna Reggiani, *Member, IEEE,* and Giorgio Baccarani, *Life Fellow, IEEE.*

***Abstract*—A Dual-Metal-Gate (DMG) Tunnel FET integrating a heavily-doped pocket within the channel is optimized through TCAD simulations by taking into account quantization-induced bandgap-widening. First, the performance penalty due to the reduced tunneling probability is estimated; next, device design options to minimize the negative impact of quantization on the DMG-TFET performance are assessed.**

***Index Terms*—Tunnel Field-Effect Transistors (TFET), Band-to-Band Tunneling (BTBT), Steep Subthreshold Slope (SSS), Quantization, Dual-Metal-Gate, Pocket, Line-TFET, InAs.**

I. Introduction

TO limit power consumption of next-generation digital systems, transistors with inverse subthreshold slope SS $\simeq$ 45 mV/dec or lower, on at least three decades of drain current, are needed [1]. However, Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) cannot provide an SS lower than 60 mV/dec at room temperature, since charge injection in the device occurs by thermionic emission, a mechanism governed by the exponential tail of Fermi statistics [2]. Thus, to obtain steeper SS, new device concepts are needed. Among them, one of the most investigated is the Tunnel Field-Effect-Transistor (TFET). In *n*-type TFETs, injection of carriers relies on Band-to-Band Tunneling (BTBT) of electrons from the source valence band into the channel (CH) conduction band, so that high-energy carriers belonging to the exponential tail of Fermi statistics are filtered out by the semiconductor bandgap. For this reason, SS lower than 60 mV/dec can be achieved [3]. However, despite the high TFET potential, some issues must still be addressed, namely: (i) achieving SS lower than 60 mV/dec over a significant number of drain-current decades is a challenge, even if steep slopes are theoretically possible; (ii) the TFET on-state current ($I_{\rm ON}$) is routinely lower than MOSFET's $I_{\rm ON}$. In order to mitigate these issues, TFETs must be carefully engineered in terms of both material choice and device architecture.

More specifically, in order to enhance $I_{\rm ON}$, the integration of a highly-doped pocket (P) extending the source region into the transistor CH may be envisaged [4]. The P increases both the tunneling area and the tunneling probability, which benefits from the alignment of the tunneling path to the electric field. On the other hand, a high electric field requires a significant doping gradient at the P-junction, thereby originating a thin potential well. Quantization effects can thus occur within the well, owing to both built-in structural, and gate-induced quantum confinement (QC). In turn, the latter yields bandgap-widening, which adversely affects the BTBT probability, and is thus expected to reduce the benefits of the P integration.

In this framework, device simulation plays a crucial role in investigating pocketed TFETs, providing a guidance to the manufacturing efforts that might be undertaken to fabricate such pockets in real TFETs. This manuscript investigates QC arising in a Dual-Metal-Gate (DMG) TFET integrating a highly-doped P in the CH. QC could be rigorously calculated using a 3D Schrödinger-Poisson solver. However, the computational burden of such a solver is considerably higher than admitted in TCAD. For this reason, simplified tools allowing us to effectively mimic the effects of QC, and that can be easily integrated in TCAD simulators, are highly desirable. In this paper we adopt a simple method to account for QC-induced bandgap-widening in pocketed TFETs: we couple a TCAD tool with a Schrödinger solver in suitable cross-sections, with the aim to optimize the performance of a promising DMG-TFET, previously studied without taking into account QC [5]-[7].

The paper is organized as follows. Section II briefly describes the DMG-TFET worked out in the first stage of device engineering, as well as the TCAD model employed for the preliminary device design. The performance of the DMG-TFET according to the initial TCAD model is also addressed. Section III is devoted to the description of the devised approach. Next, section IV discusses the impact of QC on the DMG-TFET characteristics, showing first the performance degradation due to bandgap-widening, and then describing the design countermeasures taken to mitigate the effects of QC. The resulting optimized device is then benchmarked and compared with literature. Finally, conclusions are drawn in section V.

II. DMG-TFET and TCAD model

The cylindrical DMG-TFET worked out by the initial TCAD-based approach (hereafter "semiclassical" DMG-TFET) is summarized in Fig. 1 (a) and the caption therein. A detailed analysis of the steps leading to the optimization of the semiclassical DMG-TFET is given in [5].

This work was supported in part by the EU E2SWITCH under Grant 619509 and in part by the Italian Ministry of University and Research through the "Futuro in Ricerca" Project FIRB 2010. The authors are with ARCES and DEI, University of Bologna, Viale del Risorgimento 2, 40136, Italy. (e-mail: giobettibeneventi@gmail.com ; giovanni.betti2@unibo.it)

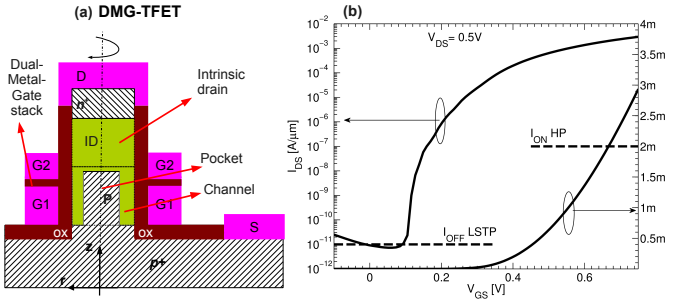

Fig. 1: (a) Schematic cross-section (not drawn to scale) of the vertical 10 nm-radius cylindrical Dual-Metal-Gate (DMG)-TFET. r is the radial coordinate, z the vertical coordinate; S, G, D are the source, gate and drain contacts, respectively; P is the pocket; ox stands for oxide (Al_2O_3). S is p^+-doped at 7×10^{19} cm^{-3}, channel length is 40 nm, D is n^+-doped at 5×10^{18} cm^{-3}, and ox thickness t_{ox} is 1.6 nm, corresponding to the Equivalent Oxide Thickness (EOT) of High-Performance (HP) 2020 International Technology Roadmap for Semiconductors (ITRS) specs. Pocket (length = 35 nm, radius = 6 nm) is p^+-doped at 7×10^{19} cm^{-3}, as S; intrinsic drain (ID) length is 100 nm, first gate (G1) length is 30 nm, second gate (G2) length is 25 nm; G1 and G2 are separated by a 3 nm gap; G1 has the same workfunction as the semiconductor (InAs), while G2's workfunction is 100 mV higher. (b) Turn-on characteristics of semiclassical DMG-TFET at $V_{DS} = 0.5$ V. The I_{OFF} and I_{ON} requirements of the 2020 ITRS Low-Standby-Power (LSTP) and High-Performance (HP) specs, respectively, are indicated by horizontal lines.

A. The TCAD model

Being the NW longer than 100 nm, carrier transport is simulated by the semiclassical drift-diffusion equations. For InAs, only direct BTBT is assumed to occur, and is simulated as a dynamic non-local generation-recombination mechanism according to the well-established Kane's theory of tunneling for uniform fields [14], extended for arbitrary band profiles in the employed Synopsys Sentaurus Sdevice simulator [15]. In the simulations, Fermi statistics is also activated, as well as a doping-dependent mobility model [16]. The InAs parameters of the BTBT model were fitted by comparison with simulation results of InAs TFETs performed with the $\boldsymbol{k}\cdot\boldsymbol{p}$ technique [8]. In the following, drain-current values are normalized to the NW diameter (occupation-area criterion) [17], and the ITRS specs for multi-gate transistors projected to year 2020 are used as performance benchmark. When the device performance is compared with ITRS, the off-state gate voltage $V_{GS,OFF}$ is chosen as the V_{GS} corresponding to the I_{OFF} value prescribed by the roadmap; then, I_{ON} is identified as the current corresponding to the on-state gate voltage $V_{GS,ON} = V_{GS,OFF} + V_{DD}$. V_{DD} is always set to 0.5 V, and simulations of turn-on characteristics were carried out with drain voltage $V_{DS} = V_{DD} = 0.5$ V.

B. Switching characteristics of semiclassical DMG-TFET

The switching characteristics of the optimized DMG-TFET proposed in [5] are illustrated in Fig.1 (b), where the turn-on drain-current I_{DS} vs. gate-voltage V_{GS} is shown. At this stage, no QC is included in the model. DMG-TFET fulfills both the I_{OFF} and I_{ON} requirements of the Low-STandby-Power (LSTP) and HP 2020 ITRS specs, respectively, with a reduction of 25% in the power consumption compared to the roadmap. Moreover, the average SS (computed from $V_{GS,OFF}$ up to threshold on about 7 decades of drain current) is as low as 43 mV/dec, with a minimum slope of 6 mV/dec, sustained across one I_{DS} decade, or more [5].

III. A NEW TCAD APPROACH TO ACCOUNT FOR QUANTUM CONFINEMENT IN TFETS

A. Motivation and literature review

The DMG-TFET channel radius R was set to 10 nm. For such R, and uniform semiconductor, the effect of QC on the BTBT probability is negligible, as will be shown in the following. However, once a heavily-doped P is integrated in the device structure, the band bending along the device radial coordinate due to doping gradient gives rise to a thin triangular-like potential well for electrons near the oxide interface; furthermore, the well depth increases with the applied positive gate voltage, yielding an additional field-induced contribution to QC. Besides, the P acts as a potential well for holes. Therefore, the Schrödinger equation must be solved self-consistently with Poisson's equation.

QC basically leads to two effects: (i) the formation of sub-bands, leading to an increased material bandgap, and (ii) the reshaping of the free charge distribution [19]. In recent literature, some authors have contributed to the understanding of QC occurring in pocketed or pocketed-like TFETs (also called "Line"-TFETs) using quantum approaches [20]- [23]. These studies essentially highlight that: (i) QC yields a threshold voltage increase [21]; (ii) QC significantly deteriorates I_{ON} due to bandgap-widening [21]; (iii) nevertheless, pocketed TFETs can feature better performance than conventional TFETs even when QC is accounted for [20].

However, such models can hardly be employed for device optimization, especially in the case of complex device geometries such as that of the DMG-TFET. In addition, they do not usually calculate the BTBT current self-consistently. Rather, the latter is evaluated in a post-processing computation based on the band diagram provided by the numerical solution of the Schrödinger-Poisson problem. Thus they apply only when I_{ON} is low [21], [23][1].

In TCAD simulators, QC is usually accounted for by the density-gradient model, which describes the modified spatial distribution of charge density, but neglects bandgap-widening [19]. On the other hand, bandgap-widening is probably the most important effect in TFETs, since a bandgap increase corresponds to an exponential decrease of the BTBT probability and, hence, of the drain current. Moreover, it is difficult to achieve convergence when the density-gradient is activated together with the dynamic non-local BTBT model [24]. Therefore, in order to take into account QC in our TCAD simulations, we concentrated on bandgap-widening and implemented the following simple procedure, hereafter referred to as "quantum-TCAD" simulation approach.

B. The quantum TCAD model

We first identified the device regions where QC is expected to be relevant, that is, where the P is surrounded by gates: the

[1]A Schrödinger solver that could be used in a quantum drift-diffusion scheme [19] is also available in Sdevice, but it is known to frequently cause convergence issues; the solver is indeed conceived as a calibration tool to be applied to simpler device architectures and at low currents [15].

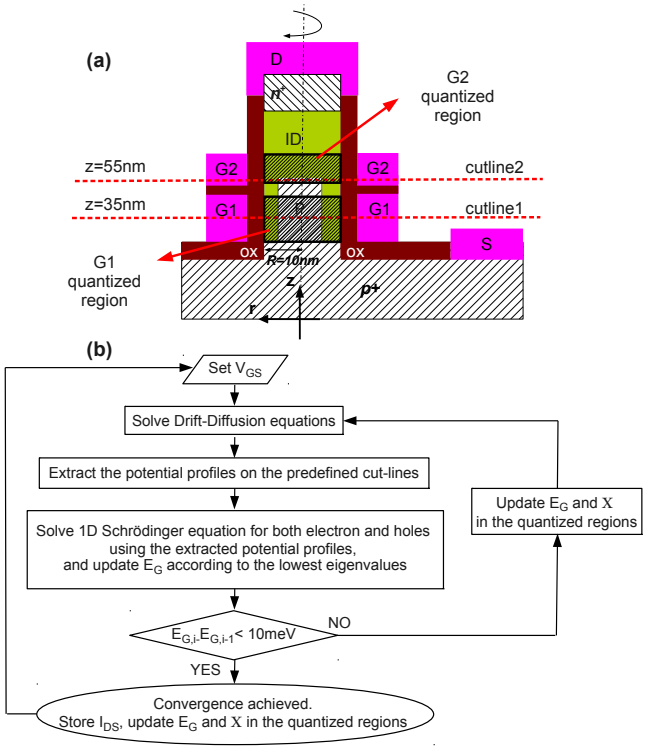

Fig. 2: (a) Pictorial illustration (not drawn to scale) of the cutlines ($z = 35$ nm, $z = 55$ nm) where the band edges are extracted to enter the cylindrical Schrödinger equation. The two corresponding "quantized regions" are the regions delimited by the black rectangles. (b) Self-consistent loop employed in our quantum-TCAD simulations. The combined TCAD-Schrödinger loop continues until $E_{\mathrm{G,i}} - E_{\mathrm{G,i-1}} < 10$ meV, where $i-1$ and i indicate successive iterations and E_{G} is the bandgap.

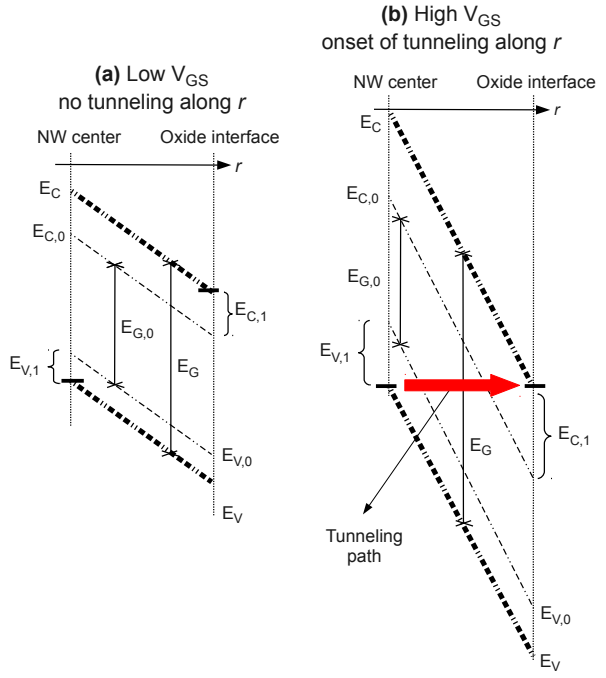

Fig. 3: Simplified band profiles along r in a quantized region: semiclassical (dashed thinner lines) vs. quantum case (dashed thicker lines) (a) At low V_{GS} no direct tunneling window is present. (b) At high V_{GS} corresponding to the onset of tunneling in radial direction, direct BTBT tunneling is triggered by band alignment. In the sketch, $E_{\mathrm{G},0}$, $E_{\mathrm{C},0}$ and $E_{\mathrm{V},0}$ are the bandgap, the conduction band energy and the valence band energy, respectively, in the unquantized case; $E_{\mathrm{C},1}$ and $E_{\mathrm{V},1}$ are the lowest eigenvalue calculated by the Schrödinger solver, thus E_{C} and E_{V} are the "quantized" bands, and E_{G} is the "quantum" bandgap.

so-called G1 and G2 "quantized" regions are thus indicated in Fig, 2 (a). It is worth noticing that QC for electrons is expected to be stronger in the G1 region, since Φ_{G2} is higher than Φ_{G1}. In fact, while G1 is a midgap metal-gate, Φ_{G2} is higher then Φ_{InAs}. This means that band bending in the G2 region will be less favorable for electron accumulation (shallower potential well). Therefore, we calculated QC separately in the two regions. In order to do so, the 1D potential profiles corresponding to the valence and conduction bands in each region (cutlines at constant z) must be extracted and fed into the Schrödinger equation. We set the first cutline to be located half-way the P sidewall in the G1 region ($z = 35$ nm), and the second one to be located in proximity of the P upper-junction, inside the pocket region aligned with G2 ($z = 55$ nm), see Fig. 2 (a).

After defining the two cutlines, the following self-consistent loop is applied, as illustrated in Fig. 2 (b). First, a semiclassical solution is performed. Afterwards, potential profiles along the two cutlines are extracted and fed into an in-house developed cylindrical Schrödinger solver. The Schrödinger equation is separately solved for electrons (using the conduction band potential profile) and for holes (using the valence band potential profile). The wavefunctions penetration in the oxide region are taken into account[2]. Next, the lowest conduction subband energy, referred to as the conduction band edge ($E_{\mathrm{C},1}$) and the highest valence subband energy, referred to as the valence band edge ($E_{\mathrm{V},1}$) are used to widen the InAs bandgap E_{G}, according to $E_{\mathrm{G}} = E_{\mathrm{G},0} + E_{\mathrm{C},1} + E_{\mathrm{V},1}$, where $E_{\mathrm{G},0}$ is the InAs bulk energy gap. Then, the InAs electron affinity is correspondingly lowered by the conduction band eigenvalue as $\chi = \chi_0 - E_{\mathrm{C},1}$, where χ_0 is the InAs bulk electron affinity. The above calculations are obviously performed at both cutlines, and the new calculated E_{G}s and χs are assigned to the two regions. A gaussian smoothing of bandgap and affinity values between the two regions and between the two regions and S and ID is applied to enhance convergence; bulk parameters are instead used at S, ID and D. The combined TCAD-Schrödinger loop continues until $E_{\mathrm{G,i}} - E_{\mathrm{G,i-1}} < 10$ meV, where $i-1$ and i indicate successive iterations. Thus, when the above condition is fulfilled, convergence is considered to be achieved, and the procedure is repeated for increased V_{GS} to obtain the device turn-on characteristics. The 1D Schrödinger solver is very quick, practically unaffecting the overall simulation time. In our approach, we essentially assume that BTBT can be modeled as in the bulk case, but with a widened bandgap due to quantization. We solve the Schrödinger equation to account for bandgap-widening, but the density of states is treated semiclassically, i.e., it is assigned to the lowest (highest) eigenvalues of the conduction (valence) band, and the subband structure is otherwise neglected. A somehow similar approach, where the energy eigenvalues are used to modify the band diagram, has recently been proposed by *Walke et al.* [26]. However, in [26], the modification of the band diagram (ascribed to the shift of the conduction band only) is empirically assumed to occur only within about 1 nm from

[2] Al_2O_3 parameters: electron affinity $= 2.58$ V, bandgap $= 6.65$, $m_{\mathrm{e}}^* = m_{\mathrm{h}}^* = 0.28\ m_0$ [25]

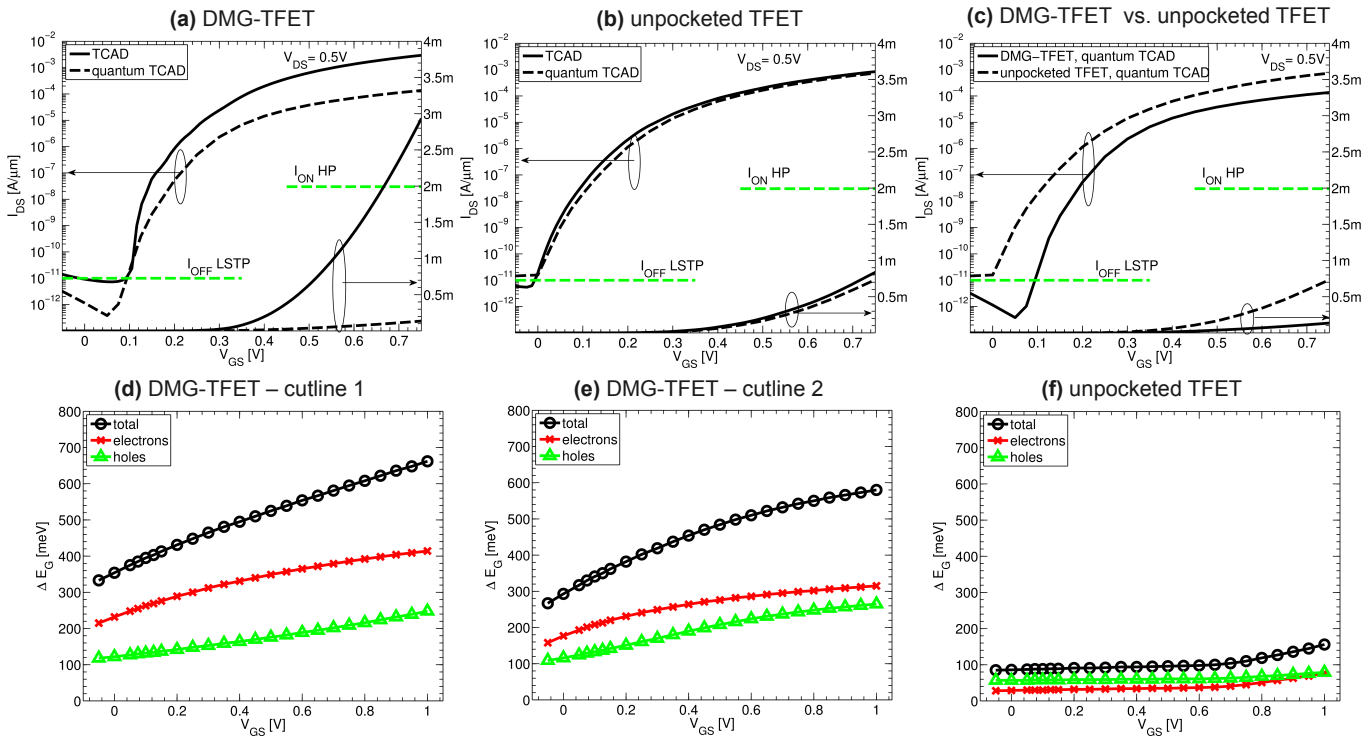

Fig. 4: (a). Turn-on characteristics of DMG-TFET according to TCAD and quantum-TCAD models. (b) Turn-on characteristics of unpocketed TFET according to TCAD and quantum-TCAD models. (c) Comparison of turn-on characteristics of the DMG-TFET and unpocketed TFET according to quantum-TCAD model. (d) $\Delta E_{\rm G} = E_{\rm G} - E_{\rm G,0} = E_{\rm C,1} + E_{\rm V,1}$ as a function of $V_{\rm GS}$ for the cutline 1 in DMG-TFET. The single contribution of electrons ($E_{\rm C,1}$) and of holes ($E_{\rm V,1}$) is displayed, (e) $\Delta E_{\rm G}$ as a function of $V_{\rm GS}$ for the cutline 2 in DMG-TFET, (f) $\Delta E_{\rm G}$ as a function of $V_{\rm GS}$ for a single cutline ($z = 40$ nm) for the unpocketed TFET.

the semiconductor-oxide interface.

Fig. 3 provides a qualitative illustration of the employed method by showing a simplified band structure in both the bulk and quantized case along one of the aforementioned cutlines. Fig. 3 (a) shows a low-$V_{\rm GS}$ case, where P does not contribute to BTBT despite QC, since band bending does not provide a direct-tunneling window. Due to the formation of a thin triangular well for both electrons and holes, we verified that the electron eigenvalue is higher than the hole eigenvalue, even if the electron effective mass is higher[3]. Fig. 3 (b) shows instead a higher $V_{\rm GS}$ case corresponding to the onset of direct BTBT due to alignment of the first eigenvalues of the valence and the conduction bands. As shown, the bandgap increase due to QC is expected to shift the onset of radial tunneling at the P sidewalls to higher $V_{\rm GS}$ values, thus increasing the transistor threshold voltage, the length of the tunneling path and reducing BTBT compared to the semiclassical case at the same bias.

IV. Optimization of a DMG-TFET by means of quantum TCAD

A. Semiclassical DMG-TFET according to quantum-TCAD

Fig. 4 (a) compares the turn-on characteristics of the DMG-TFET according to the semiclassical and quantum-TCAD models. As expected, the latter solution yields both a decreased off- and on-state currents, owing to bandgap-widening[4]. However, while the semiclassical $I_{\rm OFF}$ was already targeting the 2020 LSTP ITRS specs, $I_{\rm ON}$ is reduced by a factor of about 20 at $V_{\rm GS} = 600$ mV, and does not fulfill the HP requirements anymore. In order to understand the P role in QC, we simulate a device with the same features of the DMG-TFET, but without the P extrusion in the CH (hereafter, unpocketed TFET). Also, one single 40 nm gate is assumed, and only one cutline located at the center of the CH ($z = 40$ nm) is used to compute QC. Results are displayed in Fig. 4 (b), showing the turn-on of the unpocketed device, according to both semiclassical and quantum-TCAD. If no P is present, QC is negligible; the calculated $E_{\rm C,1}$ and $E_{\rm V,1}$ are close to the eigenvalues given by the analytical solution of the Schrödinger equation applied to a 2D circular potential box [18]: $E_{\rm C,1} = 32$ meV, $E_{\rm V,1} = 96$ meV.

Fig. 4 (c) thus compares the turn-on characteristics of the DMG and unpocketed TFETs according to quantum TCAD. It is worth noticing that the on-state current of the unpocketed device is sensibly *higher* than that of the DMG-TFET. These results highlight that, if QC is strong enough, the technological effort required to integrate a highly-doped P in the CH does not pay back, or even yield a detrimental effect on the device performance.

These conclusions are confirmed by Figs. 4 (d), (e) and

[3]Electron and light-hole InAs effective masses are $m_{\rm e}^* m_0 = 0.070\ m_0$ and $m_{\rm h}^* m_0 = 0.023\ m_0$, respectively [15], where m_0 is the free electron mass. The relatively high $m_{\rm e}$ is adopted to take into account the non-parabolicity of the InAs conduction band.

[4]Minimum $I_{\rm DS}$ is due to the device thermionic plateau, which is reduced in the quantized case mainly due to the formation of an energy barrier at the S-CH junction.

(f), displaying the bandgap-widening $\Delta E_{\mathrm{G}} = E_{\mathrm{G}} - E_{\mathrm{G},0} = E_{\mathrm{C},1} + E_{\mathrm{V},1}$ as a function of V_{GS} for the first and second cutlines in the DMG-TFET, and for the single cutline of the unpocketed TFET, respectively. The single contribution of electrons ($E_{\mathrm{C},1}$) and holes ($E_{\mathrm{V},1}$) to the bandgap-widening are displayed as well. As expected, a stronger bandgap increase is found for the DMG-TFET, where $\Delta E_{\mathrm{G}} \sim 700\,\mathrm{meV}$ at high V_{GS}, meaning that the quantized bandgap is about a factor of 3 wider than the bulk InAs one ($E_{\mathrm{G},0} \simeq 355\,\mathrm{meV}$). On the other hand, no significant bandgap increase is found in the unpocketed device. A stronger QC is found for the first cutline, compared to the second one, mainly due to the different electron contribution. This effect is explained by the difference between Φ_{G1} and Φ_{G2}, as already discussed. Then, QC for electrons is always stronger than for holes due to the positive gate voltage. Further insights are illustrated in Fig. 5. Fig. 5 (a) shows the band profiles along the radial coordinate ($z = 35\,\mathrm{nm}$, first cutline) at high $V_{\mathrm{GS}} = 1\,\mathrm{V}$ calculated with the TCAD and quantum-TCAD tools for the DMG-TFET. The quantized case clearly accounts for the tunneling barrier and tunneling path increase, the reduced tunneling window, as well as the electric-field increase due to the reduced electron concentration at the surface. Fig. 5 (b) plots BTBT generation rates (BTBT-GR) at the same bias, comparing the DMG and the unpocketed TFETs. It is clear that the unpocketed device features a *larger* tunneling area at the S junction where BTBT-GR is highest. On the other hand, the highest BTBT-GR in the DMG-TFET is located instead at the thinner P upper-junction, and is given by longitudinal tunnel from P to intrinsic drain (ID) region. The contribution of the transverse tunneling at the P sidewall is much lower, resulting in a detrimental effect of P on the overall device performance.

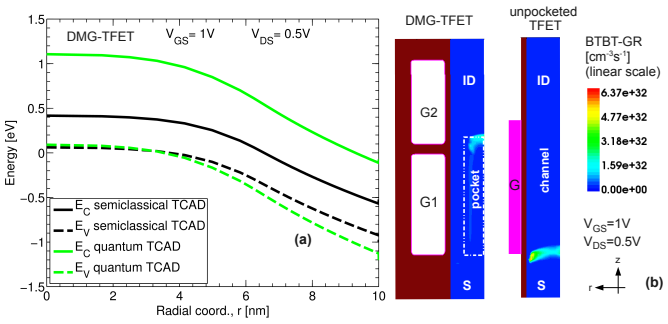

Fig. 5: (a) Band profiles taken along the first cutline ($z = 35\,\mathrm{nm}$) for the DMG-TFET according to TCAD and quantum-TCAD at $V_{\mathrm{GS}} = 1\,\mathrm{V}$. (b) Comparison of Band-To-Band-Tunneling generation rates (BTBT-GR) at same bias for the DMG-TFET (left) and unpocketed TFET (right); figure is not to scale, only half of the device cross-section is shown because of symmetry, only the part of the device in which BTBT-GR is significant is illustrated. The colormap of BTBT-GR is same for both devices and is displayed in linear scale.

B. Countermeasures to mitigate quantization issues

In the latter paragraph we have explained how QC can negatively impact the pocketed TFET performance. In this paragraph we re-work the DMG-TFET structure using the quantum-TCAD simulator, in order to mitigate these issues. At first, we increase the DMG-TFET radius, while keeping fixed the P radius at 6 nm. This solution has both a positive and a negative effect on tunneling. On the positive side, the triangular-like potential well at the InAs-oxide interface is widened and the electric field at the P sidewall junction is lowered due to the increased distance from the interface; these features are expected to reduce QC and, hence, bandgap-widening, thereby exponentially increasing BTBT. On the other side, a decreased electric field at the junction is expected to exponentially reduce BTBT. The quantitative outcome of this trade-off is illustrated in Fig. 6 (a), where the DMG-TFET I_{DS} (left) and ΔE_{G} (right) are shown as a function of the device radius ($V_{\mathrm{GS}} = 0.7\,\mathrm{V}$). The best result, i.e. the current maximum value, corresponds to $R = 16\,\mathrm{nm}$, featuring a current increase in excess of a factor of 3 compared to the $R = 10\,\mathrm{nm}$ case. For radii in the range between 10 and 16 nm, the device current mainly benefits from the lower bandgap widening, which, for $R = 16\,\mathrm{nm}$, is about one half of the corresponding value for $R = 10\,\mathrm{nm}$. For radii larger than 16 nm, the current decreases as the electric-field lowering at the junction dominates BTBT. This effect is depicted in Fig. 6 (b), where the electric field modulus at the P sidewall junction is shown to be reduced for $R = 20\,\mathrm{nm}$ compared to the $R = 16\,\mathrm{nm}$ case. Therefore, $R = 16\,\mathrm{nm}$ is assumed to be the optimum radius. The BTBT-GR is illustrated in Fig. 6 (c) for $R = 10\,\mathrm{nm}$ and $R = 16\,\mathrm{nm}$, highlighting the advantage of the latter case.

To further increase I_{ON}, the integration in the device CH of an uniform n-type-doped Pocket Buffer (PB) surrounding the p^+-doped P might be envisaged [27], see Fig. 7 (a). A doped PB should enhance the electric field at the junction by increasing the doping gradient, but could also be expected to increase the QC due to the augmented well steepness. Thus, to quantitatively assess the effect of the PB, quantum-TCAD simulations varying PB doping are performed; the turn-on of devices having n^+-doping in the range from $5 \times 10^{18}\mathrm{cm}^{-3}$ to $10^{19}\mathrm{cm}^{-3}$ are shown in Fig. 7 (b). The drain current increases with heavier doping levels due to the electric-field boosting, but the off-state current increases as well consistently with the lower threshold voltage.

Doping is also beneficial in enhancing the curve steepness, as can be seen by comparing the turn-on curves of the devices with and without PB doped, in the former case, at $5{\times}10^{18}$ cm^{-3}. On the other hand, no major SS modification is found in the explored PB doping range. We notice that $10^{19}\mathrm{cm}^{-3}$ can be considered the PB optimal doping, since the corresponding I_{OFF} is at the limit of the LSTP specs, as shown in the figure. A higher doping would further enhance I_{ON}, but it would also increase I_{OFF} above the ITRS requirement. The n-doping effect is illustrated in Fig. 7 (c) and (d), where band diagram on the radial coordinate and BTBT-GR are compared for the DMG-TFET (no PB) and the device with PB doped at $10^{19}\mathrm{cm}^{-3}$. These devices are compared at $V_{\mathrm{GS}} = 350\,\mathrm{mV}$, where the difference in I_{DS} is largest. The doped device features a higher band bending at the P-junction, thus increased electric field, reduced tunneling path and increased tunneling window. On the other hand, no bandgap increase due to the higher doping gradient is found. This is probably related to the modification of the triangular-

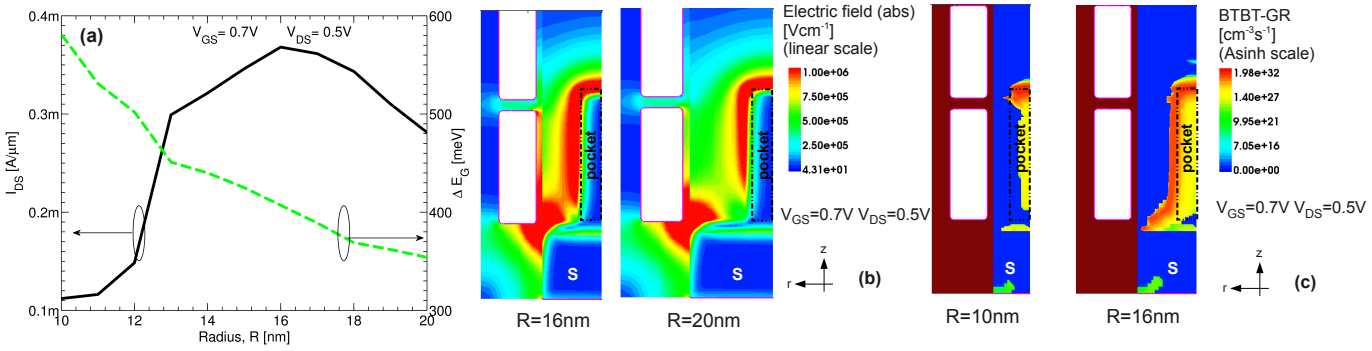

Fig. 6: (a) I_{DS} (left) and ΔE_{G} (right) as a function of device radius (P radius fixed at 6 nm as it was in the TCAD-designed DMG-TFET); (b) Modulus of the electric field for $R=16$ nm (left) and $R=20$ nm (right), not to scale; (c) Comparison of BTBT-GR (Asinh scale) for $R=10$ nm (left) and $R=16$ nm (right), not to scale.

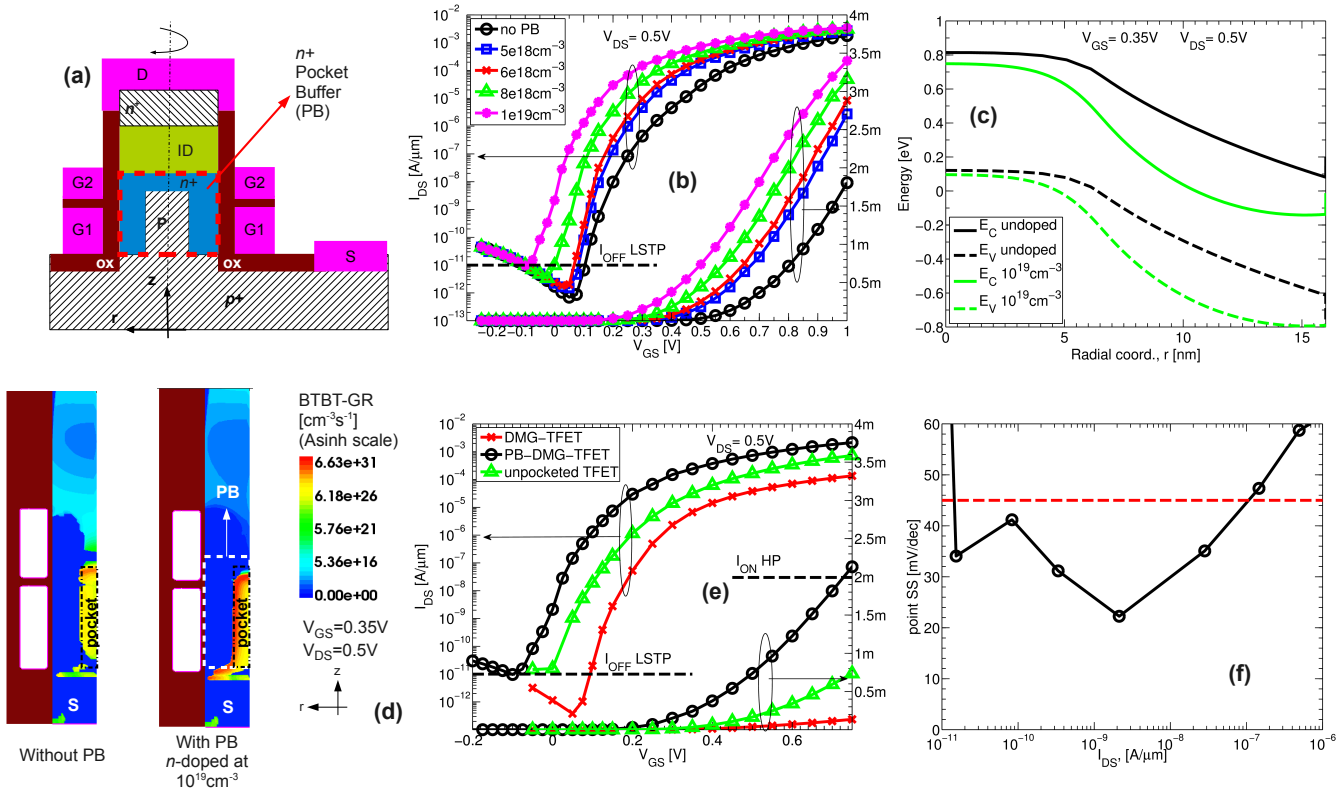

Fig. 7: (a) sketch (not to scale) of the cross-section of the DMG-TFET in which an uniformly n-doped pocket-buffer (PB) is integrated in the channel. (b) turn-on characteristics varying PB doping ($R=16$ nm for all devices). (c) Band diagram displayed along r at $z=35$ nm for the device without PB and for the transistor with PB doped at $1\times10^{19}\mathrm{cm}^{-3}$ at $V_{\mathrm{GS}}=0.35$ V. (d) BTBT-GR at same bias for both aforementioned devices, PB region, is delimited by the dashed rectangle, not to scale. (e) comparison of turn-on characteristics of TCAD optimized DMG-TFET, quantum-TCAD-optimized DMG-TFET (PB-DMG-TFET, $R=16$ nm, n-doping $1\times10^{19}\mathrm{cm}^{-3}$), and unpocketed TFET according to quantum-TCAD. (f) Point SS as a function of I_{DS} for PB-DMG-TFET.

like shape of the well, which becomes wider and concave in the quantum case [see Fig. 7 (c)]. This insight is confirmed by inspection of Fig. 7 (d), which displays BTBT-GR at $V_{\mathrm{GS}}=350$ mV; it is clear that the PB doping is beneficial in triggering BTBT at the pocket sidewall. The turn-on curve of the TCAD-designed DMG-TFET is compared with that of the quantum-TCAD-optimized DMG-TFET ($R=16$ nm and PB doped at $10^{19}\mathrm{cm}^{-3}$), hereafter indicated as PB-DMG-TFET, and with the unpocketed TFET in Fig. 7 (e). The performance increase obtained from the size increase and PB doping is clear, with I_{DS} beyond 1 mA/μm at high V_{GS} (10-fold increase at $V_{\mathrm{GS}}=0.6$ V compared to the TCAD-optimized TFET). Also, the same device features a better performance than the unpocketed one, suggesting that, if well designed, P is worth integrating. However, I_{ON} is still too low to fulfill the ITRS 2020 specs by keeping $V_{\mathrm{DD}}=0.5$ V (for HP $I_{\mathrm{ON}}\sim930\,\mu$A/ μm vs. 1900 μA/μm of the specs; for Low-Operating-Power (LOP) $I_{\mathrm{ON}}\sim760\,\mu$A/$\mu$m vs. 784 μA/μm; for LSTP $I_{\mathrm{ON}}=380\,\mu$A/μm vs. 600 μA/μm). To conclude on the performance of the quantum-optimized device, Fig. 7 (f) shows point SS as a function of I_{DS}. PB-DMG-TFET features an SS lower than 60 mV/dec over nearly 5 decades of I_{DS}, and

lower than 45 mV/dec on about 4 decades of I_{DS}. The average SS calculated from V_{GS} corresponding to LSTP I_{OFF} specs up to threshold is about 55 mV/dec. Transistor intrinsic delay calculated according to LSTP, (LOP) and HP specs ranges from 2 ps (LSTP) to 0.8 ps (HP), slightly higher than required by the ITRS.

Device-optimization results are compared with literature in Fig. 8, where the turn-on characteristics of the DMG-TFET (i.e. the semiclassically-optimized device) and of the PB-DMG-TFET (i.e. the quantum-TCAD optimized device) are superimposed to other *simulated* TFET turn-on characteristics [3]. DMG-TFET and PB-DMG-TFET feature competitive performance, providing, at relatively modest $V_{\mathrm{DD}} = 0.5\,\mathrm{V}$, low I_{OFF} compliant with LSTP, steep slope, high I_{ON} and, probably the best $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$.

Finally, it is worth noticing that the role played by G2 in the PB-DMG-TFET is essentially the same played in the "semiclassical" DMG-TFET explained in [5]. That is, G2 reduces the tunneling contribution occurring mainly in the z-direction at the pocket upper-junction at low V_{GS}. Thus, thanks to the electrostatic control of G2, the PB-DMG-TFET switch-on is dominated by tunneling occurring in the radial direction at the pocket sidewalls. This is beneficial for the turn-on slope, since tunneling occurring in the radial direction is aligned to the electric field induced by the G1.

To conclude, from the quantization point of view, DMG-TFET and PB-DMG-TFET can probably be considered best and worst cases of the *intrinsic* performance of optimized dual-metal-gate TFET based on InAs. In fact, while the simulated DMG-TFET performance is probably overestimated by completely neglecting QC, the PB-DMG-TFET simulated performance most likely represents a worst-case analysis, one of the reasons being the assignment of the whole bandgap-widening calculated on the pocket along cutline 2 to the whole G2 quantized region. Concerning the heuristic approach we devised to incorporate bandgap widening into TCAD, it is worth pointing out that such an approach would need comparison and calibration with experimental data, in order to validate the obtained results and the device design. However, to the best of our knowledge, device structures with features suitable for direct comparison with our simulations (i.e. same material, sizes, doping concentration and steepness) have not been fabricated yet.

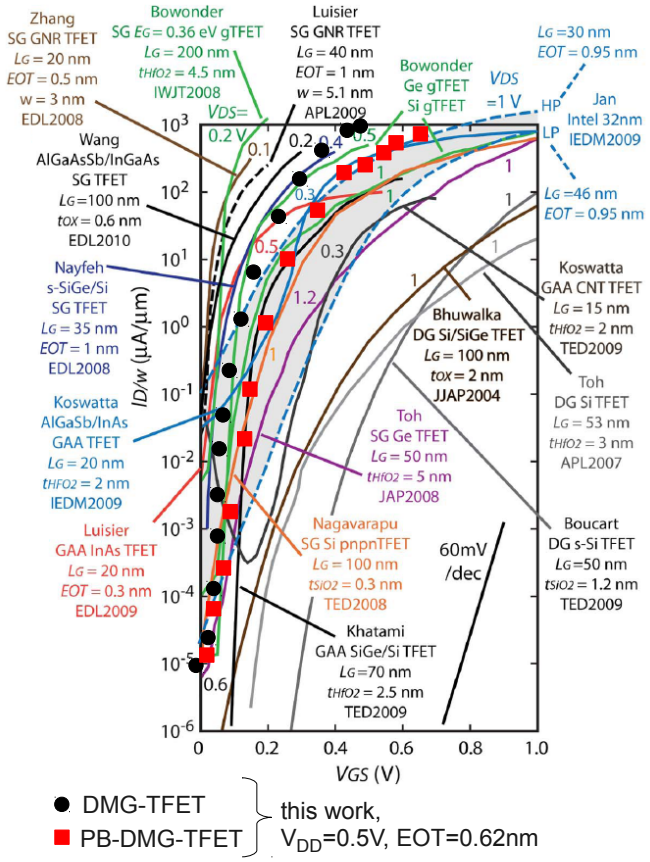

Fig. 8: Comparison between the turn-on characteristics of the TFET devices proposed in this work and other *simulated* curves taken from TFET literature (literature curves were presented in the review by *Seabaugh, et al.* [3]). In the plot, the supply voltages are annotated nearby the respective curves. Also, other device features, such as the EOT, are specified. Our results, obtained at $V_{\mathrm{DD}} = 0.5\,\mathrm{V}$ and EOT $= 0.62\,\mathrm{nm}$, are indicated in the graph with dots and squares. The dots represent the DMG-TFET, i.e. the device obtained through TCAD optimization without accounting for quantization, while the squares represent the PB-DMG-TFET, i.e the device resulting form optimization with quantum-TCAD. For easier comparison with the larger number of curves, the turn-on characteristics of our devices have been translated such that $I_{\mathrm{OFF}} \sim I_{\mathrm{OFF,LSTP}}$ occurs at $V_{\mathrm{GS}} = 0\,\mathrm{V}$.

V. Conclusion

A pocketed dual-metal-gate TFET has been optimized by means of TCAD simulations including quantization-induced bandgap-widening. A sufficiently large nanowire radius and the counterdoping of the pocket junctions are found to be crucial aspects to boost band-to-band tunneling from the pocket sidewalls, thus mitigating the reduction of tunnel probability due to bandgap-widening. With such an approach, pocket integration is proved to be truly beneficial to enhance the TFET turn-on curve steepness and the transistor on-state current.

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