Linearization Technique for CCO-based ADCs for AiMC MVM Architectures Using Resistive Memory Devices

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Andrea Lico, Marco Pasotti, Riccardo Zurla, Riccardo Vignali, Lorenzo Greco, Alessandro Cabrini, Eleonora Franchi Scarselli, Alessio Antolini

***Abstract*—This paper presents a design technique to linearize the frequency-to-conductance characteristic of a Current-Controlled Oscillator (CCO) within a CCO-based ADC used for Matrix-Vector Multiplication (MVM) in Analog in-Memory Computing (AiMC) accelerators. The proposed linearization is achieved by leveraging a bitline voltage regulator (BLVR), a circuit commonly employed to bias the bitlines (BLs) of computational resistive memory arrays. The BLVR utilizes a resistor and a copy of the bitline current to create a feedback mechanism that dynamically adjusts the bitline voltage in response to changes in the total bitline conductance (g_{BL}). This feedback reduces the oscillation period by an amount that linearizes the relationship between the CCO output frequency (f_{CCO}) and g_{BL}. Simulations in 28 nm FD-SOI technology demonstrate that the proposed BLVR reduces the quadratic coefficient k_2 of a polynomial approximation of the f_{CCO}–g_{BL} characteristic from 5.88×10^{-2} to 2.31×10^{-2}, corresponding to a $2.5\times$ improvement in linearity in the full conductance range.**

***Index Terms*—Analog in-Memory Computing (AiMC), Matrix Vector Multiplication (MVM), Current Controlled Oscillator (CCO)-based ADC, Bitline (BL) Voltage Regulation (BLVR).**

I. Introduction

THE growing demand for energy-efficient and high-throughput computing architectures has driven significant interest in Analog in-Memory Computing (AiMC) as a promising paradigm for accelerating Matrix-Vector Multiplication (MVM), a fundamental operation in machine learning and signal processing applications [1], [2]. AiMC architectures leverage resistive memory arrays to perform MVM directly within the memory, thereby minimizing costly data movement between memory and processing units and achieving substantial gains in speed and energy efficiency [3], [4].

In conventional AiMC systems, the matrix elements are encoded in the conductance values of non-volatile resistive memory devices, while the input vector is typically represented using pulse-width modulation (PWM) applied to the wordlines (WLs) of the memory array [1]. The resulting bitline (BL) currents must be integrated and accurately converted into digital values by ADCs to enable digital processing. This charge-to-digital conversion step is critical, as it directly impacts the computation accuracy and system performance [5]–[7].

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Conventional integrators combined with voltage-based ADCs, when employed in AiMC architectures, often require large integration capacitors and complex analog front-ends, which can limit scalability and increase latency [2]. To address these challenges, time-based ADCs, such as those employing Current-Controlled Oscillators (CCOs), have emerged as attractive alternatives. CCO-based ADCs convert input currents into oscillation frequencies, enabling compact, low-power, and high-speed conversion with a flexible trade-off between precision and latency [5], [8]. However, a well-known limitation of CCO is the nonlinearity introduced at high input currents due to fixed gate delays within the oscillator circuitry, which degrades the linear relationship between output frequency and input current [5], [9].

In this work, we propose a design technique that modifies the bitline voltage regulator (BLVR), the circuit responsible for biasing the memory array BLs, to linearize the CCO frequency-to-conductance characteristic. The key modification lies in introducing a resistor that, together with a scaled replica of the BL current, creates a feedback mechanism that dynamically adjusts the BL voltage in response to changes in the total BL conductance, effectively compensating for delay-induced nonlinearities in the CCO output frequency. This technique preserves the inherent advantages of time-based ADCs while significantly enhancing linearity without incurring substantial area or power overhead.

The paper is organized as follows. Section II reviews AiMC cores and charge-to-digital conversion. Section III details the proposed BLVR design for CCO linearization. Section IV outlines the design methodology. Section V presents simulation results. Section VI concludes the paper.

II. AiMC Core and Charge-to-Digital Conversion

The MVM $\mathbf{z} = \mathbf{G} \cdot \mathbf{x}$ can be directly performed within a resistive memory array of dimensions $n \times m$, as illustrated in Fig. 1 [5], [8]. Each matrix element $g_{i,j}$ is represented by the conductance stored in one resistive device. The N-bit elements x_i of the input vector $\mathbf{x} = [x_1, \ldots, x_n]$ are encoded as PWM intervals applied to the i-th wordline (WL). By biasing all m bitlines (BLs) with a voltage V_R and integrating the resulting currents $i_{BL,j}$ over time independently, m accumulated charges are obtained which are subsequently converted into M-bit digital values by the corresponding ADC. This process produces all the m elements z_j of the output vector $\mathbf{z} = [z_1, \ldots, z_m]$, which represents the result of the MVM operation.

In this context, the peripheral circuitry required for charge-to-digital conversion consists of two key components: a bitline

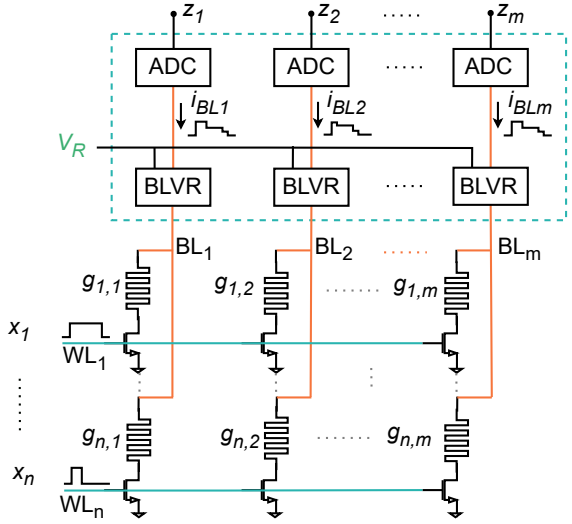

Fig. 1. Schematic of MVM performed within a resistive memory array. Input vector elements are encoded as PWM signals applied to the WLs, while the BLVR maintains a stable voltage on each BL during computation. The ADC performs the charge-to-digital conversion of the integral of the current signal.

voltage regulator (BLVR) and an ADC. A dedicated BLVR, which should be laid out within the pitch of a single resistive memory cell, is required for each bitline to maintain a stable voltage V_R during computation. Charge-to-digital conversion can be performed by the ADC integrating the BL current with a large capacitor followed by a conventional voltage-based ADC. Alternatively, current-controlled oscillator (CCO)-based ADCs eliminate the need for additional conversion cycles, offering a flexible trade-off between precision and latency. Additionally, by avoiding large integration capacitors and relying mainly on digital circuitry, this approach enables a dedicated A/D converter for each memory array column, avoiding resource sharing.

III. BLVR Design for CCO Linearization

The proposed implementation of the BLVR and the CCO-based ADC is illustrated in Fig. 2. The conductance g_{BL} represents the aggregate conductance of n resistive memory devices connected to a single BL node. Consequently, the BL current can be expressed as

$$i_{BL}(t) = V_{BL}\, g_{BL}(t). \tag{1}$$

Note that g_{BL} and, consequently i_{BL}, are time-dependent due to input variations during the MVM computation, as illustrated in Fig. 1. For conciseness, this time dependence is not explicitly indicated in the subsequent analysis.

The bit line voltage V_{BL} is driven by BLVR which is implemented using a Current-Voltage Mirror (CVM) composed of two pairs of coupled transistors (M1-M4, M2-M3) [13]–[15]. M2 and M3 are arranged as a current mirror to ensure $i' = \alpha i_{BL}$, where α is the mirroring factor of the coupled transistors; further, M1 and M4, sharing the same gate voltage and having matched drain currents, provide a voltage mirror that equalizes the voltages on BL and BL′. Therefore, neglecting the systematic voltage offset error caused by channel-length modulation affecting the CVM [15], [16], as shown in [17], the BL voltage becomes

$$V_{BL} = V_{BL'}. \tag{2}$$

A. BLVR and CCO Operation with Disabled Feedback

When the enable signal $EN_{LIN} = 0$, the voltage buffer forces $V_{BL'} = V_R$. As a result, the BLVR maintains

$$V_{BL} = V_R \tag{3}$$

within a specified range of g_{BL} variations. This ensures the BL current in (1) to be linearly proportional to g_{BL}.

A scaled copy of the bit-line current, $i'' = k\, i_{BL}$, is fed into a CCO to generate signal z_0 whose frequency is proportional to the current. The oscillation is controlled by two small equal capacitors, C, which are alternately charged until the voltage across either capacitor, L (or R), reaches the switching threshold voltage V_M of the corresponding inverter. This event toggles the latch state signals z_0 and $\overline{z_0}$, thereby digitizing the transfer of a fixed amount of charge into the circuit. The count of these charge units is tracked by a ripple counter.

Nevertheless, a key limitation of this CCO circuit is the nonlinearity of the output frequency f_{CCO}, with respect to the input current, which is critical at high current. This arises due to the gate delay t_D between the instant when L (or R) crosses the switching threshold voltage V_M of the corresponding inverter and the instant when $\overline{z_0}$ (or z_0) toggles up. Hence, $2t_D$ is added to the time period, T_{CCO}, of the output of the CCO (z_0):

$$T_{CCO} = \frac{1}{f_{CCO}} = \frac{2CV_M}{k\, i_{BL}} + 2t_D. \tag{4}$$

It is important to note that t_D depends only weakly on the input current i_{BL} [5], and is therefore treated as a constant in the subsequent analysis. This assumption is supported by simulation results presented in Section V. Substituting (1) into (4) yields the frequency as a function of the conductance:

$$f_{CCO} = \frac{kV_{BL}\, g_{BL}}{2CV_M + 2k\, t_D V_{BL}\, g_{BL}}. \tag{5}$$

This expression clearly shows the non linear dependence of f_{CCO} on g_{BL}.

B. Limitations of Existing Approaches

Several approaches have been proposed to address the delay-induced nonlinearity of CCO-based converters. These include limiting the operation to low-frequency regimes, where propagation delays have a negligible impact [10], as well as employing complex digital correction schemes such as look-up tables or other forms of post-processing [11]. In the context of AiMC systems, however, such solutions are generally impractical, as the post-processing compensation techniques are effective only for static current sensing and are unable to accurately correct errors arising from time-varying currents that are integrated over a time window, as illustrated in Fig. 1. Alternative circuit-level techniques, such as those presented in [5] and [12], tackle this issue by dynamically adjusting the effective threshold voltage to counteract delay effects, thereby improving the linearity of the CCO frequency characteristic.

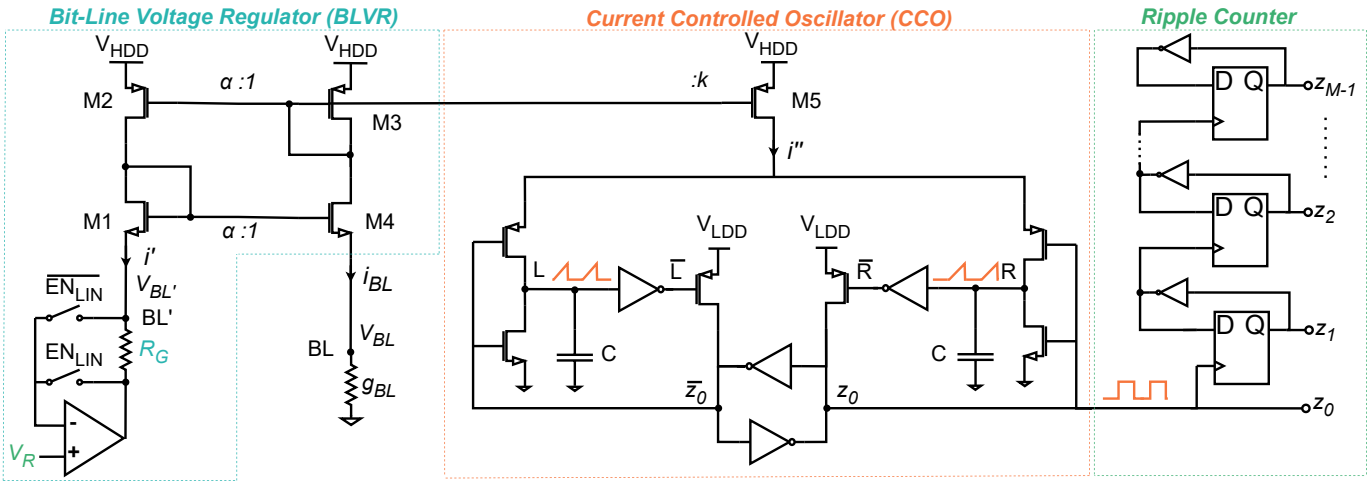

Fig. 2. Proposed bitline voltage regulator (BLVR) and current-controlled oscillator (CCO)-based ADC. The conductance g_{BL} represents the total conductance of n resistive memory devices connected to a single BL node. The BLVR equalize the voltage of BL and BL' nodes. A scaled copy of the BL current, i'', feeds the CCO and generates signal z_0 which drives the ripple counter. The capacitors are charged by current i'' while discharged by the pull-down transistors.

C. BLVR-Based Feedback for CCO Linearity Enhancement

To address these challenges, we propose a feedback compensation technique that dynamically adjusts the BL voltage in response to variations in the total BL conductance which appear during the MVM computation in AiMC cores. This adjustment is achieved setting $EN_{LIN} = 1$, which causes $V_{BL'}$ to differ from V_R and to increase with the BL current since the scaled copy of the current flows on the resistance R_G. Formally, the voltage $V_{BL'}$ becomes dependent on g_{BL}:

$$V_{BL'} = V_R + i' R_G = V_R + \alpha V_{BL} R_G \, g_{BL}. \tag{6}$$

Incorporating this relationship into (2) yields:

$$V_{BL} = \frac{V_R}{1 - \alpha R_G \, g_{BL}}. \tag{7}$$

Substituting (7) into (5), the frequency expression becomes

$$f_{CCO} = \frac{k V_R \, g_{BL}}{2CV_M - 2\alpha C V_M R_G \, g_{BL} + 2kt_D V_R \, g_{BL}}. \tag{8}$$

To achieve linearity, the second and third terms in the denominator must be equalized. This condition determines the optimal value of the resistance R_G as

$$R_G = \frac{k V_R t_D}{\alpha V_M C}. \tag{9}$$

With this choice of R_G, the CCO output frequency becomes linear with the conductance g_{BL}:

$$f_{CCO} = \frac{k V_R}{2CV_M} \, g_{BL}, \tag{10}$$

where the proportionality factor,

$$\beta_{LIN} = \frac{k V_R}{2CV_M}, \tag{11}$$

is composed of design parameters and can be tuned to meet the specific frequency-to-conductance ratio required.

It should be noted that, reasonably assuming, $k/\alpha = 2$, $V_M = V_{DD}/2$, $V_R = V_{DD}/10$, $t_D = 10\,ps$ and $C = 10\,fF$, the resistor value is $R_G = 400\,\Omega$ (from (9)), which can be implemented with minimal area overhead using polysilicon. Nonetheless, from a practical perspective, implementing the linearization resistor requires consideration of process variations, as resistance deviations affect the frequency accuracy.

A drawback of the linearization scheme is the increased power consumption due to the higher BL voltage. The power overhead is estimated by considering the BL voltage increase, defined as the ratio between (7) and (3), yielding a factor $1/(1 - \alpha R_G \, g_{BL})$, which is evaluated at mean g_{BL} value.

IV. Design Methodology

The value of the linearization resistance R_G must be determined according to the design specifications of the complete AiMC core. Referring to the general architecture shown in Fig. 1 and described in Sec. II, the absolute value of the elements of the input (x_i) and output (z_j) vectors are represented with N and M bits, respectively. Assuming the inputs are pulse-width modulated at a frequency f_{PWM}, the total conversion time of the ADC is:

$$T_{conv} = \frac{2^N}{f_{PWM}}. \tag{12}$$

The ripple counter requires 2^{M-1} cycles of the output least significant bit (z_0) to fully digitize the total BL charge into an M-bit output. Consequently, the maximum oscillation frequency of the CCO is:

$$f_{CCO}^{MAX} = \frac{2^{M-1}}{T_{conv}} = 2^{M-1-N} f_{PWM}, \tag{13}$$

which defines a design-specific relationship linking the input and output frequencies as a function of the input and output resolutions. Substituting (13) into (10) and evaluating it for the maximum BL conductance, $g_{BL} = n \, g^{MAX}$, allows for the appropriate selection of integration capacitors, C, once the reference voltage, V_R, and current mirroring ratios, k and α, are fixed. At this stage, the value of linearization resistor R_G can be initially estimated using (9) and then fine-tuned via transient parametric simulations until the maximum

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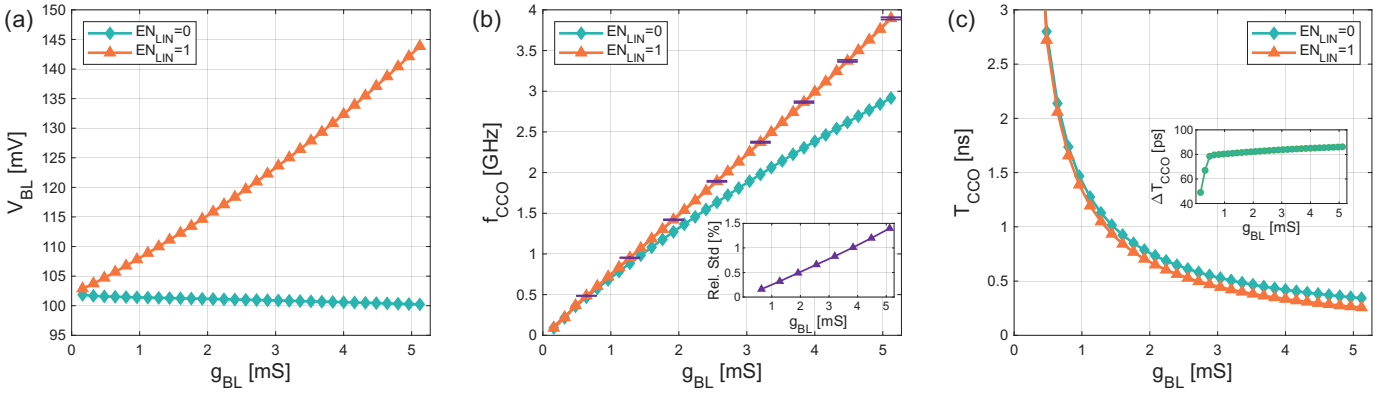

Fig. 3. Results of parametric transient pre-layout simulations with g_{BL} swept across its full range, comparing the cases without (diamond-marked) and with (triangle-marked) the linearization resistance enabled. (a) Mean BL voltage. (b) CCO output frequency with purple error bars indicating its relative standard deviation due to process variations in R_G, also reported in the inset. (c) Oscillation periods; inset: period difference, ΔT_{CCO}, between the two simulations.

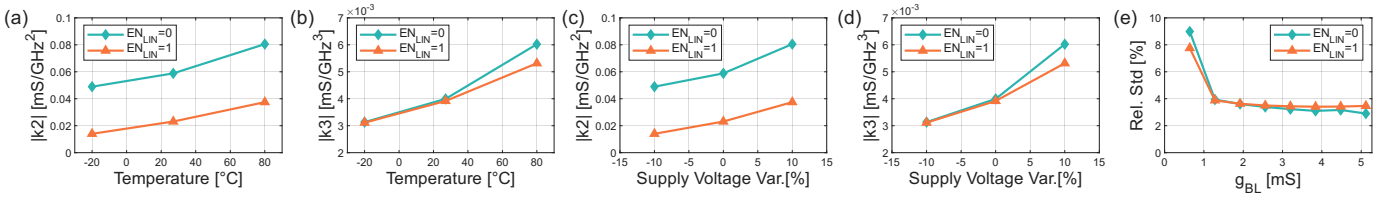

Fig. 4. Third-order polynomial fitting coefficients of the f_{CCO}–g_{BL} characteristic: (a), (b) quadratic ($|k_2|$) and cubic ($|k_3|$) coefficients vs. temperature variations; (c), (d) quadratic and cubic coefficients vs. supply variations. (e) Relative standard deviation of f_{CCO} vs. g_{BL} due to process and mismatch.

oscillation frequency aligns with the target frequency from (13). For an actual implementation, post-layout simulations can be employed for the final adjustment of the resistor value.

V. Simulation Results

The proposed circuit, depicted in Fig. 2, was designed using the 28 nm FD-SOI technology node from STMicroelectronics. The design complies with the specifications of the AiMC core described in [8]. The memory array size is assumed to be $n = m = 512$ cells, each with conductance ranging from 0 to $g^{MAX} = 10\,\mu S$, the reference voltage V_R is set to 0.1 V. The supply voltages V_{HDD} and V_{LDD} are 1.8 V and 0.9 V, respectively. The mirroring factors α and k are selected as $\frac{1}{16}$ and $\frac{1}{8}$, respectively, to optimize power consumption and minimize circuit area. The number of bits representing the absolute values of each input and output are $N = 7$ and $M = 10$, respectively. Following the methodology outlined in the Section IV and assuming a PWM frequency $f_{PWM} = 1$GHz, the maximum CCO frequency is calculated as $f_{CCO}^{MAX} = 4$ GHz. These specifications guide the capacitor selection to $C = 17.8$ fF, comprising parasitic contribution of the node (L and R, see Fig. 2), and yield a target proportionality factor $\beta_{LIN} = 0.78$ GHz/mS, as defined by (11).

The circuit was initially simulated with the linearization resistance path disabled ($EN_{LIN} = 0$) using parametric transient simulation. Each point of the diamond-marked curve in Fig. 3 (a) reports the mean BL voltage evaluated during different transient pre-layout simulations, where g_{BL} is swept across its full range. The results demonstrate the circuit's ability to maintain an approximately constant BL voltage, $V_{BL} = V_R$, as defined in (3), with only minor voltage error attributable to channel-length modulation inherent to this topology when operating over a wide current range. The corresponding f_{CCO} (Fig. 3(b), diamond marks) exhibits nonlinearity, consistent with the behavior described in (5).

The simulation was repeated with the linearization resistance path enabled ($EN_{LIN} = 1$) and with $R_G = 980\ \Omega$, determined using the method described in Section IV and implemented, targeting minimal area, with a polysilicon resistor occupying an area of $1.3\mu m^2$. The triangular-marked curves in Fig. 3 (a) and (b) show the mean BL voltage and CCO oscillation frequency, respectively. The feedback resistance effectively adjusts BL voltage in response to changes in the total BL conductance, in agreement with the relationship defined in (7). To evaluate the impact of process variation on R_G and their effect on f_{CCO}, Monte Carlo simulations were conducted at eight different g_{BL} values. The purple error bars in Fig. 3 (b) represent the standard deviation of the results, demonstrating a small impact from the resistor variability with a relative standard deviation below 1.4%, as showed in the inset plot in Fig. 3 (b). Fig. 3 (c) shows the corresponding oscillation periods. The difference between the periods of the two simulations (ΔT_{CCO}) is shown in the inset graph, revealing an almost constant offset, which correspond to $2t_D$ defined by (4).

The same simulations were repeated while sweeping temperature from -20°C to $+80$°C and varying both V_{LDD} and V_{HDD} by $\pm 10\%$. The resulting f_{CCO}–g_{BL} characteristics were used to extract the third-order polynomial fitting coefficients shown in Fig. 4 (a)–(d). At nominal supply voltage and RT, the proposed linearization technique (Fig. 4 (a) and (c)) reduces the quadratic coefficient $|k_2|$ from 5.88×10^{-2} to

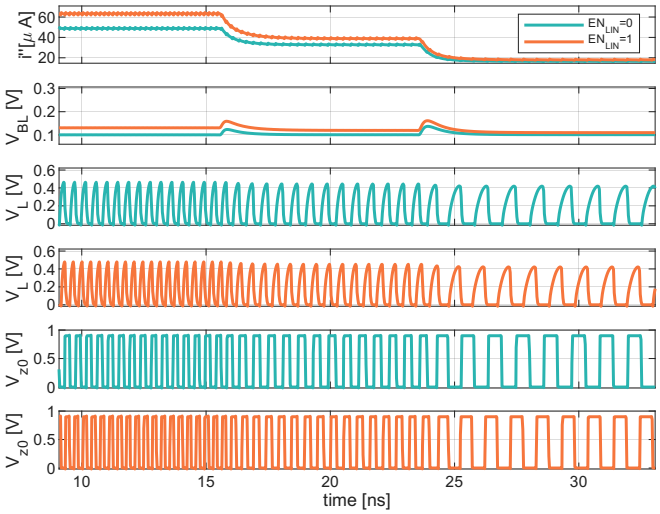

Fig. 5. Transient simulation with three step changes in g_{BL}. From top to bottom (see Fig. 2): CCO input current i'', voltages V_{BL},V_L and V_{z0}.

2.31×10^{-2}, corresponding to a $2.5\times$ improvement in linearity. The cubic coefficient $|k_3|$ remains essentially unchanged, as illustrated in Fig. 4 (b) and (d), indicating that the proposed technique primarily suppresses the dominant quadratic distortion. The sensitivity of the extracted coefficients to temperature and supply variations is comparable in the two cases.

Additionally, Monte Carlo simulations performed at eight g_{BL} values confirm that the proposed linearization technique does not significantly increase frequency variability, as indicated by the relative standard deviation reported in Fig. 4 (e).

To emulate input variations during MVM computation, as shown in Fig. 1, a transient simulation was performed with three distinct step variations in g_{BL}. Results are reported in Fig. 5, where the scaled BL current (i''), corresponding to the CCO input current, exhibits the typical monotonically decreasing behavior. In the linearized case, this current spans a wider range due to the variation of V_{BL} since the linearization technique increases the BL current by raising the BL voltage compared to the non-linearized case, resulting in a reduced oscillation period of the LSB output (z_0).

Finally, considering the value of R_G, the power overhead, estimated as described in Section III-C, is 18.6%, assuming $g_{BL} = 2.56$ mS, in the middle of the conductance range. This estimate is conservative, as in the AiMC application context, i.e. neural networks, the weight and input distributions that determine the time-averaged conductance typically result in a lower effective g_{BL} than the value assumed here.

VI. Conclusions

This paper presents a design technique to linearize the frequency characteristic of a CCO within a CCO-based ADC for MVM in AiMC accelerators. Simulations conducted in a 28 nm FD-SOI CMOS technology demonstrate that the modified BLVR reduces the delay-induced nonlinearities. The technique retains the key benefits of CCO-based ADCs requiring only the addition of a resistor within the BLVR circuitry and offers a scalable and efficient solution to improve CCO-based ADC linearity in AiMC systems.

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