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Efficiency-Oriented DPS Implementation in Morphed Three-Phase Three-Level DAB for Light-Load EV Charging

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ABSTRACT This work presents an efficiency-oriented modulation and morphing strategy for a three-phase three-level dual active bridge converter operating across both 800 V and 400 V electric vehicle battery systems. By reconfiguring the converter into a single-phase dual active bridge or a hybrid half-bridge/full-bridge structure at light-load, the proposed approach reduces current-invariant losses. A unified dual phase-shift framework is formulated to analytically model power flow and peak-current minimization across all three-level modulation variants, inner phase shift, duty-cycle control, and T-type zero-level modulation, demonstrating that all combinations produce equivalent voltage and current waveforms. Simulation efficiency maps are generated for all valid primary/secondary modulation pairs and indicate that inner and duty-cycle modulation achieve the highest efficiency across the full operating window. Hardware-in-the-loop experiments confirm stable three-phase-to-single-phase morphing and accurate power tracking between reference and measured power profiles for both voltage levels. The results validate that the proposed morphing strategy enables wide-range, auxiliary-free light-load operation suitable for next-generation EV charging architectures.

INDEX TERMS Dual active bridge, Dual-phase-shift, EV charging, morphing, light-load efficiency, wide output voltage range.

I. INTRODUCTION

High-power dc fast charging for battery electric vehicles is increasingly moving toward hundreds of kilowatts of charging power and wide battery voltage ranges [1]. Recent standards and demonstrators show dc charging modules delivering 150-350 kW or more, while the dc link on the vehicle side can span roughly 200-1000 V, with the mainstream clustering around 400 V and 800 V battery systems [2]–[4]. This trend is driven by the need to shorten charging time without exceeding cable and battery current limits, and it directly translates into demanding requirements for the isolated dc-dc stage of the charger in terms of power density, efficiency, and controllability [5], [6].

Among isolated dc-dc topologies, the dual active bridge (DAB) has emerged as a strong candidate for such applications thanks to its galvanic isolation, step-up/-down operations, zero voltage switching (ZVS), and bidirectional power flow capability [7]. The single-phase DAB reached great popularity because of its great modulation flexibility. In fact, besides the conventional single-phase-shift (SPS), several other techniques like extended-, dual-, and triple-phase-shift took advantage of inner phase shifts to achieve optimizations

in terms of light-load operations, soft-switching, and peak current minimization [8], [9]. However, the single-phase structure limits the straightforward use of commercial three-phase power modules, constraining both power density and cost competitiveness at the very high power levels targeted by next-generation fast chargers [10].

To address this, three-phase two-level DAB converters have been proposed [7]. In their simplest implementation, they operate under a six-step SPS modulation, offering high power capability and leveraging mature three-phase module technology. Yet, in symmetric operation they lack many of the advanced modulation features available in the single-phase case, which restricts control flexibility, especially under light-load and wide-voltage conditions [11]. This limitation has motivated the adoption of three-level power modules (e.g., neutral-point-clamped or T-type), leading to the three-phase three-level DAB, which combines the benefits of multilevel operation with the high-power capability of a three-phase structure [12]–[15].

In the context of EV charging, however, even a three-phase three-level DAB suffers from low efficiency at light-load and experience soft-switching degradation across a wide output voltage range, unless additional hardware, such as interphase inductors, auxiliary switches, or modular converter stages, is introduced [16], [17]. These solutions increase cost and architectural complexity and are not always attractive for industrial deployment.

To address this challenge, this paper proposes a morphing technique that reconfigures the three-phase three-level DAB into different effective topologies depending on the operating point, while keeping the physical hardware unchanged. In high-power regions, all three phases remain active and the converter exploits the full three-phase three-level structure; at light-load, one or more phases are intentionally shed, and the converter transitions into a single-phase DAB, which ensures a wide output voltage range, and enhanced light-load efficiency.

Once the converter is morphed into a single-phase equivalent, it becomes possible to apply modulation strategies commonly used in single-phase DABs, including SPS as well as extended-, dual-, and triple-phase-shift variants. In particular, prior work in [18] focused on SPS operation, addressing soft-switching boundaries and light-load efficiency in the morphed configuration. This paper represents a direct extension of that concept by investigating dual-phase-shift (DPS) control applied to the morphed topology and evaluating how the additional degree of freedom can be exploited for current shaping and loss reduction.

The conventional DPS implementation introduces an inner phase shift between the legs of each bridge to synthesize a three-level voltage waveform [19]. However, the same waveform can also be generated through duty-cycle modulation, which directly regulates the conduction intervals, or by activating the T-type horizontal devices to synthesize explicit zero-voltage levels [20]. These alternative mechanisms allow several primary/secondary combinations, inner-inner, duty-duty, inner-duty, duty-inner, and T-type-based variants, each offering the same average power capability but exhibiting different conduction paths, switching

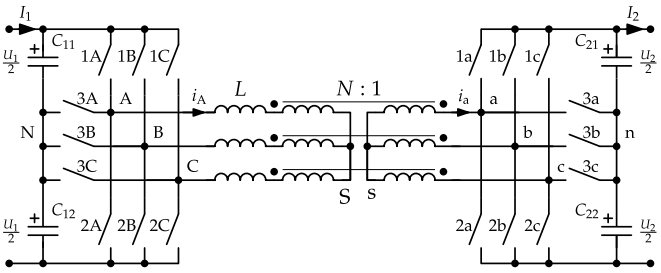


FIGURE 1: Three-phase three-level (T-type) DAB with star-connected transformers, whose parameters are listed in Table 1.

events, and therefore distinct loss characteristics. This work systematically analyzes these options in the context of morphing-based operation and evaluates their impact on efficiency across the full 400 V/800 V operating regions. The feasible three-level modulation combinations are comparatively evaluated through device-level simulations to identify the most efficient primary-secondary pairs, and the approach is validated experimentally through hardware-in-the-loop testing, confirming stable morphing, clean current transition, and a good power-tracking accuracy.

The remainder of the paper is organized as follows. Section II reviews the proposed light-load morphing schemes for the 800 V-800 V and 800 V-400 V operating conditions and derives the associated maximum power limits. Section III introduces the analytical models for six-step three-phase operation and DPS-based single-phase operation, including the peak-current optimization. Section IV presents the simulation setup and efficiency maps for all modulation combinations. Section V reports the hardware-in-the-loop verification of the morphing and control strategy under realistic charging profiles. Finally, Section VI summarizes the main findings and outlines possible extensions of this work.

II. PROPOSED LIGHT-LOAD MORPHING TECHNIQUE

In virtue of the great number of switches that characterize the three-phase three-level DAB, the operation in light-load conditions leads to low-efficiency values [21]. To address this issue, the current manuscript leverages the multiple degrees of freedom given by the three-phase three-level topology in Fig. 1. To set a scenario popular in EV charging applications, it is assumed from now on that the primary DC-link voltage U_1 is fixed at 800 V while the secondary voltage U_2 depends on the voltage level of the EV battery, which is 400 V or 800 V. The main circuit parameters are summarized in Table 1.

A. LIGHT-LOAD OPERATIONS AT 800 V-800 V

In this operative condition, one of the DAB phases is alternatively turned off; i.e., implementing the so-called rotation phase shedding [22]. An example of phase C-c being turned off can be seen in Fig. 2(a). This adaptation allows for a rough reduction by 1/3 of the current invariant losses share, improving the light-load efficiency [23].

Such working conditions are equivalent to a single-phase three-level DAB having double transfer-inductance ($2L$); see Fig. 2(a). The theoretical maximum power processed in this

TABLE 1: Three-phase three-level DAB main parameters from [10].

Parameter	Symbol	Value
Transformer turns ratio	$N:1$	1:1
Transfer-inductance	L	0.117 mH
DC-link capacitance	C_{xy}	600 μF
Primary voltage	U_1	800 V
Secondary voltage	U_2	200–900 V
Switching frequency	f_{sw}	2 kHz
Maximum outer phase shift	d_{max}	0.25
Three-phase DAB rated power†	P	265 kW at $U_2 = 800$ V 133 kW at $U_2 = 400$ V
Vertical MOSFETs	1x, 2x	CAS300M17BM2
Horizontal IGBTs	3x	SKM300GM12T4

†*Considering SPS according to [7].*

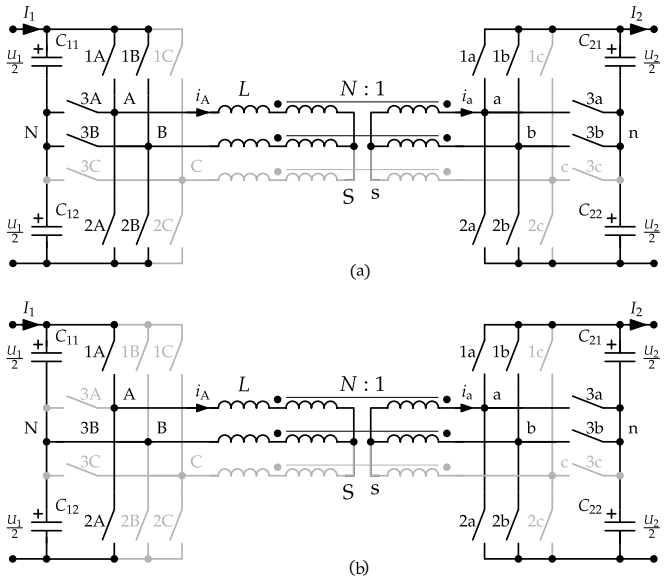


FIGURE 2: Equivalent circuit of the three-phase DAB in Fig. 1 under light-load. (a) Phase C-c shedding, suitable for 800 V-800 V operation. (b) Phase B-C-c shedding and switch 3B turned on, suitable for 800 V-400 V operation.

condition is:

$$P_{\max} = \frac{U_1 U_2 N}{16 f_{sw} L}\ , \tag{1}$$

which corresponds to about 171 kW with the parameters of Table 1 and assuming $U_2 = 800$ V. If compared with the theoretical maximum power of the three-phase three-level DAB, it corresponds to a reduction of about 35 % [7]. Actual maximum power values are usually sharply smaller because of accounting for the real components' ampacity.

In this working condition, it is still possible to leverage the classical five degrees of freedom of the three-level DAB. Namely, outer phase shift, inner phase shifts, and primary and secondary pole voltages zero-level durations [24]. This allows for primary and secondary voltages v_{AB} and v_{ab} to be characterized with up to five levels ranging the $\pm U_1$ and $\pm U_2$ diapasons respectively. If operated in SPS modulation, the ZVS is almost always ensured by virtue of the voltage gain ratio $G = U_1/NU_2 \approx 1$ [7].

Beyond SPS, the three-level DAB can also be operated with DPS modulation. The most conventional implementation of the DPS is introducing an inner phase shift between the legs of each bridge, allowing both v_{AB} and v_{ab} to assume three effective voltage levels during the switching period [19]. The same three-level behaviour can also be obtained by duty-cycle modulation, where the power is regulated by directly controlling the duty of the switches, which implicitly sets the duration of the zero-voltage interval, or by turning on the horizontal IGBTs of the T-type structure to synthesize zero-level segments [20]. As a result, several valid combinations exist for shaping the primary and secondary pole voltages: inner phase shift on both bridges, inner on one bridge and duty on the other, duty-cycle on both bridges, or cases where one of the bridges or both the bridges employs the T-type zero-level generation. Therefore, in total, nine combinations can be implemented, and each combination provides a distinct trade-off between current shaping, switching losses, and control complexity. The study of SPS modulation has already been investigated in [18]. Thus, this paper investigates all DPS modulation combinations to assess their impact on light-load operation and to identify the most suitable strategy for the considered application.

B. LIGHT-LOAD OPERATIONS AT 800 V-400 V

Similarly to what was discussed in Section II-A, one of the DAB phases is alternatively turned off. Additionally, to ensure ZVS conditions, one of the primary active legs can be clamped to the split-capacitor middle point. With reference to Fig. 2(b), switch 3B can be permanently turned on while switches 1B and 2B are turned off. This operation allows for a reduction by 42 % of the current invariant losses and by 50 % of the number of switching events, with respect to three-phase three-level operations, greatly improving light-load efficiency [23].

Such a working condition is equivalent to a single-phase three-level hybrid configuration constituted by one half-bridge at the input and one full-bridge at the output having double transfer-inductance ($2L$) [25], [26]; see Fig. 2(b). The theoretical maximum power processed in this condition is:

$$P_{\max} = \frac{U_1 U_2 N}{32 f_{sw} L}\ , \tag{2}$$

which corresponds to about 42 kW with the parameters of Table 1 and assuming $U_2 = 400$ V. If compared with the theoretical maximum power of the three-phase three-level DAB, it corresponds to a reduction of about 68 % [7]. Clearly, such a technique should be employed at a very light-load.

If compared with Section II-A, the primary side loses one degree of freedom (i.e., inner phase shift) and the related primary voltage $v_{AB} = v_{AN}$ to assume up to three levels ranging the diapason $\pm U_1/2$. Clearly, the secondary side remains unchanged to maintain the voltage gain ratio $G = U_1/2NU_2 \approx 1$, which ensures ZVS while operating in SPS modulation [27].

Although the primary bridge behaves as a half-bridge in this condition and therefore loses the inner phase shift degree

of freedom, the implementation of DPS modulation remains possible. In particular, duty-cycle modulation can be applied to the primary bridge, whereas, the secondary full-bridge still offers the capability to generate three voltage levels through different mechanisms, inner phase shift between the legs, duty-cycle modulation that adjusts the duty of the switches, or activation of the horizontal devices of the T-type structure to synthesize the zero-level interval. As a result, three valid modulation options exist for this hybrid single-phase operating mode, each providing a different trade-off between current shaping, switching effort, and achievable conversion efficiency. Thus, even in this case, apart from the SPS modulation which has already been discussed in [18], all of the three-level modulation combinations are investigated to assess their impact on light-load operation and to identify the most suitable strategy for the considered application.

III. ANALYTICAL MODELLING

A. THREE-PHASE DAB OPERATION UNDER SIX-STEP MODULATION

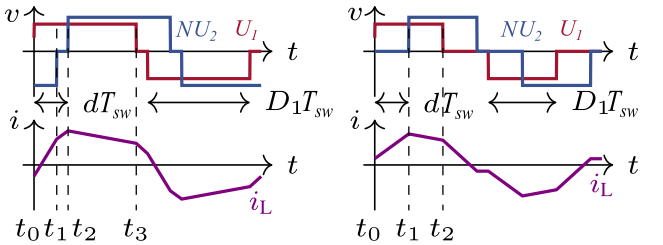
In the three-phase three-level DAB, the power transfer mechanism can be interpreted through the classical six-step operation originally introduced for the three-phase DAB topology [7]. In this mode, each bridge synthesizes a three-phase line-to-neutral voltage set where each phase remains clamped to either $+U_1$, 0, or $-U_1$ for $1/6$ intervals, producing the familiar six-segment waveform over half of the switching period. The primary and secondary bridges operate with the same six-step structure but are phase-shifted by the controllable value d, so the effective voltage applied to the transformer leakage inductance L is the difference between the two six-step waveforms. Because the transformer is Y-Y connected and the phase currents satisfy $i_A + i_B + i_C = 0$, the system dynamics reduce to a single equivalent leakage inductance per phase, and the inductor current can be solved piecewise over the six conduction intervals. Thus, the resulting average transferred power can be calculated as:

$$P = \frac{NU_1U_2}{Lf_{sw}} \begin{cases} d\left(\frac{2}{3} - d\right) & 0 \le d \le 1/6 \\ \left(d - 2d^2 - \frac{1}{36}\right) & 1/6 \le d \le 1/3 \end{cases}. \quad (3)$$

This power equation describe the fundamental behaviour of the three-phase six-step DAB and provide the analytical reference for the operating region from which the converter later morphs into the single-phase mode.

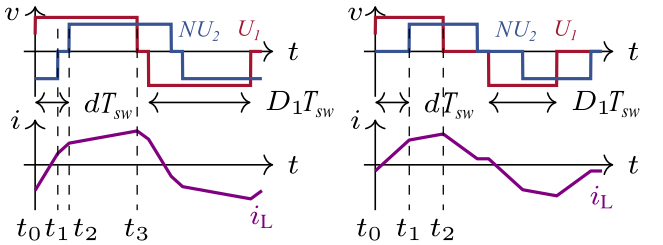
B. SINGLE-PHASE DAB OPERATION UNDER DPS MODULATION

In contrast to SPS, which relies solely on the outer phase-shift d, DPS introduces an additional inner phase shift ratio, denoted as D_1, between the two legs of both the primary and secondary bridges. This additional degree of freedom generates a three-level voltage waveform for both U_1 and U_2, and can be exploited to minimize the peak current. The combined use of d and D_1 provides substantial control flexibility and enables improved current shaping [28].



(a) DPS: $0.5-d \le D_1$ (b) DPS: $d \le D_1 < 0.5-d$

FIGURE 3: Operational waveforms under DPS when $G \le 1$ for (a) Mode 1 and (b) Mode 2.



(a) DPS: $0.5-d \le D_1$ (b) DPS: $d \le D_1 < 0.5-d$

FIGURE 4: Operational waveforms under DPS when $G > 1$ for (a) Mode 1 and (b) Mode 2.

Under DPS, two operating modes arise depending on the relative values of d and D_1. Mode 1 corresponds to the range $0.5-d \le D_1$, while Mode 2 applies when $d \le D_1 < 0.5-d$. The corresponding voltage and current waveforms for these two modes are illustrated in Fig. 3(a)–(b) and Fig. 4(a)–(b). The transferred power under DPS can be expressed in closed form for each mode as:

$$P = \frac{NU_1U_2}{Lf_{sw}} \begin{cases} d(1-2d) - (0.5-D_1)^2 & \text{Mode 1} \\ d(2D_1 - d) & \text{Mode 2} \end{cases}. \quad (4)$$

In DPS modulation, the transferred power depends on both d and D_1, as given in (4). The role of D_1 is to provide an additional degree of freedom, enabling current shaping and peak-current reduction for a given power reference by selecting an appropriate (d, D_1) pair.

It is worth noting that under inner phase shift control, the duty of all MOSFETs remains fixed at 50 %, and only the relative phase shift between the two legs is modulated through D_1. Whereas, in duty-cycle modulation, the same parameter D_1 is interpreted as the duty ratio of the MOSFETs, while the phase shift between the legs is kept fixed at half a switching period. As a result, the duty-cycle variant produces the same effective voltage and current waveforms shown in Fig. 3 and Fig. 4, despite relying on a different control mechanism.

A similar behaviour arises with the T-type modulation. Here, D_1 is applied as the duty ratio of the vertical MOSFETs, while the horizontal IGBTs are activated according to the complementary switching combinations that synthesize the zero-voltage level. This also results in a three-level pole voltage identical to that produced by the inner phase shift and duty-cycle methods, and therefore yields the same voltage

TABLE 2: Optimization results of DPS with minimum peak current.

P	G	D_1	d	Mode
$[P_{\text{lim1}}, 1]$	$G > 1$	$(G-1)d - \frac{1}{4}G + \frac{3}{4}$	$[d_{\text{lim1}}, 0.25]$	1
$[0, P_{\text{lim1}}]$	$G > 1$	$\frac{G+1}{G-1}d$	$[0, d_{\text{lim1}}]$	2
$[P_{\text{lim2}}, 1]$	$G \leq 1$	$\frac{3G-1}{4G} + \frac{1-G}{G}d$	$[d_{\text{lim2}}, 0.25]$	1
$[0, P_{\text{lim2}}]$	$G \leq 1$	$\frac{1+G}{1-G}d$	$[0, d_{\text{lim2}}]$	2

and current waveforms illustrated in Fig. 3 and Fig. 4. Since all three modulation strategies ultimately generate the same power-transfer behaviour, where (4) is always valid, they can be freely combined on the primary and secondary sides in multiple configurations, as outlined in Section II.

Furthermore, the DPS modulation offers a large set of feasible (d, D_1) combinations for a given reference power. To identify the most favourable operating point within this set, an optimization criterion is required. In this work, the minimum-peak-current condition is selected, as reducing the current extrema directly lowers conduction losses and improves light-load efficiency. The optimal pair (d, D_1) can be obtained by applying a Lagrange multiplier to the power expression in (4), enforcing the power constraint while minimizing the current peak. This procedure yields the analytical relationship between d and D_1 that defines the optimal operating trajectory for DPS modulation. The Lagrangian function in this paper is given by the following:

$$\mathcal{L}(d, D_1, \lambda) = T(d, D_1) + \lambda[P(d, D_1) - P^*] \,, \tag{5}$$

where $T(d, D_1)$ is the target function, which represents the formula for peak current. $P(d, D_1)$ refers to the transmission power, and the constraint condition is given by $P(d, D_1) = P^*$. The λ is the Lagrange multiplier.

For DPS, the peak current behavior in mode 1 and mode 2 is influenced by the relationship between U_1 and NU_2. As illustrated in Fig. 3(a) and Fig. 4(a), the peak currents occurs at t_2 when $G \leq 1$, and at t_3 when $G > 1$. Similarly, in mode 2, the peak current appears at t_1 and t_2 under the two respective voltage conditions, as shown in Fig. 3(b) and Fig. 4(b). Thus the corresponding expressions for both modes can be summarized as:

$$I_{\text{LP}} = I_{\text{max}} \begin{cases} 8d + D_1(4G-4) & G > 1 \\ 8Gd + D_1(4-4G) & G \leq 1 \end{cases} , \tag{6}$$

where I_{max} is $NU_2/16Lf_{sw}$ in 800 V-800 V case and $NU_2/32Lf_{sw}$ in 800 V-400 V case.

Having these current expressions and using the Lagrangian condition in (5), the optimal solutions for DPS with minimum peak current can be calculated as a function of P_{lim1}, P_{lim2}, d_{lim1}, and d_{lim2} and are summarized in Table 2. Here, P_{lim1}, P_{lim2} are normalized with respect to P_{max}, and their analytical expressions, together with the corresponding limits d_{lim1}, and d_{lim2}, are defined as:

$$\begin{cases} P_{\text{lim1}} = \dfrac{G^2 + 2G - 3}{2G^2} \\ P_{\text{lim2}} = -\dfrac{3}{2}G^2 + G + \dfrac{1}{2} \end{cases} , \tag{7}$$

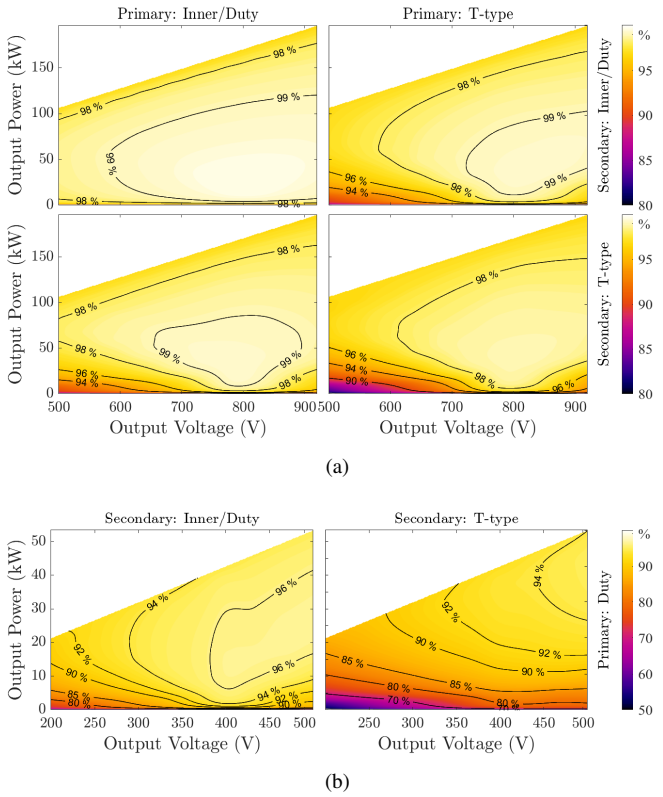
$$\begin{cases} d_{\text{lim1}} = \dfrac{G-1}{4G} \\ d_{\text{lim2}} = \dfrac{1-G}{4} \end{cases} . \tag{8}$$

IV. NUMERICAL VALIDATION

In the study, the analytical DPS power expression was used to compute the operating points by deriving the corresponding values of d and D_1 for each reference power and voltage pair. Once these modulation parameters were obtained, the converter was simulated in PLECS using the detailed thermal models of the semiconductor devices CAS300M17BM2 and SKM300GM12T4, which are listed in Table 1 and the parameters are taken from the datasheets. These models account for the switching and conduction losses of the MOSFETs and IGBTs, calculated at a fixed junction temperature at 100 $^\circ C$, enabling a realistic estimation of the converter efficiency. Since all modulation combinations generate equivalent voltage and current waveforms and the same transformer is used in every case, the corresponding transformer losses are not included in the comparison. For the same reason, auxiliary losses are also neglected, as their inclusion would uniformly shift the absolute efficiency values without affecting the relative efficiency trends among the modulation strategies.

The operating power was swept from zero up to the maximum value P_{max} defined in Section II, while the input voltage U_1 was fixed at 800 V and the output voltage was varied between 500 V-920 V for the 800 V-800 V case and 200 V-500 V for the 800 V-400 V case. This results in a voltage-gain range of approximately 0.86 to 1.6 in the 800 V battery case and 0.8 to 2 in the 400 V battery case, thereby covering both $G \leq 1$ and $G > 1$ operating conditions. These voltage intervals also align with practical EV-charging requirements reported in the CharIN specifications [29]. For each operating point, the efficiency was extracted from the simulated waveforms, enabling a direct comparison among the different modulation combinations. In addition to the semiconductor conduction and switching losses, a fixed gate-driver loss of 5 W per device was included to account for the auxiliary power consumption of the converter.

Figure 5(a) summarizes the simulated efficiency for all nine possible modulation combinations in the 800 V-800 V case. The top-left plot shows the four combinations obtained when both the primary and secondary bridges use inner phase shift or duty-cycle modulation; the top-right and bottom-left plots correspond to the two mixed cases where one bridge uses inner/duty modulation and the other uses T-type modulation; finally, the bottom-right plot represents the case where both bridges use T-type modulation. As expected, inner phase



(a)

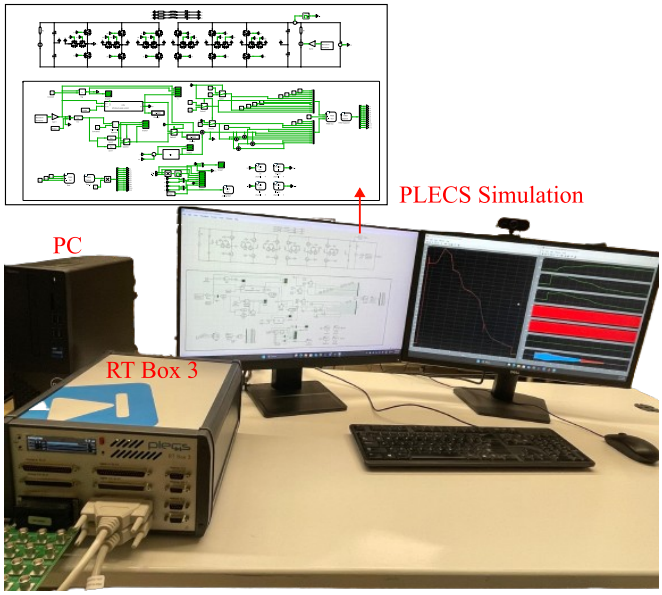
(b)

FIGURE 5: (a) Efficiency maps for the 800 V-800 V case under all nine primary/secondary modulation combinations. (b) Efficiency maps for the 800 V-400 V case under all three primary/secondary modulation combinations.

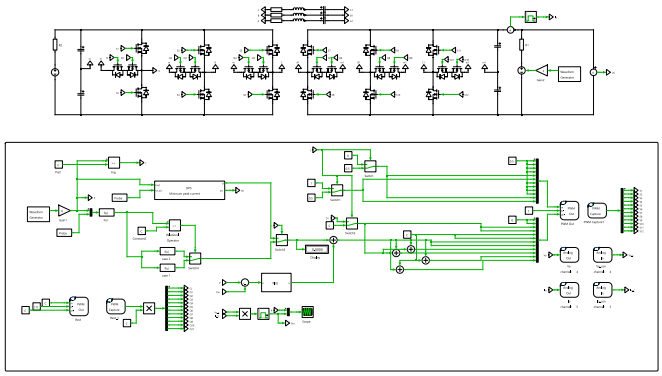
shift and duty-cycle modulation yield identical efficiency curves, since both strategies generate the same three-level voltage waveform and involve the same number of switching transitions. In contrast, T-type modulation consistently results in a slightly lower efficiency, primarily due to the larger number of semiconductor devices involved in generating each switching state, which increases both conduction and switching losses. This trend is evident in all operating regions and across both voltage-gain conditions.

For the 800 V-400 V case, shown in Fig. 5(b), the primary side operates as a dual active half bridge and therefore cannot apply inner phase shift modulation; only duty-cycle modulation is feasible on the primary side. On the secondary side, inner phase shift, duty-cycle modulation, and T-type modulation were implemented. Even in this case, the T-type modulation consistently exhibits slightly lower efficiency due to the increased number of semiconductor devices involved, which raises both conduction and switching losses.

Across all operating points, the simulations showed that inner phase shift and duty-cycle modulation achieve nearly identical efficiency, since both produce the same three-level voltage waveform and involve the same number of active devices. Consequently, although four inner/duty combinations were examined in simulation, their efficiency overlapped completely. The efficiency contour lines in Fig. 5 enable a



(a)



(b)

FIGURE 6: (a) Real-time HIL experimental setup. (b) Plecs schematic of real-time HIL test depicting converter and morphing technique controller.

direct comparison among the modulation strategies over the entire operating range and show that inner phase-shift and duty-cycle modulation consistently yield the highest efficiency across most operating points, which therefore represent the recommended operating regions for practical implementation.

For the HIL validation, it was therefore sufficient to implement only the representative cases: inner-inner and duty-duty for the 800 V case, and duty-inner and duty-duty for the 400 V case, respectively on the primary-secondary sides. The T-type combinations were not considered further, as their efficiency remained consistently lower throughout the simulation study.

V. HARDWARE-IN-THE-LOOP VERIFICATION

To verify that the proposed morphing strategies can be executed reliably by a real controller rather than only in offline simulation, hardware-in-the-loop (HIL) tests were carried out. The simulation study already indicated that the inner phase shift control and

duty-cycle modulation on both the primary and secondary sides deliver the highest efficiency among the examined combinations. Therefore, both approaches were included in the HIL campaign. The results presented in this section, focus on the transition from full three-phase operation to the morphed single-phase mode under DPS modulation, evaluating both the inner phase shift and duty-cycle implementations.

Fig. 6(a) shows the real-time HIL experimental setup and Fig. 6(b) depicts the Plecs schematic of HIL setup. The tests were executed on an RT Box 3 platform from Plexim GmbH. The converter architecture of Fig. 1 was implemented using FlexArray blocks from the PLECS library. Due to hardware limitations, the PWM signals were generated at a switching frequency of 2 kHz, whereas the DAB converter dynamics were emulated with a sampling frequency of 200 kHz. Increasing the number of samples per switching period enables accurate reconstruction of the inductor current waveforms and corresponding power transfer.

To reproduce a realistic charging scenario, the power and voltage profile of a Fiat 500e battery during a full charging cycle, derived from the datasets in [8], [30], was used as the reference signals for the DAB converter. The original power profile reaches approximately 80 kW, and the voltage ranges between $390\,\mathrm{V}$ and $450\,\mathrm{V}$. To match the rated power and operating limits of the converter parameters listed in Table 1, the profile was uniformly scaled for both the $800\,\mathrm{V}$-$800\,\mathrm{V}$ and $800\,\mathrm{V}$-$400\,\mathrm{V}$ validation cases. This ensures that the HIL controller is exercised across the full usable power range of the proposed morphing strategies. In addition, the time axis of the profile was accelerated so that the full charging cycle is reproduced in approximately 20 seconds, allowing the HIL platform to evaluate the entire operating range within a short test duration.

During HIL execution, for each sampling step, the controller computes the nominal phase-shift values directly from the analytical steady-state power equations of Section III: in three-phase operation, only the outer phase shift d is calculated, whereas in the morphed single-phase DPS mode, both the outer and inner phase shifts d and D_1 are obtained from the corresponding DPS expression. Since these equations neglect losses, dead time, and quantisation effects, the purely feedforward solution cannot perfectly track the reference profile. To compensate for the resulting mismatch, the measured power is compared with the reference power, and the error is processed by a discrete PI regulator. The PI output Δd is then added to the analytically computed feedforward value of the outer phase shift d, while D_1 is kept as given by the DPS formula. In this way, the analytical model provides the main phase-shift command, and the PI loop only performs fine correction, ensuring accurate tracking of the power profile in both three-phase and morphed single-phase operation. Furthermore, the morphing operation does not alter the form of the fundamental power-transfer relationship of the converter, which remains governed by phase-shift–based energy transfer between the primary and secondary bridges. Instead, morphing results in an equivalent topology with modified effective parameters, such as the transfer inductance and the maximum transferable power. As a consequence, the same analytical power expressions remain valid, while the operating limits are adapted according to the morphed configuration. Therefore, no retuning of control parameters is required, and the same feedforward and PI control structure is preserved before and after morphing.

From an implementation perspective, the proposed strategy introduces limited additional complexity, as it relies on standard phase-shift computation and a single PI regulator, without requiring extra sensing or high-bandwidth control loops, making it suitable for real-time execution on conventional digital control platforms.

A. VALIDATION OF 800 V-800 V CASE

For the $800\,\mathrm{V}$-$800\,\mathrm{V}$ operating condition, the converter starts in full three-phase mode and morphs into the single-phase configuration when the transmitted power becomes sufficiently low. The transition is not based on time, but on the outer phase-shift value d, which directly reflects the transferable power capability of the morphed single-phase DAB topology. The morphing threshold is therefore selected to correspond to the maximum power that can be safely processed in single-phase operation. The exact value of the threshold is not critical, as long as it is selected within a safe margin below the analytical power limit, resulting in limited sensitivity and ensuring reproducible behavior across different implementations. In this experiment, the morphing threshold was set at $d = 0.15$, ensuring that the transition occurs while the converter is still operating in a safe region.

Fig. 7 presents the HIL results for inner phase shift modulation applied on both the primary and secondary sides. The output power in Fig. 7(a) closely follows the reference profile from the scaled Fiat-500e dataset across the full charging window. After reaching the morphing threshold, the controller commands the single-phase DPS mode, and the power tracking remains continuous, with only a minor undershoot highlighted in the zoomed view on the right. The inductor currents in Fig. 7(b) clearly show the three distinct operating stages: (i) balanced three-phase currents during the high-power interval, (ii) a smooth shedding of phases during the morphing interval, and (iii) stable single-phase current with doubled transfer inductance in the light-load region. The absence of irregular oscillations confirms that the morphing action is fully controlled and does not introduce dynamic stress.

A second HIL test evaluated duty-cycle modulation applied on both the primary and secondary sides under identical conditions, using the same morphing threshold of $d = 0.15$. Fig. 8(a) again demonstrates tight tracking between the reference and measured power. The inductor-current waveforms in Fig. 8(b) show the expected change in current shape after morphing, and the three-phase-to-single-phase transition is achieved without waveform distortion. These results show that inner phase shift modulation and duty-cycle modulation

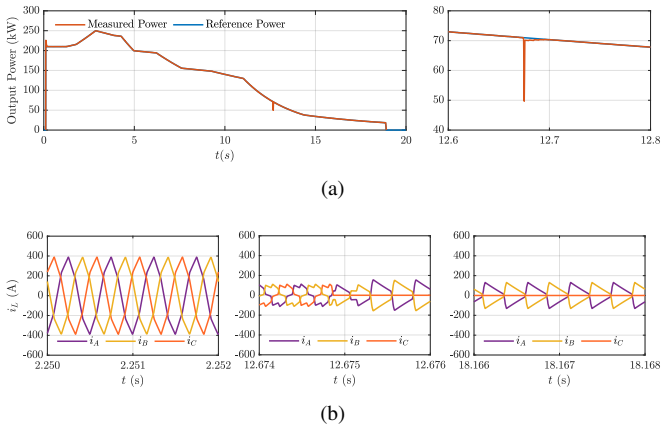


FIGURE 7: HIL results for the 800 V-800 V operating case using inner phase shift modulation on both the primary and the secondary. (a) Measured and reference output power, including a zoomed view during the morphing instant. (b) Inductor current waveforms highlighting the three operating stages: balanced three-phase operation, phase shedding during the morphing instant, and steady single-phase operation at light-load.

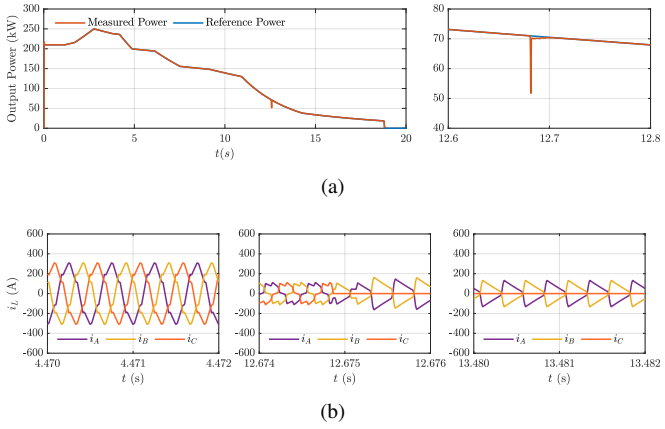


FIGURE 8: HIL results for the 800 V-800 V operating case using duty-cycle modulation on both the primary and the secondary. (a) Measured and reference output power, including a zoomed view during the morphing instant. (b) Inductor current waveforms highlighting the three operating stages: balanced three-phase operation, phase shedding during the morphing instant, and steady single-phase operation at light-load.

produce effectively identical waveforms, as discussed in Section III, confirming their compatibility with the proposed morphing strategy. They also demonstrate that using the outer phase-shift value as the transition trigger enables a stable and reliable changeover.

B. VALIDATION OF 800 V-400 V CASE

For the 800 V-400 V operating case, the converter again starts in full three-phase mode and transitions to the morphed single-phase configuration once the transmitted power becomes sufficiently low. In this scenario, the morphing threshold was set to $d = 0.2$, corresponding to the power level that can be reliably processed by the dual-active half-bridge configuration.

Fig. 9 shows the corresponding results for duty-cycle modulation applied on the primary, and the inner phase shift is applied on the secondary side. The power-tracking performance in Fig. 9(a) follows the reference profile throughout the operating range, although a noticeable overshoot appears immediately after morphing, as highlighted in the zoomed plot. This behaviour arises because the duty-cycle command reacts abruptly on the primary side, affecting the split-capacitor voltage balance. The overshoot, however, is short-lived, and the system quickly settles to the correct power level. The inductor currents in Fig. 9(b) confirm the expected three-phase operation before morphing, a transient disturbance during the topology change, and the stable single-phase waveform reached afterward. In practice, this transition disturbance can be further minimized through more advanced control strategies, if required by the application.

A second HIL test evaluated duty-cycle modulation on both the primary and the secondary sides, using the same morphing threshold of $d = 0.2$. Fig. 10(a) demonstrates the good tracking between the reference and measured power. The inductor currents in Fig. 10(b) confirm the expected three-phase-to-single-phase transition. As dicussed in Section III, the voltage and current waveforms resulting from duty-cycle control and inner phase shift control are theoretically equivalent when operated in single-phase mode. The experimental traces in Fig. 9 and Fig. 10 confirm this equivalence in practice, with both tests producing identical waveforms once the converter settles after morphing.

It is noted that HIL validation does not capture all non-idealities of a physical prototype, such as parasitic elements and device-level transient stresses. Nevertheless, transient handling during transitions between operating modes is a well-established topic, with techniques such as zero-crossing-based transitions and the use of DC-blocking capacitors commonly adopted to mitigate transients [31]. Since the proposed morphing strategy involves a transition between two known converter topologies, the HIL results effectively validate the control logic and transition behavior.

To quantitatively assess the power-tracking quality of the proposed controller, the measured power was compared with the reference power over the complete charging profile, illustrated in Fig. 11 and Fig. 12 for both the 800 V-800 V and 800 V-400 Voperating cases. In both cases, the measured points align closely with the bisecting line, confirming that accurate power regulation is maintained across the full operating range. The coefficients of determination is calculated to be $R^2 = 0.9999$ for all the modulation combinations, indicating that the control performance remains excellent in both cases. The zoomed regions simply highlight the slight deviation from the measured points and the bisecting line, whereas the transition point itself is clearly visible in the full plots. Overall, the analysis confirms that both cases are compatible with the proposed morphing strategy. Although the 800 V–800 V and

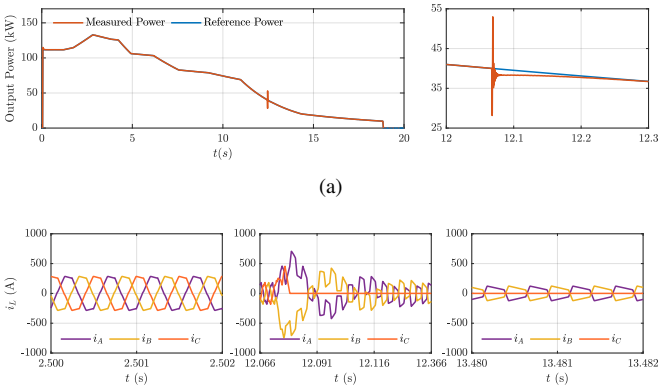


FIGURE 9: HIL results for the 800 V-400 V operating case using duty-cycle modulation on the primary and inner phase shift on the secondary. (a) Measured and reference output power, including a zoomed view during the morphing instant. (b) Inductor current waveforms highlighting the three operating stages: balanced three-phase operation, phase shedding during the morphing instant, and steady single-phase operation at light-load.

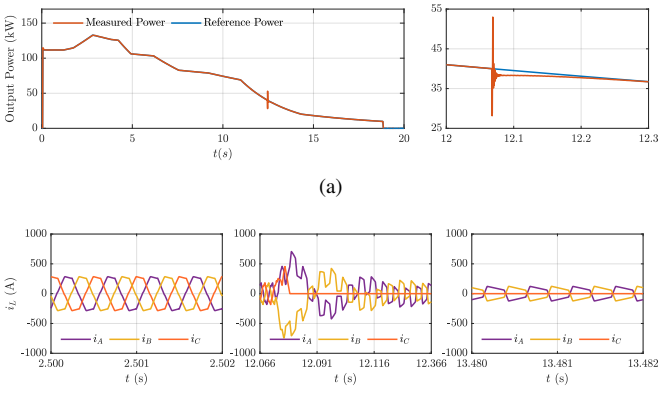


FIGURE 10: HIL results for the 800 V-400 V operating case using duty-cycle modulation on both the primary and the secondary. (a) Measured and reference output power, including a zoomed view during the morphing instant. (b) Inductor current waveforms highlighting the three operating stages: balanced three-phase operation, phase shedding during the morphing instant, and steady single-phase operation at light-load.

800 V–400 V cases correspond to different power ratings, these results primarily validate the proposed control and morphing logic rather than a specific converter rating. Scaling the converter to higher or lower power levels mainly affects hardware-related aspects, such as semiconductor selection, thermal design, and passive component sizing, while the underlying control philosophy and morphing criteria remain unchanged. Consequently, the proposed approach can be extended to converters operating in different power classes.

Fig. 13 and 14 present the measured switch current waveforms for switch 1A under all tested modulation cases, shown at the same time instants depicted in the inductor

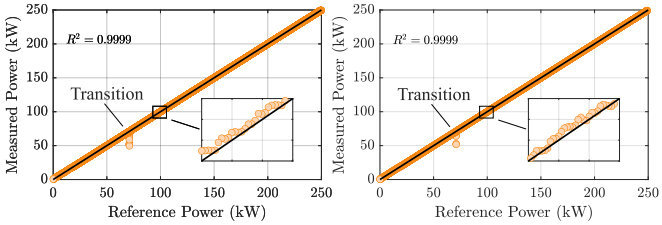


FIGURE 11: Measured power versus reference power across the complete charging profile for 800 V-800 V case: (a) inner phase shift on both primary and secondary; (b) duty-cycle modulation on both primary and secondary.

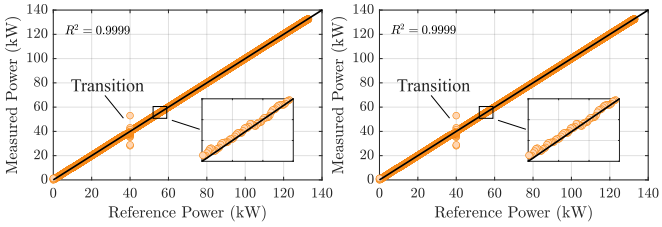


FIGURE 12: Measured power versus reference power across the complete charging profile for 800 V-400 V case: (a) Duty-cycle on primary and inner phase shift on secondary; (b) Duty-cycle on both the primary and secondary.

current results of Fig. 7–Fig. 10. In Fig. 13(a), the right-hand plot corresponds to the 800 V-800 V operating condition in full three-phase mode, whereas the left-hand plot shows the morphed single-phase DAB with inner phase-shift control applied on both primary and secondary bridges. Fig. 13(b) presents the same comparison for the duty-cycle modulation case, again showing three-phase operation on the right and the corresponding single-phase duty-controlled waveforms on the left. The reported RMS values illustrate the difference in switch current between the three-phase and single-phase operating regions, reflecting the higher power handled during the three-phase interval. For the 800 V-800 V power profile used in this study, the maximum RMS switch current observed is approximately 204 A.

Similarly, Fig. 14 illustrates the 800 V-400 V operating case. In Fig. 14(a), the left-hand plot shows the morphed topology with duty-cycle modulation on the primary and inner phase shift on the secondary, while Fig. 14(b) applies duty-cycle modulation on both sides. In both figures, the right-hand plot represents the original three-phase operation prior to morphing. The reduced RMS currents observed in the single-phase plots reflect the lower transmitted power in that region, while the morphing strategy enables operation at this operating point without compromising efficiency. For the 800 V-400 V power profile used in this study, the maximum RMS switch current observed is approximately 172 A. Thus, the RMS switch currents observed in all modulation cases fall within the continuous current capability of the CAS300M17BM2 module. In this work, the morphing

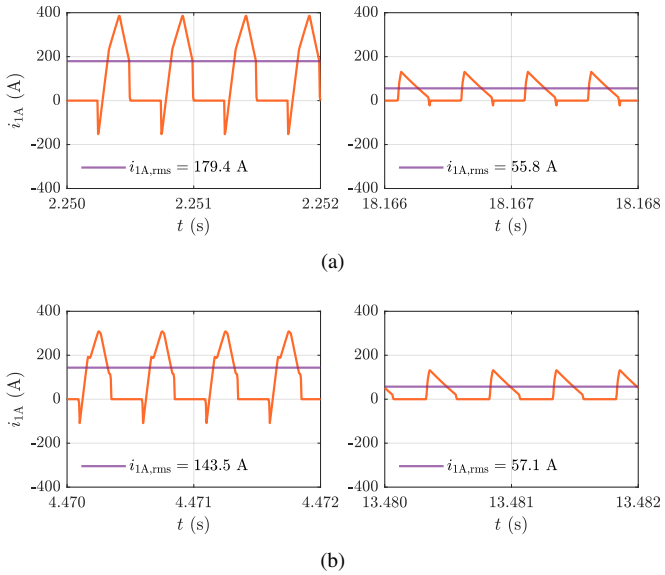


FIGURE 13: Switch 1A current comparison for the 800 V–800 V case: three-phase operation (right) and single-phase operation (left) for (a) inner phase-shift on both primary and secondary sides and (b) duty-cycle control on both primary and secondary sides, with RMS values indicated.

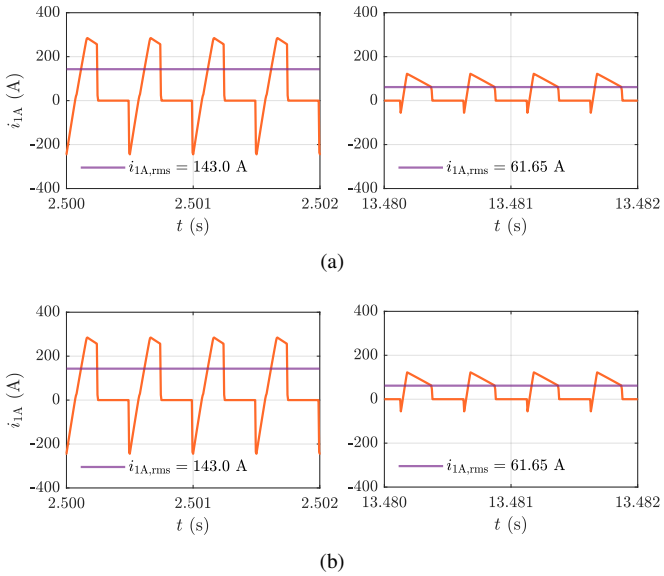


FIGURE 14: Switch 1A current comparison for the 800 V–400 V case: three-phase operation (right) and single-phase operation (left) for (a) duty-primary/inner-secondary and (b) duty-primary/duty-secondary, with RMS values shown.

threshold is selected based on the transferable power capability of the morphed topology. Alternatively, RMS current can be adopted as a criterion for threshold selection in applications where thermal stress or lifetime considerations are more critical. It is also acknowledged that single-phase operation may introduce thermal imbalance between the switches. This can be mitigated through established techniques such as leg rotation shedding, which allow the thermal stress to be distributed among the semiconductor devices over time.

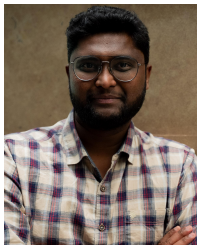
VI. CONCLUSION

This manuscript demonstrated a morphing-based control strategy for the three-phase three-level DAB that enables high-efficiency operation across both 800 V and 400 V EV battery systems without hardware modifications. By transitioning to a single-phase structure at light-load and employing DPS-based modulation, peak current is minimized while significantly reducing current-invariant losses. Analytical modeling confirmed that inner phase shift, duty-cycle, and T-type modulation generate identical voltage and current waveforms in the morphed configuration. Simulation-derived efficiency maps showed that inner phase shift and duty-cycle modulation are the most effective among the nine possible combinations in the 800 V-800 V case, and among the three viable options in the 800 V-400 V. Hardware-in-the-loop validation further demonstrated stable morphing, a disturbance-free current transition, and near-perfect power-tracking accuracy, with $R^2 = 0.9999$ across the entire charging profile for both voltage levels. Overall, the analytical, simulation, and HIL results confirm that the proposed morphing technique is a practical and high-efficiency solution for wide-range EV fast-charging applications. Future work will focus on the experimental validation of the proposed morphing strategy on a hardware prototype, with particular attention to transient behavior and device-level stresses during topology transitions. In addition, the extension of the proposed approach to higher switching frequencies and modular converter architectures, which are commonly adopted in lower-power or modular EV fast-charging systems, will be investigated. A detailed analysis of current redistribution, thermal loading, and semiconductor stress under morphed single-phase operation will also be addressed.

REFERENCES

[1] C. Jung, "Power up with 800-v systems: The benefits of upgrading voltage power for battery-electric passenger vehicles," *IEEE Elect. Mag.*, vol. 5, no. 1, pp. 53–58, 2017.
[2] H. Wouters and W. Martinez, "Bidirectional onboard chargers for electric vehicles: State-of-the-art and future trends," *IEEE Tran. Power Electron.*, vol. 39, no. 1, pp. 693–716, 2024.
[3] G. Rituraj, G. R. C. Mouli, and P. Bauer, "A comprehensive review on off-grid and hybrid charging systems for electric vehicles," *IEEE Op. Jr. Ind. Electron. Soc.*, vol. 3, pp. 203–222, 2022.
[4] G. Arena, A. Chub, M. Lukianov, R. Strzelecki, D. Vinnikov, and G. De Carne, "A comprehensive review on dc fast charging stations for electric vehicles: Standards, power conversion technologies, architectures, energy management, and cybersecurity," *IEEE Op. Jr. Power Electron.*, vol. 5, pp. 1573–1611, 2024.
[5] E. L. Carvalho, A. Sidorova, A. Blinov, A. Chub, and D. Vinnikov, "Design considerations of dual-active bridge dc grid-forming converter for dc buildings," *IEEE Tran. Ind. Electron.*, vol. 71, no. 9, pp. 10 601–10 611, 2024.
[6] R. Pradhan, S. B. Shah, M. I. Hassan, Z. Wang, and A. Emadi, "A 15-kw wide-input reconfigurable three-level dab converter for on-board charging of 1.25-kv electric vehicle powertrains," *IEEE Tran. Transp. Elect.*, vol. 10, no. 4, pp. 9144–9162, 2024.
[7] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Tran. Ind. App.*, vol. 27, no. 1, pp. 63–73, 1991.

[8] S. Cuoghi, L. K. Pittala, R. Mandrioli, V. Cirimele, M. Ricco, and G. Grandi, "Model-based adaptive control of modular dab converter for ev chargers," *IET Power Electron.*, vol. 17, no. 16, pp. 2669–2685, 2024.
[9] S. Shao, L. Chen, Z. Shan, F. Gao, H. Chen, D. Sha, and T. Dragičević, "Modeling and advanced control of dual-active-bridge dc–dc converters: A review," *IEEE Tran. Power Electron.*, vol. 37, no. 2, pp. 1524–1547, 2022.
[10] N. Baars, "Three-phase dual active bridge converters: a multi-level approach for wide voltage-range isolated dc-dc conversion in high-power applications," Phd Thesis 1 (Research TU/e / Graduation TU/e), Electrical Engineering, Nov. 2017, proefschrift.
[11] J. Hu, N. Soltau, and R. W. De Doncker, "Asymmetrical duty-cycle control of three-phase dual-active bridge converter for soft-switching range extension," in *Proc. Ene. Conv. Cong. Expo. (ECCE)*, 2016, pp. 1–8.
[12] P. Liu, C. Chen, S. Duan, and W. Zhu, "Dual phase-shifted modulation strategy for the three-level dual active bridge dc–dc converter," *IEEE Tran. Ind. Electron.*, vol. 64, no. 10, pp. 7819–7830, 2017.
[13] C. Li, J. Liu, S. Du, H. Dang, Z. Deng, and H. Chen, "A t-type dab-based isolated dc-dc-ac three-port converter with high power efficiency," *IEEE Tran. Power Electron.*, vol. 38, no. 11, pp. 14 178–14 194, 2023.
[14] D. Yadeo and P. Chaturvedi, "Performance characterization of t-type multilevel dual active bridge dc-dc converter," *IEEE Tran. Ind. App.*, vol. 59, no. 2, pp. 1877–1886, 2023.
[15] J. Pang, K. Wang, Z. Zheng, T. Zheng, and Y. Li, "Quasi two-level operation and neutral-point voltage balance method for a four-level anpc based dual active bridge dc-dc converter," in *Proc. Ene. Conv. Cong. Expo. (ECCE)*, 2022, pp. 1–7.
[16] L. K. Pittala, R. Barbone, R. Mandrioli, V. Cirimele, M. Ricco, and G. Grandi, "Insights on dab converter with auxiliary inductors," in *Proc. Int. Conf. Clean Ele. Power (ICCEP)*, 2023, pp. 458–463.
[17] F. Grazian, T. B. Soeiro, and P. Bauer, "Voltage/current doubler converter for an efficient wireless charging of electric vehicles with 400-v and 800-v battery voltages," *IEEE Tran. Ind. Electron.*, vol. 70, no. 8, pp. 7891–7903, 2023.
[18] R. Mandrioli, F. Grazian, L. K. Pittala, M. Ricco, and G. Papafotiou, "Three-phase three-level dual active bridge for ev charging: Wide output voltage range with light-load soft-switching morphing," in *Proc. Seventh Int. Conf. DC Mg. (ICDCM)*, 2025, pp. 1–6.
[19] B. Zhao, Q. Song, W. Liu, and W. Sun, "Current-stress-optimized switching strategy of isolated bidirectional dc–dc converter with dual-phase-shift control," *IEEE Tran. Ind. Electron.*, vol. 60, no. 10, pp. 4458–4467, 2013.
[20] R. Mandrioli, M. Ricco, G. Grandi, T. A. Pereira, and M. Liserre, "Dab-based common-mode injection in three-phase four-wire inverters," in *Proc. Int. Conf. Comp., Power Electron. Power Eng. (CPE-POWERENG)*, 2022, pp. 1–6.
[21] N. H. Baars, J. Everts, C. G. E. Wijnands, and E. A. Lomonova, "Performance evaluation of a three-phase dual active bridge dc–dc converter with different transformer winding configurations," *IEEE Tran. Power Electron.*, vol. 31, no. 10, pp. 6814–6823, 2016.
[22] Z. Xiao, Z. Yao, F. Deng, L. Zhang, and Y. Tang, "Seamless rotational phase shedding for multiphase dc–dc converters," *IEEE Tran. Power Electron.*, vol. 39, no. 5, pp. 4996–5001, 2024.
[23] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics," in *Proc. 7th Int. Conf. Integrated Power Electron. Sys. (CIPS)*, 2012, pp. 1–22.
[24] P. Liu, C. Chen, and S. Duan, "An optimized modulation strategy for the three-level dab converter with five control degrees of freedom," *IEEE Tran. Ind. Electron.*, vol. 67, no. 1, pp. 254–264, 2020.
[25] S. Luo, F. Wu, and G. Wang, "Single-stage hybrid three-level dab type resonant ac–dc converter," *IEEE Tran. Transp. Elect.*, vol. 8, no. 1, pp. 799–807, 2022.
[26] P. Jing, C. Wang, W. Jiang, and G. Zhang, "Performance analysis of isolated three-level half-bridge bidirectional dc/dc converter," in *Proc. 7th Int. Power Electron. Mot. Cont. Conf.*, vol. 3, 2012, pp. 1527–1531.
[27] K. Kim and H. Cha, "Split-capacitor dual-active-bridge converter," *IEEE Tran. Ind. Electron.*, vol. 68, no. 2, pp. 1445–1453, 2021.
[28] J. Geng, R. Mandrioli, A. Sangwongwanich, and M. Ricco, "Impacts of sps, dps, and eps modulations on the reliability of modular dab ev chargers," in *Proc. Int. Conf. Comp., Power Electron. Power Eng. (CPE-POWERENG)*, 2025, pp. 1–6.
[29] "Dc ccs power classes for bidirectional charging," in *Charging Interface Initiative (CharIN) e.V.*, 2023. [Online]. Available: https://www.charin.global/media/pages/technology/knowledge-base/bb62e2344d-1686142056/20230605-power-classes-bidirectional-v1.07.pdf
[30] F. Lo Franco, M. Ricco, V. Cirimele, V. Apicella, B. Carambia, and G. Grandi, "Electric vehicle charging hub power forecasting: A statistical and machine learning based approach," *Energies*, vol. 16, no. 4, 2023.
[31] L. Xu, J. Wang, X. Guo, C. Wang, and Q. Cheng, "Intrinsic dc-bias-free control for dual active bridge dc-dc converters based on zero initial current switching sequence construction," *IET Power Electronics*, vol. 18, no. 1, p. e70133, 2025.



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