BTI saturation and universal relaxation in SiC power MOSFETs

BTI saturation and universal relaxation in SiC power MOSFETs

Luis Sanchez[1], Eliana Acurio[2], Felice Crupi[3], Susanna Reggiani[4], Gaudenzio Meneghesso[5]

[1] DFB, Escuela Politécnica Nacional (EPN), Quito, Ecuador,

[2] Physics Department, Escuela Politécnica Nacional (EPN), Quito, Ecuador

[3]DIMES, Università della Calabria, Rende, Italy

[4] ARCES and DEI, Università di Bologna, Bologna, Italy

[5] Università di Padova, Padova, Italy

Abstract - This work focuses on the positive bias temperature instability of SiC-based MOSFETs under different stress voltages and temperatures. Stress experiments demonstrate that the threshold voltage shift (ΔV_{th}) does not follow a conventional power law for long stress time, but exhibits a saturating log- time dependence attributed to the charge trapping in the pre-existing defects at the SiC/SiO_2 interface or in the SiO_2 layer. The maximum V_{th} shift (ΔV_{max}), which is a function of the total trap density, increases with the stress voltage (V_{stress}) and decreases for temperatures higher than 50 °C. The time constant of the traps (τ_0) also shows an uptrend with V_{stress} with a maximum value around 50 °C. Moreover, the trap energy distribution (γ) slightly increases with temperature. The recovery analysis shows that an empiric universal relaxation function well describes the data with a dispersion parameter (β) that follows the Arrhenius law. Finally, the V_{th} recovery, after the same V_{stress}, is enhanced with temperature and also depicts a linear behavior on the Arrhenius plot. This indicates that the charge de-trapping process is thermally activated and explains the low degradation observed at high temperatures during the stress phase.

Keywords—De-trapping, PBTI, recovery, universal relaxation, SiC, trapping, Zafar's model.

1. Introduction

Silicon Carbide (SiC) metal-oxide semiconductor-field-effect-transistors (MOSFETs) are innovative devices with excellent wide-bandgap properties, as well as a higher critical electric field (Ec = 3 × 10^6 V/cm) and superior thermal conductivity (k = 5 W/cmK) compared to Si and GaN technologies. Furthermore, they feature a very tight variation of on-resistance vs. temperature, very high operation junction temperature capability, very fast and robust intrinsic body diode and low capacitance [1]. Therefore, SiC devices have captured important attention in the market because they fulfill most of the required properties for high-power and high-temperature applications. Moreover, SiC is the only compound whose native oxide is SiO_2 (the same insulator as Silicon), which eases the fabrication of the entire family of MOS-based electronic devices.

In the last decades, many efforts have been focused on developing SiC with better features such as different presentations of crystals (3C-SiC, 4H-SiC and 6H-SiC) and processing device technology based on this material. Due to the number of breakthroughs obtained in industrial and academic research during the 1980s and 1990s, first SiC Schottky barrier diodes (SBDs) were commercially released in 2001. From that on, SiC power switching devices, primarily JFETs (junction field-effect transistors) and MOSFETs have been employed in a variety of power systems since the size and weight can be reduced by a factor of 4–10 with a substantial power dissipation reduction [1].

One of the main concerns from the industrial point of view is the reliability of SiC-based devices in different processes and is the main motivation for this work because new power devices with wide bandgap could offer great monetary and space savings. Recent reliability studies in SiC MOSFET use positive bias temperature instability (PBTI) and the recovery phase analysis to determine the traps contribution in reducing oxide reliability [2,3]. It has been concluded that the measuring action can cause de-trapping in PBTI or even trapping during the recovery, so new measurement methods have been developed [4]. This paper aims to provide a more comprehensive analysis of the PBTI in SiC-based MOSFETs, under different stress conditions (temperature and voltage) by using DC characterization and independently analyzing the stress and the recovery phase. This paper examines the dynamics of the threshold voltage V_{th} to find appropriate models that correctly describes the stress and relaxation behavior for prolonged test periods (10^4 s) beyond the conventional ones [5] and allows extracting information about the degradation mechanisms of this

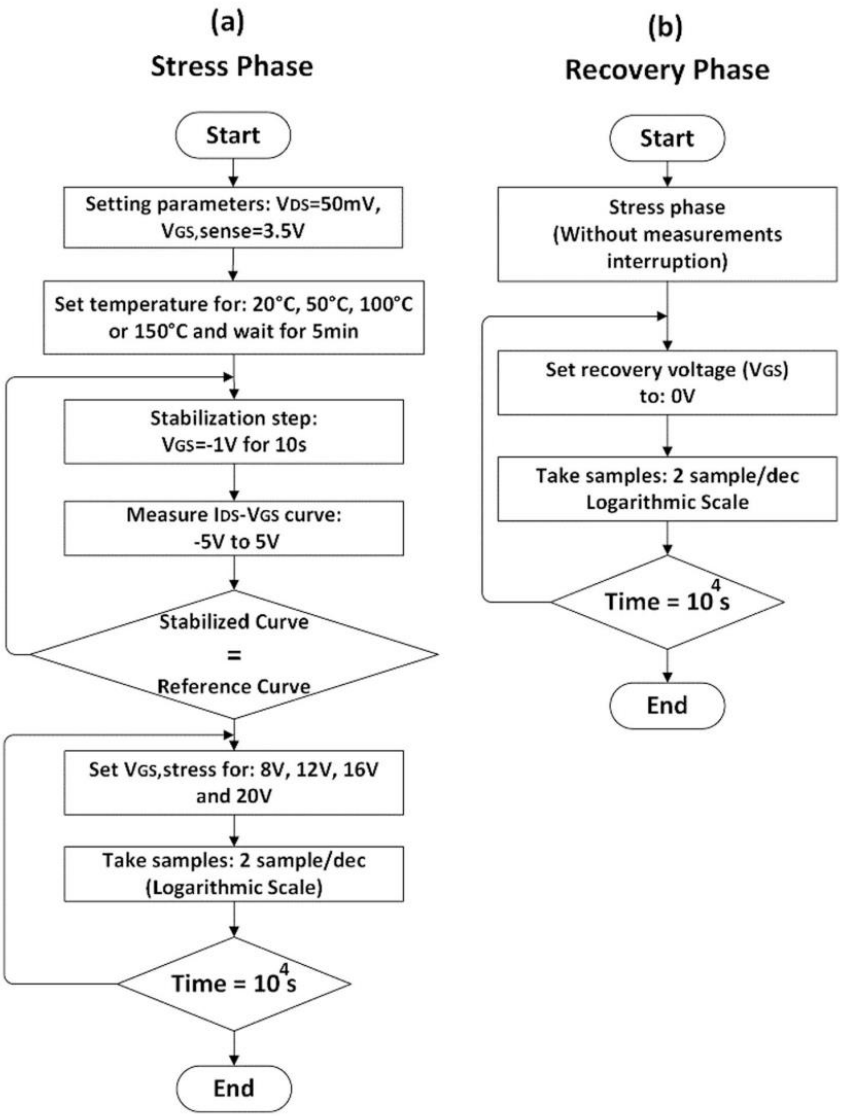

Fig. 1. Testing procedure diagram for (a) the stress and (b) the recovery phase.

device. Since this work also uses an initial stabilization phase and a recovery behavior analysis with an uninterrupted stress phase, a more accurate PBTI degradation can be extracted.

The remainder of this paper is organized as follows: in Section 2, we provide details of the device fabrication and characterization methodology; in Section 3, we discuss the results obtained under different conditions; and finally, in Section 4 the main achievements of this paper are summarized.

2. Device specifications and characterization methodology

BTI measurements were carried out on packaged commercial SiC power MOSFETs, characterized by a breakdown voltage of 1200 V and a maximum R_{DSon} at $V_{GS} = 20$ V, $I_D = 40$A and $T = 25$ °C equal to 69 mΩ. The electrical characterization was performed by using the measurement routines of the parameter analyzer Keithley 4200-SCS.

Fig. 1 shows the flow diagram of the measurement procedure to acquire data during the stress and recovery phase, respectively.

Before performing PBTI stress, an initial stabilization phase was done. This phase consists of applying a negative gate voltage (−1 V) for 10s to release charges originally contained in trapping centers [6]. The stabilization allows the device to reach a reproducible reference state for the subsequent experiments. After this phase, we measured a complete I_D-V_{GS} curve by sweeping V_{GS} from −5 V to 5 V. PBTI stress measurements were done by applying different V_{GS} (from 8 V to 20 V), different temperatures (from 20 °C to 150 °C) and biasing $V_{DS} = 50$ mV. The stress was interrupted at fixed time intervals (2 samples per decade until 10^4 s) to monitor the threshold voltage shift (V_{th}) by sensing I_D at $V_{GS} = 3.5$ V [7,8].

In order to monitor the recovery evolution, devices were stressed at $V_{GS} = 8$ V for 10^4 s without interruptions and afterward were biased at $V_{GS} = 0$. The relaxation was interrupted at fixed time intervals to sense

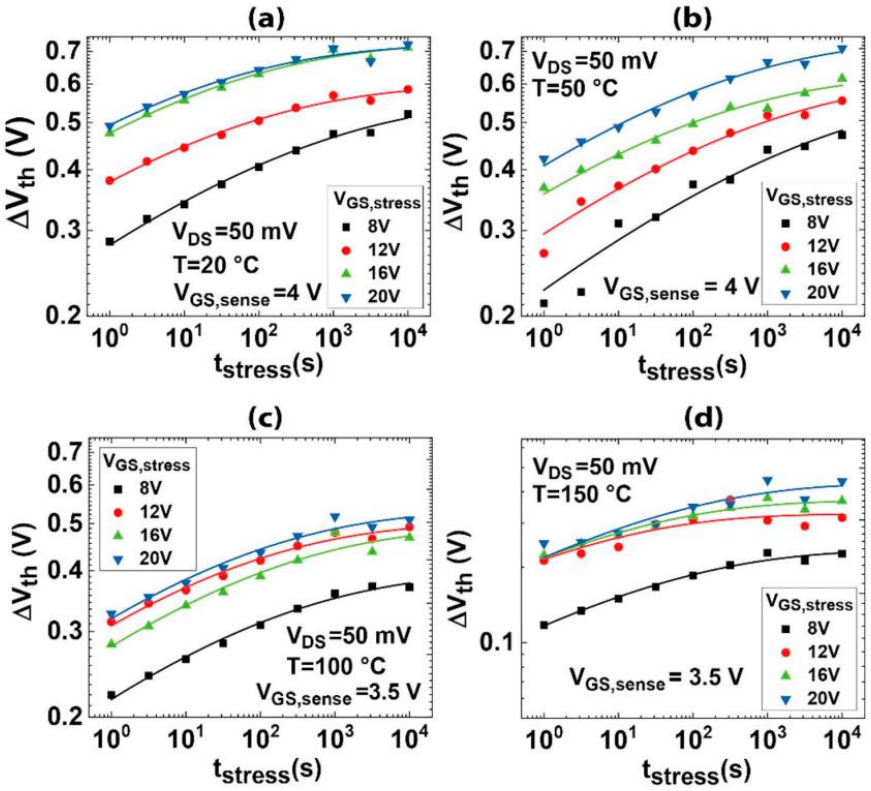

Fig. 2. Experimental (markers) and fitting curves (lines) of the ΔV_{th} evolution during the stress phase under different stress voltages and temperatures (a,b,c,d).

I_D at V_{GS} = 3.5 V and consequently ΔV_{th}.

3. Results and discussion

3.1. Stress phase

Fig. 2 shows the evolution of PBTI induced ΔV_{th} under different stress voltage and temperatures. A ΔV_{th} saturation behavior is observed for prolonged stress time over 1000 s, which agrees with the charge-trapping process in pre-existing defects located in the gate dielectric without the generation of extra traps described by Zafar et al. [9]. This model predicts the dependence of threshold voltage shift on injected charge carrier density (N_{inj}) as follows:

$$\Delta V_{th} = \Delta V_{max}[1 - exp(-(N_{inj}.\ \sigma_0)^{\beta})] \quad (1)$$

where ΔV_{max} is related to the total trap density and the centroid of the trap-charge distribution in space, β is a dependent constant of the gate stack, and σ_0 is the characteristic capture cross-section for the ensemble of traps with a continuous distribution [10].

Eq. (1) can also be expressed as a function of the total stress time t by the expression:

$$\Delta V_{th} = \Delta V_{max}\left[1 - exp\left(-\left(\frac{t}{\tau_0}\right)^{\gamma}\right)\right] \quad (2)$$

where τ_0 is the time constant of the traps and γ describes the trap energy distribution through $\gamma = (1 - \alpha)\beta$, where α is determined from gate leakage current density vs. time plot [9].

According to the previously described model, ΔV_{max} (Fig. 3) obtained from the stress phase exhibits upward behavior until 50 °C and then decreases at higher temperatures. This indicates an initial charge-trapping that is diminished by a natural thermal-activated de-trapping process [5].

Furthermore, as depicted in Fig. 3, τ_0 exhibits a maximum value around 50 °C and a decreasing behavior for elevated temperatures such as 100 °C and 150 °C.

Finally, γ (Fig. 3), which describes the distribution of traps, slightly increases with temperature and is ascribed to faster charge de-trapping during the measurement delay between the stress and sense.

It is important to mention that according to Zafar's model β is constant for all ΔV_{th} vs. t_{stress} curves. Since it depends on the gate stack structure and materials, different values have been reported in the literature [10].

Summarizing the stress results (ΔV_{max}, τ_0 and γ), one can say that the investigated SiC Power MOSFET shows maximum degradation at 20 °C and 50 °C as indicated in Table 1. Meanwhile, the minimum degradation is obtained at high temperatures (100 °C and 150 °C) at low V_{stress} due to the fast natural de-trapping process. These results agree with previous work in SiC devices as illustrated in Fig. 4.

3.2. Recovery phase

The partial recovery once the stress is removed to perform the characterizing I_D-V_{GS} curve cannot be neglected because it results in an underestimation of the PBTI degradation even at ultra-fast measurement techniques. Therefore, the universal relaxation model that is

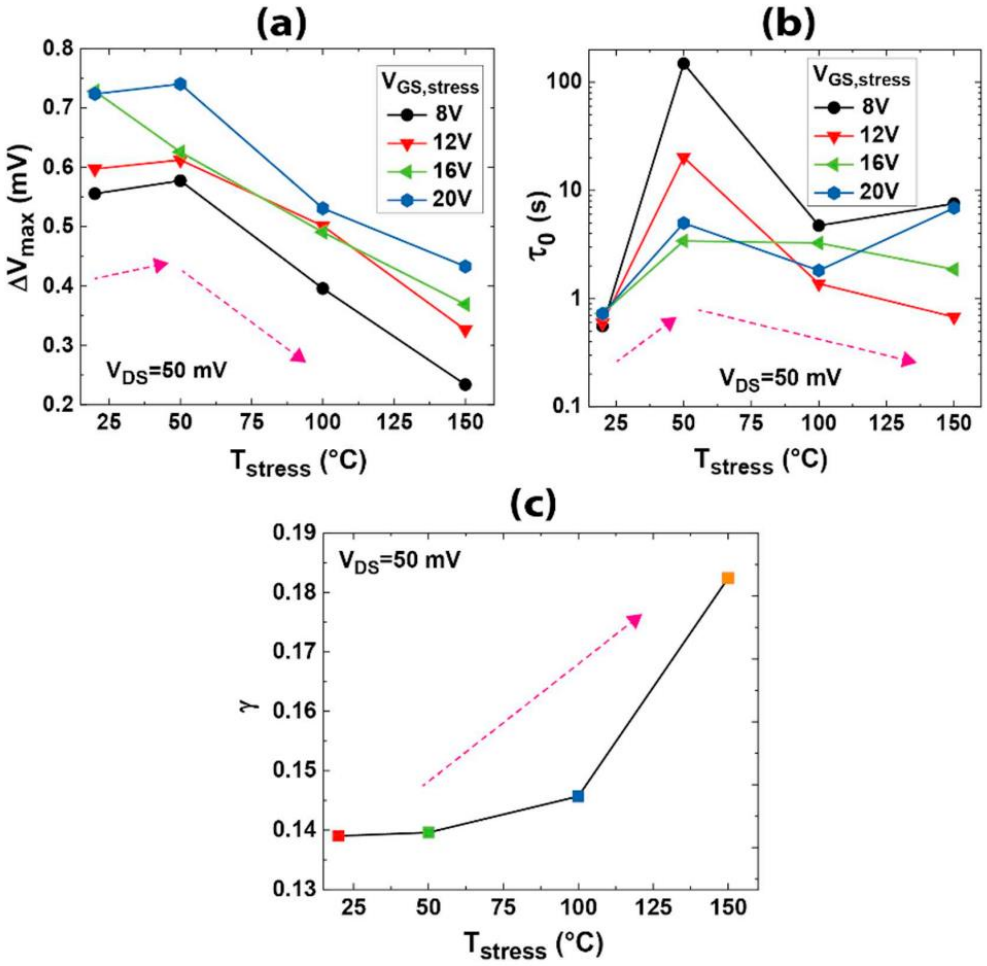

Fig. 3. Evolution of Zafar's parameters (markers): (a) ΔV_{max}, (b) τ_0 and (c) Υ under different stress voltages and temperatures. Lines are for eye guidance.

Table 1
Maximum degradation parameters (V_{stress} = 20 V).

Temperature (°C)	ΔV_{max}(V)	τ_0 (s)	Υ
20	0.72	0.723	0.1390
50	0.74	4.989	0.1396

based on the observation of certain common features through different studies appears in response to the difficulty of minimizing the measurement delay [11].

The first step of this methodology is to normalize the relaxation data $R(t_{stress}, t_{relax})$ captured at different t_{stress} to the first available point, which is recorded after a measurement delay t_M. This is called fractional recovery and is given by the following expression:

$$r_f(t_{stress}, t_{relax}) = \frac{R(t_{stress}, t_{relax})}{R(t_{stress}, t_M)} \quad (3)$$

By using the relation between the fractional recovery (r_f) and the relaxation function ($r(\xi)$), it is possible to extract the fitting parameters that better adjust the obtained recovery data

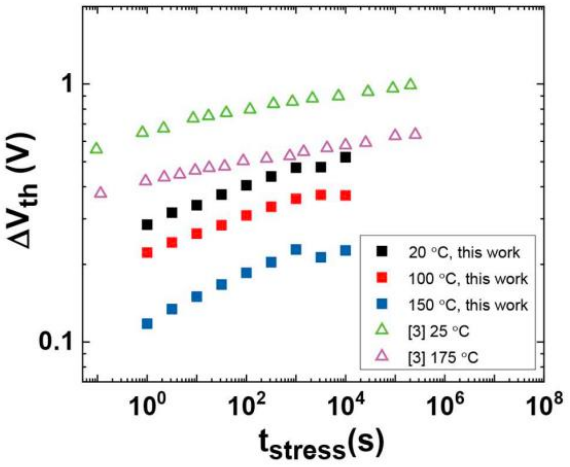

Fig. 4. Degradation comparison of the data obtained from stress measurements with previous work [3].

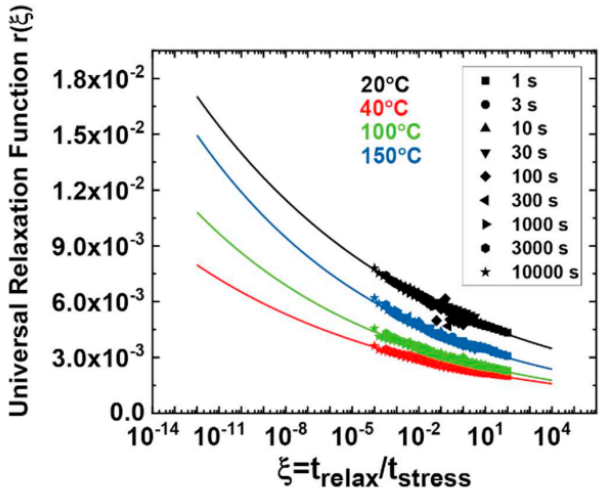

Fig. 5. Experimental (markers) and fitting curves (lines) of the measured recovery values fitted with the universal relaxation function.

$$\frac{r(\xi)}{r(\xi_M)} = \frac{R(t_{stress}, t_{relax})}{R(t_{stress}, t_M)} \tag{4}$$

where $\xi = t_{relax}/t_{stress}$ and $\xi_M = t_M/t_{stress}$. Several empirical expressions have already been proposed to fit the measured relaxation data [7], but in this work, the generalized form given by

$$r(\xi) = \frac{1}{1 + B\xi^{\beta}} \tag{5}$$

is used since it covers a larger range of measurement data and exhibits an asymptotic limit for large and/or small ξ. By introducing the above function into Eq. (4), the scaling B and the dispersion parameter can be easily obtained. Once the relaxation data is fitted, it is possible to get a rough estimation of the recoverable component $R(t_{stress}, t_{relax} = 0)$ at a relaxation time $t_{relax} = 0$.

The BTI relaxation property of scaling with the universal relaxation time, ξ, allows fitting the complete ΔV_{th} recovery with a single set of parameters B and β by using the expression:

$$\Delta V_{th} = R(t_{stress}, t_{relax} = 0) r(\xi) + P(t_{stress}) \tag{6}$$

where $P(t_{stress})$ is the permanent component. Since the I_D-V_{GS} curve always comes back to the original reference state after the stress phase under different stress conditions (not shown for the sake of brevity), we assumed $P(t_{stress}) = 0$ for the analyzed stress voltages and temperatures. It is worth mentioning that this assumption also coincides with the model of the stress phase where there is no generation of new traps.

Fig. 5 depicts that the recovery values are well described by the universal relaxation model under different stress temperatures and can be explained by the electron de-trapping from the defect sites located at the interface and in the gate oxide.

As illustrated in Fig. 6, the scaling parameter B does not follow a clear trend with the temperature, while the dispersion parameter follows the Arrhenius law with relatively low activation energy E_a = 13.45 meV. The latter temperature dependence agrees with the predictions of dispersive hydrogen transport models [11,12]. The ΔV_{th} evolution during the recovery phase at different temperatures is well adjusted by using the Eq. (6) as shown in Fig. 7. As previously mentioned (stress phase results), the temperature acts as an accelerating factor of the de-trapping process. Therefore, the first measured value during the recovery (FMVR) for the same V_{stress} and t_{stress} decreases with temperature and also exhibits an Arrhenius behavior as observed in the example of Fig. 8.

4. Conclusions

This study evaluated PBTI in market packaged SiC MOSFETs. The presented measurement methodology allows separately analyzing and understanding the trapping (stress) and de-trapping (recovery) processes. Since the recovery data are obtained with no measurement interruption during the stress, a closer value to the true threshold voltage degradation is acquired. The observed ΔV_{th} is mainly ascribed to electron trapping at the interface or border traps. The PBTI evolution shows a saturation behavior for prolonged stress time (10^4 s) well described by Zafar's model. The anomalous decrease with temperature is ascribed to faster de-trapping at higher temperatures during the measurement delay between stress and sense. During the recovery phase, high temperature accelerates the charge de-trapping process and the V_{th} dynamics is properly described by the empirical universal relaxation function, where the dispersive parameter and the FMVR follow the Arrhenius law. The acquired data during the stress and recovery phase

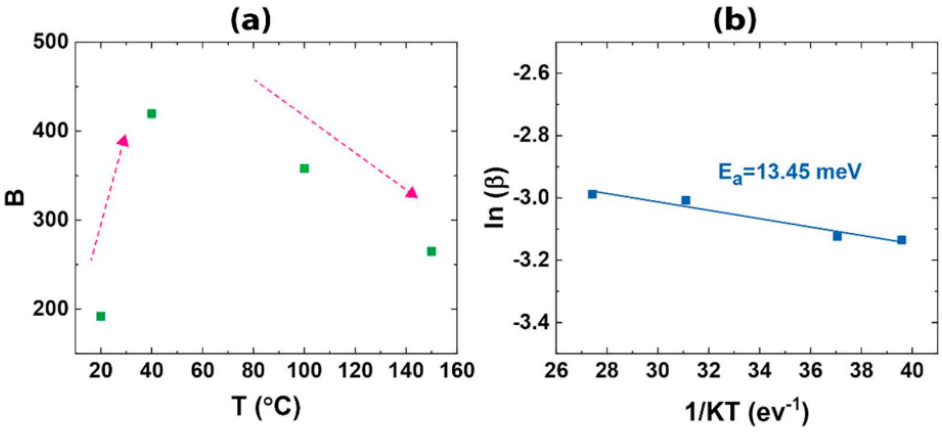

Fig. 6. Temperature dependence of the scaling B (a) and dispersion parameter β (b).

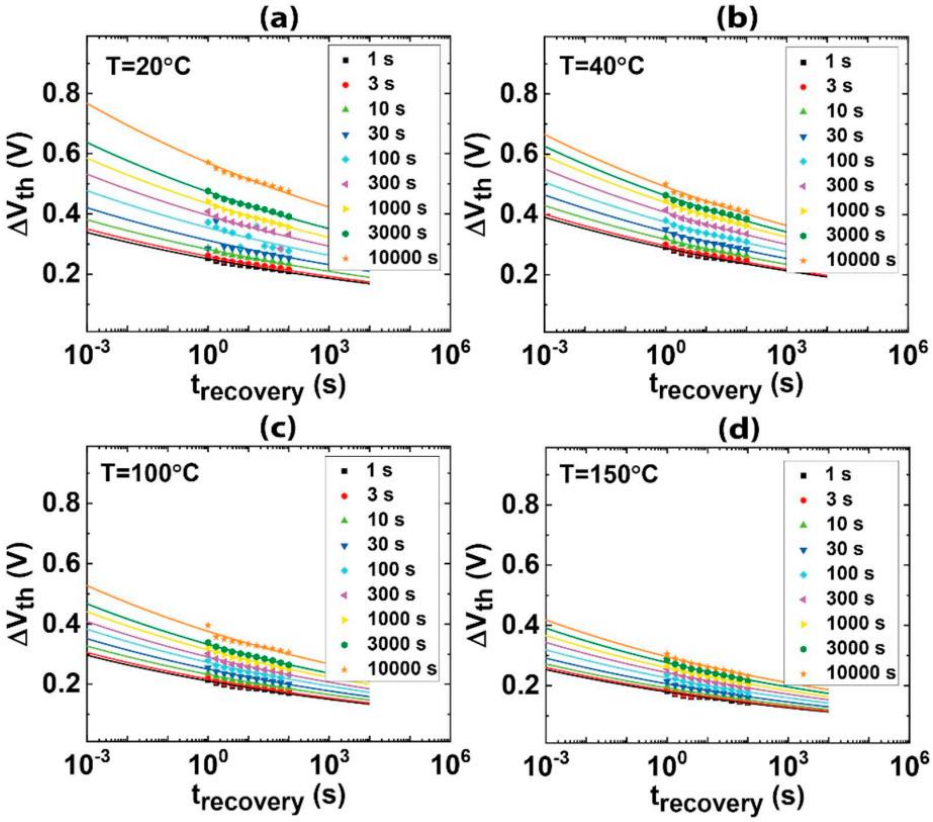

Fig. 7. ΔVth recovery evolution after applying a V_{stress} = 8 V at different t_{stress} and temperatures (a,b,c,d).

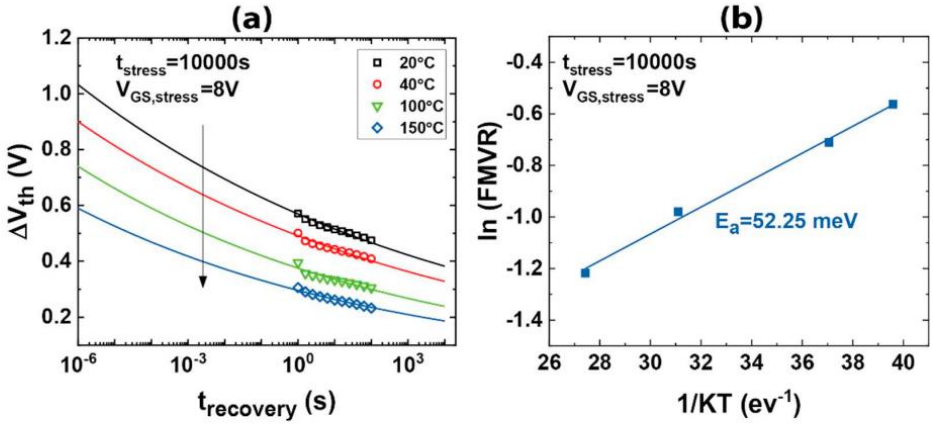

Fig. 8. (a) Relaxation data after t_{stress} = 10,000 s and V_{stress} = 8 V at different temperatures. (b) Arrhenius plot of the first measured value during the recovery (FMVR).

indicates no permanent damage. Therefore, the observed degradation could be exclusively ascribed to pre-existing defects.

CRediT authorship contribution statement

Luis Sánchez:Conceptualization, Methodology, Formal analysis, Investigation, Data curation.**Eliana Acurio**:Methodology, Software, Formal analysis, Investigation, Writing - original draft.**Felice Crupi**:Conceptualization, Writing - review & editing, Supervision.**Susanna Reggiani**:Writing - review & editing, Supervision.**Gaudenzio Meneghesso**:Writing - review & editing, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by the ECSEL JU project WInSiC4AP (Wide Band Gap Innovative SiC for Advanced Power), grant agreement n. 737483.

References

[1] T. Kimoto, J.A. Cooper, Fundamentals of Silicon Carbide Technology, John Wiley & Sons Singapore Pte. Ltd, Singapore, 2014.

[2] D.B. Habersat, A.J. Lelis, R. Green, Measurement considerations for evaluating BTI effects in SiC MOSFETs, Microelectron. Reliab. 81 (February 2018) (Feb. 2018) 121–126, https://doi.org/10.1016/j.microrel.2017.12.015.

[3] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, T. Grasser, Understanding BTI in SiC MOSFETs and its impact on circuit operation, IEEE Trans. Device Mater. Reliab. 18 (2) (2018) 144–153 Jun https://doi.org/10.1109/TDMR.2018.2813063.

[4] J.A.O. Gonzalez, O. Alatise, A novel non-intrusive technique for BTI characterization in SiC mosfets, IEEE Trans. Power Electron. 34 (6) (2019) 5737–5747 Jun https://doi.org/10.1109/TPEL.2018.2870067.

[5] G. Consentino, E. Guevara, L. Sanchez, F. Crupi, S. Reggiani, G. Meneghesso, Threshold voltage instability in SiC power MOSFETs, International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, PCIM Europe 2019, 2019, pp. 7–9 no. May. (ISBN: 978-3-8007-4938-6).

[6] E. Acurio, F. Crupi, P. Magnone, L. Trojman, G. Meneghesso, F. Iucolano, On recoverable behavior of PBTI in AlGaN/GaN MOS-HEMT, Solid. State. Electron 132 (2017) 49–56 Jun https://doi.org/10.1016/j.sse.2017.03.007.

[7] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin, T. Grasser, Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation, 2017 IEEE International Integrated Reliability Workshop (IIRW), 2017, pp. 1–5, , https://doi.org/10.1109/IIRW.2017.8361232.

[8] S. Mahapatra, Fundamentals of Bias Temperature Instability in MOS Transistors, vol. 52, Springer India, New Delhi, 2016 no. 6.

[9] S. Zafar, A. Callegari, E. Gusev, M.V. Fischetti, Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks, J. Appl. Phys. 93 (11) (2003) 9298–9303 Jun https://doi.org/10.1063/1.1570933.

[10] E. Acurio, F. Crupi, P. Magnone, L. Trojman, F. Iucolano, Impact of AlN layer sandwiched between the GaN and the Al_2O_3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs, Microelectron. Eng. 178 (2017) 42–47 Jun https://doi.org/10.1016/j.mee.2017.04.044.

[11] T. Grasser, W. Gos, V. Sverdlov, B. Kaczer, The universality of NBTI relaxation and its implications for modeling and characterization, 2007 IEEE International Reliability Physics Symposium Proceedings. 45th Annual, 2007, pp. 268–280, , https://doi.org/10.1109/REL-PHY.2007.369904.

[12] B. Kaczer, V. Arkbipov, R. Degraeve, N. Collaert, G. Groeseneken, M. Goodwin, Disorder-controlled-kinetics model for negative bias temperature instability and its experimental verification, 2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual, 2005, pp. 381–387, , https://doi.org/10.1109/RELPHY.2005.1493117.