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Impact of interface traps on the subthreshold performance of InGaAs nanosheet transistors☆

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ABSTRACT

The performance of InGaAs based transistors can be significantly affected by the presence of interface traps, particularly in the subthreshold regime. In this study, the role of such defects has been investigated through the fabrication and the characterization of MOSCAP structures and nanosheet transistors. TCAD simulations have been used to extract interface-trap densities. Results reveal that the distributed defect tail into the bandgap is ~5 × 10^{11} cm^{-2} eV^{-1} and degrades the subthreshold slope of about 39%, while interface traps inside the conduction band limit g_m^{MAX} to 561 μS/μm. The study emphasizes the need for improved interface engineering to unlock the full potential of nanoscale InGaAs-based devices.

1. Introduction

With the end of Moore's Law, research efforts are directed toward alternative solutions, including the use of new materials and advanced device architectures [1]. III–V compound semiconductors such as InGaAs are particularly attractive for low-power and high-speed logic applications due to their higher electron mobility and injection velocity with respect to Si-based technologies, enabling improved current drive capability [2,3]. But mere scaling down leads to serious performance degradation. By utilizing new geometries such as nanowires, promising results have been recently obtained showing than it is even possible to reach short-channel effect (SCE) immunity [4,5]. As silicon technology is approaching the transition to stacked nanosheet field-effect-transistors, there is growing interest in studying the equivalent InGaAs-based nanosheets as potential candidates for next RF technologies due to their high effective electron velocity [6]. However, a significant challenge in their development lies in the absence of a high-quality interfaces with low trap density (D_{it}) between the high-κ dielectric insulator and the InGaAs. Various interface engineering strategies have been explored to reduce D_{it}. These methods include atomic layer deposition (ALD) of the Al_2O_3 as gate dielectric and ammonia sulfide $(NH_4)_2S$ treatment, showing the minimum D_{it} in the midgap down to ~10^{12} cm^{-2} eV^{-1} [7], additional InGaAs surface nitridation, reducing it to ~2 × 10^{11} cm^{-2} eV^{-1} [8], and remote plasma treatment after high-κ/ Al_2O_3 gate oxide deposition for further improvement [9]. Similar ALD process can be applied for HfO_2, stacked HfO_2/Al_2O_3 or nanolaminated $HfAlO_x$ to reduce the equivalent oxide thickness down to 1–2 nm and the smallest D_{it} was shown by the stacked structure [10]. Although high-performance InGaAs devices have recently been demonstrated, interface traps still significantly affect device performance in terms of overall electrostatic control [5,6]. In this study, InGaAs MOS capacitors (MOSCAPs) and nanosheet MOSFETs incorporating an ALD aluminum oxide (Al_2O_3) interlayer and hafnium dioxide (HfO_2) barrier oxide, in combination with sulfur passivation and N_2 remote plasma treatment, were fabricated, characterized and simulated to investigate the impact of interface traps on device performance. The addressed geometries have been designed with large widths and heights in order to easily isolate the impact of the trap density at the Al_2O_3/InGaAs interface on the electrical performance, while minimizing the influence of SCEs and contact resistances. TCAD simulations have been performed to extract D_{it} and model its impact on the DC electrical behavior of the nanosheet transistors. Such findings provide valuable insight for the performance scaling rules.

2. Device fabrication and characterization

The fabricated devices are shown in Fig. 1. The MOSCAP was fabricated using the following process flow. The starting wafer consisted of an epitaxial InGaAs channel with doping concentration 5×10^{16} cm^{-3} grown on a (100)-oriented InP substrate by metal–organic chemical

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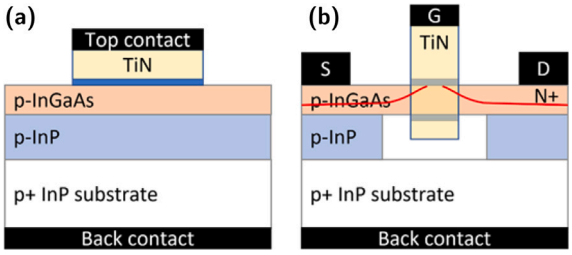

Fig. 1. Schematic cross-sections of the realized (a) MOSCAP and (b) nanosheet MOSFET.

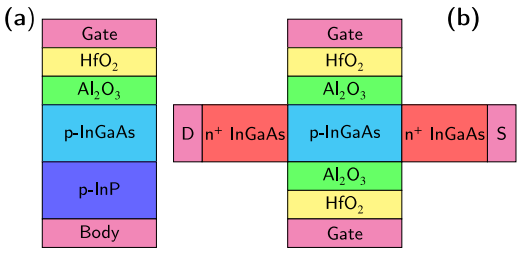

Fig. 2. 2D TCAD structures of (a) MOSCAP structure and (b) nanosheet MOSFET (not to scale).

Table 1
Geometrical parameters and doping concentration of the investigated structures.

MOSCAP		Nanosheet	
t_{InP}	50 nm	t_{sh}	43 nm
t_{InGaAs}	30 nm	W	140 nm
Area	100 × 100 μm^2	Lg	150 nm
t_{Al2O3}	0.8 nm	t_{Al2O3}	0.8 nm
t_{HfO2}	3 nm	t_{HfO2}	2.25 nm
Na_{InGaAs}	5 ·10^{16} cm^{-3}	Na_{ch}	5 · 10^{16} cm^{-3}
Na_{InP}	10^{18} cm^{-3}	$Nd_{S,D}$	8.6 · 10^{18} cm^{-3}

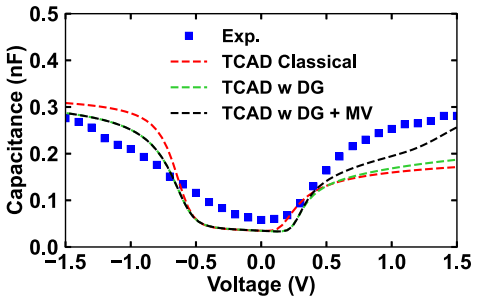

Fig. 3. Simulated C–V curves of the MOSCAP with different physical models, compared with experiments at 10 kHz. The fully classical approach is compared with the density-gradient (DG) and the density-gradient and multi-valley (DG+MV). Symbols: Experiments. Lines: TCAD simulations.

vapor deposition (MOCVD). Following surface cleaning with ammonium sulfide (NH4)2S, the sample was immediately transferred to the atomic layer deposition chamber for sequential deposition of thermal Al_2O_3, HfO_2, and in-situ titanium nitride (TiN). After ALD, physical vapor deposition (PVD) of TiN and the subsequent definition of the top metal pad and back contact pad were carried out via a lift-off process. The nanosheet devices followed a similar fabrication process, with the addition of source/drain (S/D) ion implantation using silicon at a dose of 1×10^{14} cm^{-2} and an energy of 15 keV. After fin formation by inductively coupled plasma (ICP) etching, the InP sacrificial layer was selectively wet etched using a HCl solution to release the suspended InGaAs channel layer. Following nanosheet formation, the gate stack was deposited by ALD and the contact pads were defined. The geometrical parameters and the doping concentrations for both structures are listed in Table 1. A Keysight B1500 A semiconductor parameter analyzer, equipped with multi-frequency capacitance measurement units (CMU) and source measurement units (SMU), was used to extract both the AC and DC characteristics of the devices.

3. TCAD setup

Synopsys SDevice was used to extract the main features of the devices by adopting their corresponding 2D structures in order to balance computational efficiency and accuracy [11]. Geometries are large enough to make the transport effects on the lateral walls of the nanosheet MOSFET negligible. The TCAD 2D domains are reported in Fig. 2. They reproduce the gate-to-channel stack of the fabricated ones. The HfO_2 features a high dielectric constant ($\kappa = 22$), significantly higher than that of Al_2O_3 ($\kappa = 9$), which allows for the formation of a physically thicker dielectric layer while maintaining the same equivalent oxide thickness (EOT = 0.88 nm). This results in negligible gate leakage. The work function of the gate electrode was set to 4.5 eV, corresponding to the TiN metal contact, ranging from approximately 4.3 eV to 4.7 eV, depending on composition, purity and deposition method [12]. MOSCAP simulations of the small-signal AC regime are carried out adopting accurate physical models for the InGaAs (Fig. 3).

The drift–diffusion approach is used with the Fermi statistics. Quantum confinement effects are accounted for using the density gradient (DG) model with the correction parameter gamma (γ) fixed to 1.776, following [4]. A significant increase of the capacitance value at positive biases is observed by including also the multi-valley model (MV), as available in the Synopsys tool. MV accounts for the density of states including the two lowest-lying conduction band valleys (Γ and L) and incorporates the nonparabolicity of the band structure. A clear increase of the capacitance at positive biases is found in the C–V curve, with a larger capacitance induced by the charge density in the L valley at voltages larger than 1 V. The additional X valley is omitted as it was found to have negligible effects in the analyzed regimes. The band parameters were obtained from the literature [13]. By comparing the predicted C–V against experiments, the numerical predictions with negative gate-bulk voltage ($V_{gb} < 0$) show a sharper variation, which can be associated with donor-type D_{it} in the bandgap. Viceversa, for $V_{gb} > V_{th}$, with V_{th} the threshold voltage, TCAD C–V is smaller than the measured one, indicating the presence of acceptor-type D_{it} located in the conduction band [14].

4. Results and discussion

The D_{it} distribution is extracted by adding the trap contributions in the TCAD setup so to fit the C–V experiments. A table-based implementation of the D_{it} is adopted, which can be used to add donor or acceptor traps at specific energies located in the gap and in the conduction band of the InGaAs/Al_2O_3 interface. Their contribution in the generation–recombination term is accounted for consistently along with the Shockley–Read–Hall (SRH) term for the bulk material [11]. The value for the interface-trap cross-section is fixed to the default one as it is in accordance with the experiments in [8] and no relevant sensitivity was further observed. Fig. 4 shows the full set of the extracted D_{it}. The adoption of the donor-type traps in the gap allows for a nice prediction of the C–V curves with $V_{gb} < 0$. For $V_{gb} > V_{th}$, a density of acceptor traps is implemented in the conduction band as discussed in [14]: the extracted distribution quantitatively represents the experimental curves. It is worth pointing out that the frequency dependence is mostly due to the role of the bulk SRH term. The lifetime parameter τ in the SRH model is fixed to 1.6 × 10^{-14} s, which can be ascribed to high defect density. The extracted trap density is similar or lower than those reported in previous works [8,14]. A nice

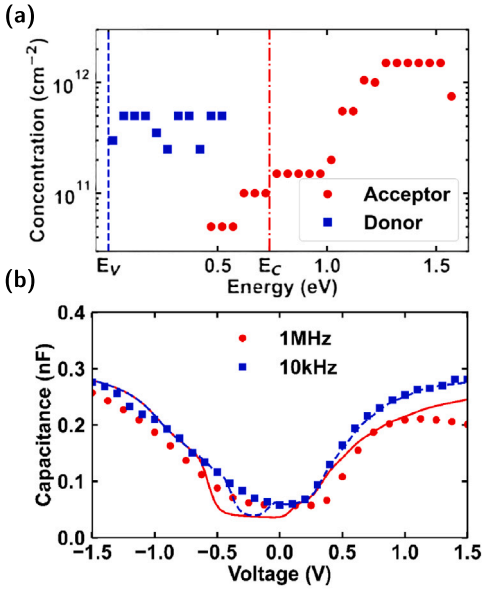

Fig. 4. (a) Extracted D_{it} as implemented in the TCAD simulator: vertical lines at E_V and E_C correspond to the valence and conduction band edges, respectively. (b) Experimental and simulated C–V curves of the MOSCAP for two different values of the small-signal frequency. Symbols: Experiments. Lines: TCAD simulations carried out by incorporating the extracted D_{it}.

Table 2
TCAD mobility parameters of the InGaAs nanosheet device.

Parameter	Value	Units
μ_b	400	cm^2/V s
B	$3.11 \cdot 10^8$	cm/s
δ	$6.11 \cdot 10^{18}$	cm^2/V s
A	3	1
β	2.7	1
v_{sat}	$8.9 \cdot 10^6$	cm/s

agreement is obtained on the whole bias range (Fig. 4, bottom), the slight discrepancy in the intermediate region (depletion regime) could be attributed to the absence of additional bulk traps in the InGaAs.

The obtained D_{it} is implemented in the simulation setup for the nanosheet MOSFET. The additional calibration of transport models is carried out by fitting the corresponding current–voltage experiments. Specifically, electron tunneling through the gate oxide stack is considered as the primary mechanism contributing to the drain current (I_d) in off state. The electron tunneling mass is set to 0.32 m_0 by fitting I_d at negative gate–source biases ($V_{gs} < 0$) with large drain–source voltage ($V_{ds} = 0.5$ V) (Fig. 5(a)). The sub-threshold slope is nicely reproduced by the implemented interface-trap density, confirming the validity of the proposed extraction. The low-field mobility model incorporates the Masetti formulation for the doping dependence and the Lombardi model for the combination of bulk mobility with surface phonon and surface roughness scattering mechanisms [11]. The effective low-field mobility was carefully fitted against the $I_d - V_{gs}$ at $V_{ds} = 0.05$ V. The resulting bulk mobility (μ_b in Table 2) is relatively low, but is consistent with previous studies, where the reduced mobility has been attributed to degradation of the Al_2O_3/InGaAs interface properties [15] in addition to high-κ remote Coulomb scattering effects [16]. To account for high-field velocity saturation effects, the Canali model is also integrated. The effective saturation velocity is fixed to the value extracted by delay-time analyses [6]. The nice agreement of the simulated $I_d - V_{ds}$ curves with the experiments validates the overall model (Fig. 5(b)).

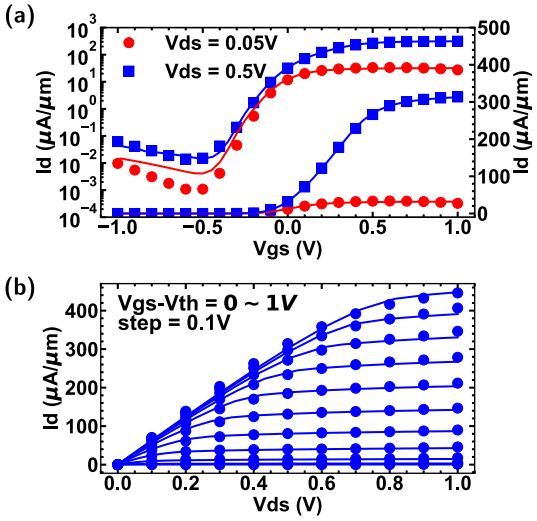

Fig. 5. Comparison between experimental and simulated (a) $I_d - V_{gs}$ and (b) $I_d - V_{ds}$ curves of the nanosheet MOSFET. Symbols: Experiments. Lines: TCAD simulations.

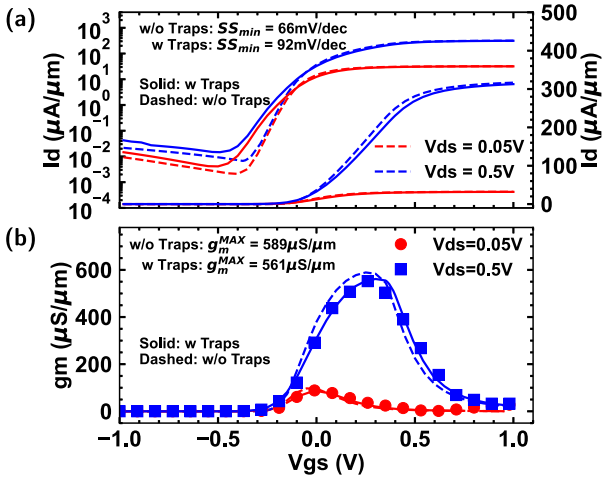

Fig. 6. Simulated Id-Vg curves of the nanosheet MOSFET with and without interface traps, highlighting (a) the subthreshold swing (SS) and (b) the transconductance.

The mobility parameters used for calibration are provided in Table 2. Default parameters for InGaAs are used for parameters not reported in the Table.

In Fig. 6(a), the simulated $I_d - V_{gs}$ curves are compared with those of a transistor with the same mobility parameters but no traps at the Al_2O_3/InGaAs interface. It can be observed that the performance degradation in the subthreshold slope can be mostly attributed to trapping effects. In the figure, the minimum values of the SS for V_{ds} = 0.5 V are reported. SS_{min} is 66 mV/dec without interface traps (close to the ideal SS) and 92 mV/dec with interface traps, corresponding to 39% degradation. In addition, the average SS values at V_{ds}=0.5 V are extracted, showing 70 mV/dec without interface traps and 97 mV/dec with interface traps, again reflecting the same amount of degradation. The average values are extracted over a V_{gs} window from −0.3 V to −0.2 V in the ideal case, and from −0.35 V to −0.25 V in the case with interface traps to account for the threshold voltage shift. In Fig. 6(b), it is also shown that the maximum transconductance (g_m^{MAX}) degrades with interface traps of about 5%. This limited effect might be due to

the adopted mobility model, which is kept constant in the two cases: as explained above, the resulting μ_b value simply includes interface-trap and remote Coulomb scattering effects by fitting the I–V curves without assuming a specific model for such contributions.

5. Conclusions

In this work, InGaAs based nanosheet transistors have been fabricated and characterized to investigate the impact of interface traps on device performance. By performing TCAD simulations it has been possible to understand that the subthreshold slope degrades of about 39% due to traps at the oxide/semiconductor interface, and effective mobility is limited to 400 cm^2/Vs. This implies that the intrinsic potential of InGaAs-based nanosheets has not yet been fully exploited if compared to the fin-based MOSFETs, primarily due to the immaturity of the current fabrication technology which limits the effective electron velocity. The choice of the best high-κ stack is still under analysis along with improved post-deposition annealing treatments. Although these devices require further optimization, they hold strong promise as viable candidates for next-generation applications in the post-CMOS era.

CRediT authorship contribution statement

Luigi Balestra: Writing – review & editing, Writing – original draft, Supervision, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Simone Di Stasi:** Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Elena Gnani:** Project administration. **Susanna Reggiani:** Writing – review & editing, Validation, Supervision, Project administration, Funding acquisition. **Mu-Yu Chen:** Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Hiroshi Iwai:** Supervision, Project administration, Investigation, Funding acquisition. **Edward Yi Chang:** Supervision, Project administration, Investigation, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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