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A −8 mV/+15 mV Double Polarity Piezoelectric Transformer-Based Step-up Oscillator for Energy Harvesting Applications

Antonio Camarda, Marco Tartagni, *Member*, *IEEE*, and Aldo Romani

***Abstract*—This work presents two circuit topologies of battery-less integrated boost oscillators suitable for kick-starting electronic systems in fully discharged states with ultra-low input voltages, in the context of energy harvesting applications based on thermoelectric generators, by coupling a piezoelectric transformer in a feedback loop. With respect to prior work, the first presented solution is a double polarity integrated circuit designed in a 0.18 µm CMOS technology able to boost ultra-low positive and negative voltages without the need of switching matrixes. The circuit exploits a CMOS inverter made up of low threshold transistors, and also includes a hysteretic voltage monitor consuming only ~15 nW to enable an external circuit. The minimum achieved positive and negative oscillation voltages are +15 mV and −8 mV, which to the best of the authors' knowledge, are among the lowest start-up voltages achieved in literature up to now without using magnetic components. Moreover, the input impedance in the range of several kΩ makes the presented solution suitable also for high impedances sources such as rectennas. The second presented circuit, designed in a 0.32 µm CMOS technology, exploits an input stage based on depletion-mode MOSFETs in a common source stage configuration and achieves high-step ratios up to ~60.**

***Index Terms*— boost circuit, bootstrap circuit, double polarity, energy harvesting, oscillator, piezoelectric transformer, rectenna, thermoelectric generator, voltage monitor**

I. Introduction

Wireless Sensors Networks (WSN) are groups of widespread sensors communicating between each other through wireless channels. They have the duty of collecting, transmitting and storing spatially distributed data about several environmental physical quantities such as temperature, humidity or air-pressure. Battery-powered WSN generally use a certain amount of energy for collecting and sending data to the central unit (few nJ/bit) [1]. The consumed power can be reduced by implementing architectures exploiting specific blocks such as wake-up radios or by reducing the overall duty-cycle of operation (i.e., the duration of the on-state compared to sleep-mode) of the network of sensors [2].

In any case, lifetime is one of the most important and critical aspects of energy autonomous systems. Technology scaling has played its role by reducing circuits dimensions and thus making systems less power-demanding. Nevertheless, this is not sufficient, given that relying on batteries is not the optimal solution because their replacement can require very high maintenance costs. In order to achieve fully energy autonomous systems, it is possible to conceive battery-less systems that convert in an electric form the harvested energy available in the environment in several forms such as sunlight, wind, heat, vibrations or RF [3] [4] [5] [6]. However, environmental energy sources often provide extremely low voltages, whereas switched-mode boost converters or charge pumps might require a higher minimum input voltage typically in the order of the threshold voltage of the used transistors in order to produce a usable supply voltage for a WSN. To cite an example, photovoltaic cells (PVCs) provide different output power levels depending on the illumination conditions which may vary in the range of two orders of magnitude [7], and the provided output voltage can be as low as ~200 mV in low illumination conditions. Radio Frequency (RF) signals can also be exploited to provide power to passive devices, as is the case in radio frequency identification (RFID) tags. However, the distance of power transmission typically is limited to several meters [8], and at such high distances the amplitude of the received voltage of rectennas (i.e. rectifying antennas) can be as low as ~100-200 mV. Moreover, in order to extract power, temperature gradients can be exploited as well by means of thermoelectric generators (TEGs) based on the Seebeck effect (Fig. 1): when two different metals are electrically connected and subject to a temperature gradient, a voltage difference arises at the terminals of the connection. The electrical series-connection and the thermal parallel connection of such thermocouples increases the output voltage at the expenses of a higher output resistance. The size of these devices is in the order of few cm^2 with output voltages around 10-50 mV/°C and output resistances as low as ~0.4 Ω [9].

This paragraph of the first footnote will contain the date on which you submitted your paper for review. It will also contain support information, including sponsor and financial support acknowledgment. For example, "This work was supported in part by the U.S. Department of Commerce under Grant BS123456".

A. Camarda, M. Tartagni and A. Romani are with the Department of Electronics Engineering and Information Technology of the University of Bologna, Cesena Campus, 47521 Cesena (FC) - Italy. (e-mail: antonio.camarda@unibo.it, marco.tartagni@unibo.it, aldo.romani@unibo.it).

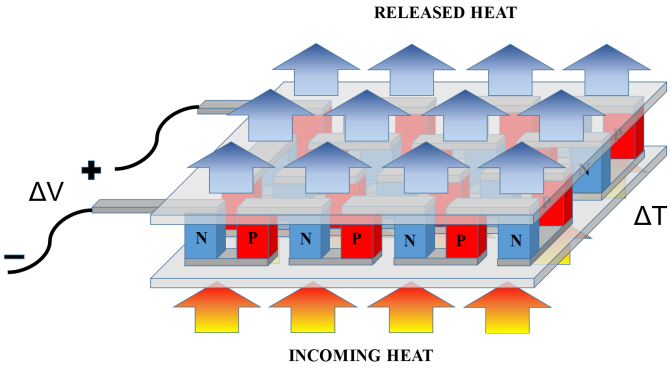

Fig. 1: Representation of a TEG. An array of electrically series-connected and thermally parallel-connected thermocouples outputs a voltage proportional to the temperature difference.

In most cases, the output voltage of the aforementioned transducers is not sufficient to overcome the threshold voltage V_{TH} of the power devices in a conventional boost power converter or charge pump. Then, in energy harvesting (EH) systems (Fig. 2), since the main power converter requires a minimum supply voltage, it can be activated only once a storage element (e.g. a capacitor) has been charged to this level by a separate kick-start voltage booster circuit. The kick-start voltage booster is a circuit able to function at very low voltages levels down to few tens of mV by exploiting normally-ON transistors such as JFETs or depletion-mode MOSFETs (DeplMOS). The main purpose of such circuit is the charge of the storage capacitor to a voltage level sufficient to provide the minimum supply voltage for a conventional power converter to perform the power conversion.

The problem of kick-starting from ultra-low voltages down to few tens of mV has been extensively addressed in literature. The first approach was presented by Damaschke in 1997 [10] and is depicted in Fig. 3. The Ultra-Low Voltage Source (ULVS) is modeled through a voltage V_{IN} with an output resistance R_S. A normally-ON transistor (M_1, DeplMOS or JFET), coupled with a Magnetic Transformer (MT), is required to provide an overall negative resistance in parallel to the LC tank, made by the secondary inductance and the equivalent capacitance C_G seen at the gate of the transistor M_1, when V_{IN} does not exceed few tens/hundreds mV. The positive feedback due to the MT thus produces an oscillation which is then rectified through the Voltage Doubler (VD) made by C_{PUMP}, the diodes D_1 and D_2 and the storage capacitor C_{STORE}. The minimum input voltage $V_{IN,MIN}$ to achieve oscillation is dependent from the transformer turn-ratio N and the losses in the MT [11]. This particular topology has been adopted for RF harvesting purposes [12] and in commercial products operating from 20 mV with a 1:100 MT [13]. The cascade-connection of several MTs allows to reduce the minimum voltage to trigger an oscillation down to ~7 mV, at the expenses of system compactness [14].

Other ultra-low voltage systems were presented in literature, but an initial voltage (e.g. provided by an external energy source or by a battery) of several hundreds of mV is necessary [15] [16].

A minimum input voltage of 35 mV was achieved through

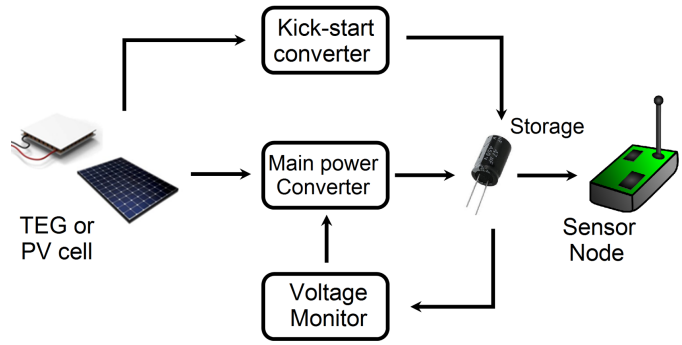

Fig. 2: Diagram of an energy autonomous system based on energy harvesting. A kick-start boost converter provides the initial voltage and energy required to turn on a more efficient power converter.

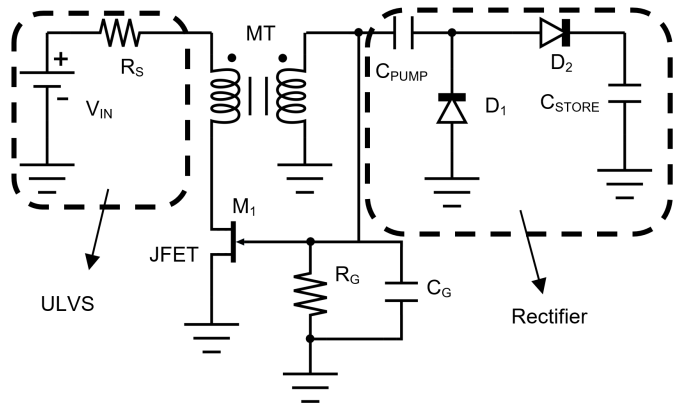

Fig. 3: Schematic of the conventional Armstrong oscillator with output rectification.

exploitation of a motion-activated switch [17]. Furthermore, input voltages down to 10 mV were also recently achieved [18] [19], but the kick-start is aided by means of a 32-stages Dickson charge pump boosting the output of a secondary harvester providing a much higher voltage (rectenna).

Other solutions are related to the design of specific integrated circuits (ICs) exploiting Forward Body Biasing (FBB) techniques [20], which aim at reducing the threshold voltage of transistors in a charge pump. Such technique allows to lower the start-up voltage down to 0.18 V. However, the main drawback is the higher leakage currents that degrade the whole efficiency of the converter. Dynamic Body Biasing (DBB) techniques [21] represent an improvement with respect to FBB, however both FBB and DBB require deep wells in the process in order to have a floating body connection.

Another technique with the purpose of starting from voltages lower than the normal threshold voltage of transistors consists in tuning the V_{TH} of the transistors at the end of the fabrication step. This technique [22] was applied to the p-channel MOS transistors (pMOS) placed in a ring oscillator providing the clock signal for a conventional Dickson charge-pump (DCP) and achieved 95 mV operation. This technique essentially provides additional fixed charge in the transistors' gate dielectrics fixing the V_{TH}. Among other types of low-voltage circuits, a battery-less integrated harvesting system with minimum voltage of 50 mV was recently presented [23], in which the oscillation is achieved through a cross-coupled nMOS LC oscillator exploiting the high Q-factor of a commercial inductor. Moreover, an ultra-low

quiescent power boost converter for sources down to 70 mV is presented in [24]: the quiescent power is lowered down to 544 pW with a peak power conversion efficiency of about 56%. However, it still relies on magnetic components and requires the injection of extra energy for kick-starting. A reconfigurable buck/boost converter suitable for solar-cells is presented in [25]. The quiescent power consumption is as low as 3 nW but the minimum start-up voltage is ~140 mV. It is worth remarking that the efficiency as well as the minimum activation voltage of such systems generally depend on the "quality" of magnetic components, whose scaling poses several constraints during the design phase [26]. In [27], an ultra-low voltage of 21 mV, with minimum input power of 5.8 µW and efficiency higher than 70% is achieved, exploiting 1:1 MTs. However, such values are achieved with 10 mH coils.

Piezoelectric transformers (PTs) are highly efficient power conversion devices that are generally used for high voltage applications such as Cold Cathode Fluorescent Lamps (CCFL) [28] [29] or highly efficient resonant converters [30] [31]. Nevertheless, their use in ultra-low voltage applications has been demonstrated: a novel start-up approach based on the use of PTs instead of MTs has been recently presented [32]-[34]. Such bootstrap circuit was successfully adopted for kick-starting a fixed-frequency boost converter, from a fully discharged state, performing a power conversion from a TEG with efficiencies around more than 40% in the range 30-50 mV [35]. However, such systems work only with positive voltages. It is worth remarking that PTs in a feedback loop for oscillation boosting purposes were also previously reported [36], however the PT in [36] works close the resonance frequency and the circuit is a Pierce-type oscillator that requires an inductor to achieve oscillation. Differently, in [32] [33] the PT works close to its parallel resonance (or anti-resonance) frequency and magnetic components are not necessary to trigger an oscillation.

A first contribution of this work is a new double-polarity circuit topology of integrated boost oscillator designed and fabricated in a UMC 0.18 µm CMOS technology, able to boost positive and negative voltages without the necessity of switching the polarity of the input voltage through switching matrixes [37]. The circuit achieves a minimum positive start-up voltage of 15 mV by exploiting PTs in a feedback loop. When polarized by a negative voltage, the circuit is able to oscillate at −8 mV. To the best of the authors' knowledge, these are among the lowest values reported in literature without magnetic components and without any battery or external energy contributions. The output voltage with a ±15 mV input is around 150 mV, achieved with a rectifying VD; however, higher voltages can be obtained through use of voltage multipliers or conventional multi-stage charge pumps. With respect to prior work [33], the input stage is based on a CMOS inverter gate made up of low-threshold native MOSFETs (low-V_{TH} or NatMOS) rather than a common source (CS) stage. One of the main advantages is that NatMOS are generally more common in ICs with respect to JFETs or DeplMOS. This solution, based on CMOS inverter input stage, differently from [33], integrates also a nano-power hysteretic voltage monitor (VM) sinking only ~9 nA at 1.6 V. The aim of such VM is to connect a load R_{LOAD} to C_{STORE1} when $V_{STORE1} > V_H$, and to disconnect such load when $V_{STORE1} < V_L$, with V_H and V_L the switching thresholds of the VM.

Moreover, the circuit presented in prior work [33] is suitable only for low input impedances sources such as TEGs, whereas another relevant feature of the CMOS inverter-based circuit is the capability to work with high impedances sources in the range of several kΩ such as rectennas.

An additional contribution of this work is an improved integrated version of the circuit shown in [33], based on DeplMOS rather than JFETs and implemented in a STMicroelectronics 0.32 µm CMOS process. This circuit is able to self-start from voltages as low as 31 mV and to provide an output voltage of 5 V, with a maximum step-up ratio of ~60. The minimum voltage is comparable to that reported in [33], but in this specific case, no magnetic component was used, given that the main purpose of the research is to avoid the insertion of any magnetic components. Moreover, through the exploitation of a higher Q-factor PT, with respect to [33], it was possible to modulate the voltage gain of the system in order to improve further the performances.

The presented boost oscillators are not intended as stand-alone converters because of their poor efficiency. As shown in Fig. 2, their duty is to kick-start an energy autonomous system from a fully discharged state and to enable a more efficient power converter, once a sufficient voltage is achieved on the storage element. In fact, the presented circuits do not aim at extracting the maximum power from the TEG, which is the target of the main boost converter, but rather at working in proximity of the open circuit output voltage to reduce voltage drops that would compromise the gain of the amplifier stage, so as to minimize the operating voltage. Fig. 4 depicts the numerically simulated I-V (current-voltage), I-P (current-power), R-P (resistance-power) and R-V (resistance-voltage) characteristics of a TEG providing 100 mV in open circuit with an internal resistance $R_S = 10\ \Omega$. In order to operate in the maximum power point (MPP), the boost oscillator should draw a current causing the output voltage of the TEG to be equal to half of its open-circuit voltage. However, in this condition, if the boost oscillator has a minimum operating voltage $V_{IN,\mathrm{MIN}}$, the TEG should provide an open circuit voltage equal to $2 \cdot V_{IN,\mathrm{MIN}}$,. Hence, for these converters, the MPP operation is in contrast with the purpose of lowering the minimum activation voltage. On the other hand, biasing the TEG close to its open-circuit voltage will reduce the extracted power but will also ensure a higher voltage for supplying the kick-start converter.

The paper is organized as follows: Section I introduces the work, Section II presents the circuits, Section III deals with experimental validation, and Section IV concludes the paper.

II. Description of step-up oscillators

A. The PT

Table I reports the electromechanical parameters of the Rosen-type PT used in our work, provided by Noliac (Fig. 5).

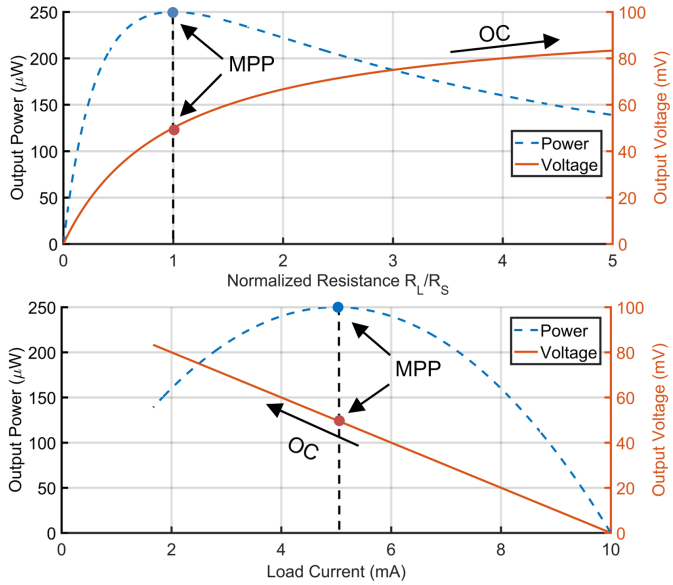

Fig. 4: Characteristics R-V, R-P, I-P and I-V of a TEG providing 100 mV in open circuit with a series resistance of 10Ω.

TABLE I
ELECTRO-MECHANICAL PARAMETERS OF THE TWO-PORTS BUTTERWORTH-VAN DYKE NETWORK OF THE ADOPTED SAMPLE.

Mode	C_{IN} (nF)	L_M (μH)	R_M (Ω)	C_M (nF)	N	C_{OUT} (pF)	f_s (kHz)	f_p (kHz)
1	136.65	635	0.21	14.7	55.6	17.35	58.8	61.23
2	136.65	220.8	1.14	11.2	58.3	17.35	110.4	114.14

C_{IN} and C_{OUT} are the PT input and output capacitance respectively. The electromechanical transduction is modeled through the branch composed by the inductance L_M, the capacitor C_M, and the resistance R_M. The factor N represents the stress-ratio from input to output (the equivalent of the turns-ratio of a MT). Additional details concerning the modeling and behavior of PTs, can be found in [38]-[40].

The voltage transfer function of a PT is that of a two-poles system with extremely high-quality factor (Q-factor) [33]:

$$A_{V,PT}(s) = \frac{C_{M2}\omega_S^2}{NC_{OUT}\left(s^2 + \frac{\omega_s s}{Q} + \omega_S^2\right)}, \quad (1)$$

where $C_{M2} = C_M \cdot N^2 C_O/(C_M \cdot N^2 C_O)$ is the open-circuit mechanical capacitance, $Q=\omega_s \cdot L_M / R_M$ is the quality factor and $\omega_s = (L_M \cdot C_{M2})^{-1/2}$ is the resonance pulsation. The resonance frequency can be defined as: $f_s = \omega_s / 2\pi$. C_O is the equivalent capacitance seen at the output capacitance, that is $C_O = C_{OUT} + C_{VD} + C_G$; C_{VD} accounts for the capacitive load effect of the VD around 0 V (due to the ultra-low voltage in input, the DC level of several nodes can be safely approximated to ground), whereas C_G is the capacitive load effect of the CS or the CMOS inverter.

As explained later, for CS-based step-up oscillators, it is possible to put an additional capacitance C_{OPT} in parallel to C_{IN}. In this case, we define $C_{IN2}=C_{IN}+C_{OPT}$. The anti-resonance frequency f_p of the PT can be expressed as:

$$f_p = \frac{\omega_p}{2\pi} = 2\pi\left(L_M \frac{C_{M2} \cdot C_{IN2}}{C_{M2} + C_{IN2}}\right)^{-1} \quad (2)$$

The values of both f_s and f_p for the PT used in our work are reported in Table I. At both f_s and f_p the input impedance of a PT is approximately real, with the only difference that at f_s the impedance is at its minimum, whereas at f_p is at its maximum. Between f_s and f_p, the input impedance is inductive, whereas for frequencies much lower than f_s and much higher than f_p, such impedance is capacitive and dominated by C_{IN} [33].

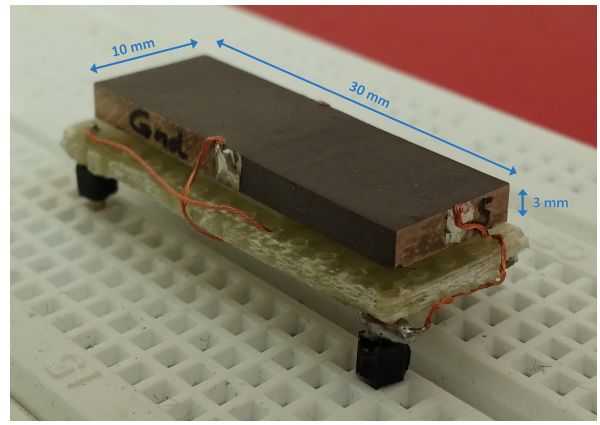

Fig. 5: The PT prototype used in this experiment.

B. Step-up oscillator with CMOS inverter as input stage and output voltage monitor

Fig. 6 depicts the schematic of the proposed step-up oscillator for ULV sources. Due to its capacitive behavior in DC, the PT has to be connected in parallel with the input inverting stage. Differently, if the PT is replaced with a MT in the circuit in Fig. 6, the connection node between M_1 and M_2 (M_INV output) would be shorted to ground and the circuit does not oscillate. The ULVS (TEG/rectenna) is represented by an equivalent voltage source V_{IN} and a series resistance R_S.

The mode of operation of the feedback loop is similar as the circuit presented in [33]. In this specific case, the CS is replaced by a CMOS inverter (M_INV) made up by complementary NatMOS transistors. A voltage monitor (VM) is connected to the storage capacitor C_{STORE1} of 4.7 μF. The purpose of the hysteretic VM is to connect a load R_{LOAD} to C_{STORE1} when a certain voltage V_H is sensed across C_{STORE1}, and to disconnect such load when V_{STORE1} becomes lower than a threshold $V_L < V_H$. C_{PUMP} is an external capacitor of 200 pF. The second load capacitor C_{STORE2} was set to 100 nF. The resistor R_P (~10MΩ, placed off-chip) placed between the input and output of M_INV is necessary to correctly polarize the stage in its high-gain region, as it is done in Pierce-type oscillators. The three series pn diodes D_A, D_B and D_C connected at the gate of M_1 have the function of clamping voltages higher than the maximum gate-source voltage V_{GS} (1.8 V) allowed by the input transistors. The D_{ESD} diode clamps the negative peak of the oscillation at ~−0.5 V, hence the oscillation will have a positive DC offset. If D_{ESD} is replaced by three series diodes with same polarity, oscillating voltage would have ~0 V DC offset. It is possible to produce an oscillation with a negative DC offset as well, by replacing D_A, D_B and D_C with a single diode and by replacing D_{ESD} with three series-connected diodes with the same polarity of D_{ESD}. The size of both M_1 and M_2 is W/L=4166, M_1 and M_2 have an interdigitated layout, with W and L being the width and channel length respectively.

At the beginning of the oscillation, a small-signal analysis can be applied by linearizing the circuit around the bias point

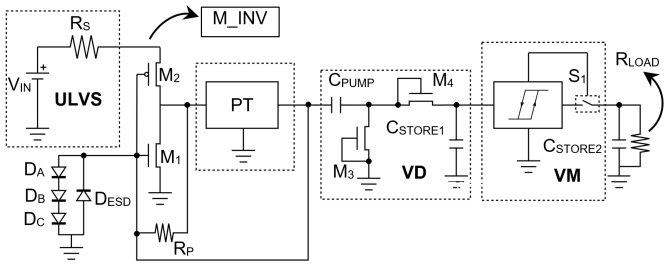

Fig. 6: Schematic of the PT-based step-up oscillator with a CMOS inverter as input stage and an integrated voltage monitor (VM).

$V_{IN}/2$ is the stage is designed to be symmetric with respect to V_{IN}. In this case, the voltage gain of the CMOS inverter is given by:

$$A_{V,INV}\left(V_{IN}\right) \cong -\left(g_{m,n}+g_{m,p}\right)\cdot\left(r_{out,n}//r_{out,p}\right), \qquad (3)$$

where $g_{m.n}$ and $g_{m.p}$ are the transconductances of the nMOS and pMOS respectively, whereas $r_{out.n}$ and $r_{out.p}$ are the output resistances of the transistors. The operator "//" corresponds to the parallel combination of two resistances (e.g. $R_A // R_B = (R_A^{-1}+ R_B^{-1})^{-1}$. It is worth remarking that while the DeplMOS or JFETs in the CS stage work in the triode region above threshold [33], the low threshold devices in the CMOS inverter work in deep subthreshold region, given that the gate-to-source voltage does not exceed few tens of mV, whereas the threshold voltage is considerably higher. Furthermore, in the subthreshold region the transconductance has an exponential behavior with respect to the gate-source voltage, rather than the conventional linear dependence. In the CMOS inverter, the devices work in subthreshold region, where the current is due to diffusion effects rather than drift effects (as in above-threshold conditions). This implies that the g_m depends almost linearly on V_{IN} for $V_{IN}<n\cdot V_t$, where $V_t=kT/q$ is the thermal voltage (~26 mV) and n is a number depending on the channel length; differently the dependence of g_m on V_{IN} is much lower when $V_{IN}>n\cdot V_t$, because all the electrons diffusing from source are collected at the drain. By means of Spice simulations, we found that $n\cdot kT/q\approx 50$ mV, hence we expect a maximum of the voltage step-up ratio around 50 mV.

One of the most important advantages of a CMOS inverter stage compared to the conventional CS stage reported in [33], is that both transistors contribute to the voltage gain through their g_m. Fig. 7 shows a picture of the fabricated die. The size of the presented boost oscillator, is 260 µm × 170 µm.

Assuming that all blocks in Fig. 6 are unidirectional, then the return-ratio is a safe approximation of the loop gain.
In order to find the loop gain $T(s)$, it is necessary to find the voltage gains of the stages involved in the loop as well as the load effects.

As explained in [33], due to its high Q-factor, at a frequency extremely close to f_P the PT provides approximately π radians of phase shift, which combined with the additional π radians provided by the inverting input CMOS inverter stage, determine an overall phase shift of roughly 2π. This necessary (but not sufficient) condition is required by the Barkhausen phase criterion to achieve oscillation. Thus, it can be safely stated that the presented system oscillates at a frequency

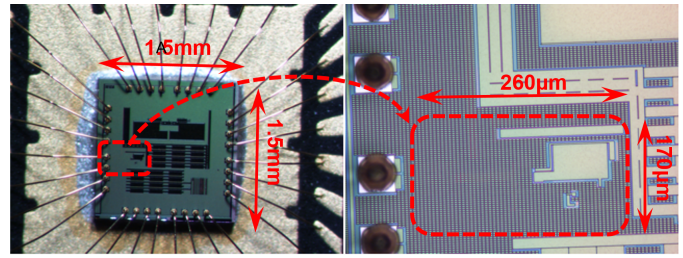

Fig. 7: Picture of chip designed in 180nm CMOS.

$f_{OSC}=\omega_{OSC}/2\pi$ extremely close to f_P if a sufficient loop gain is provided (Barkhausen gain criterion).

If a PT is able to vibrate at different modes, the prediction of the vibration mode from an AC linear analysis is not possible if the Barkhausen criteria are satisfied in more than a single frequency. As explained in [33], if the modes are separated by a factor two, as it happens in this case, the oscillation might start at the first mode, but the nonlinearities of the circuit will shift the oscillation to the second mode. Generally, when the Barkhausen criteria are satisfied in more than a frequency, the oscillation mode is conditioned by the shape of the non-linearity of the circuit. To cite an example, an abrupt saturation excited by a sinusoid of frequency f_0 produces a square-wave with only odd higher-order harmonics ($3\cdot f_0$, $5\cdot f_0$, $7\cdot f_0$ etc.). Such kind of non-linearity cannot excite the mode of the PT placed at $2\cdot f_0$. To cite another example, the absolute value function instead, produces a DC component plus even harmonics of the fundamental mode ($2\cdot f_0$, $4\cdot f_0$, $6\cdot f_0$ etc.). In order to predict the oscillation mode, when the Barkhausen criteria are satisfied in more than one frequency, a large-signal analysis is required. However, this goes beyond the scopes of the paper.

Equation (1) with the substitution $s = j2\pi f$, evaluated at $f = f_P$, assumes the form [32]:

$$A_{V,PT}\left(f_p\right) \cong -C_{IN2}/N\cdot C_O. \qquad (4)$$

Equation (4) suggests that the PT voltage gain at the anti-resonance frequency is independent from the Q-factor, in a first approximation.

The input impedance of the PT at $f = f_P$ is equal to [33]:

$$Z_{IN,PT}\left(f_p\right) \cong \frac{L_M C_{M2}}{R_M\left(C_{M2}+C_{IN2}\right)C_{IN2}} \cong R_M\left(\frac{QC_{M2}}{C_{IN2}}\right)^2. \qquad (5)$$

From (5) we see that $Z_{IN,PT}$ is inversely proportional to R_M or directly proportional to Q.

In order to determine the loop gain, it is necessary to assess the load effect of the PT on the M_INV stage. This is equal to:

$$A_{V,L}\left(f_p\right) \triangleq \frac{Z_{IN,PT}\left(f_p\right)}{Z_{IN,PT}\left(f_p\right)+r_{out,INV}}. \qquad (6)$$

The loop gain T is then found by multiplying (3), (4) and (6), combined with (5). T is a monotonically increasing function of V_{IN}, hence there exists a minimum value of V_{IN}, $V_{IN,\min}$, which satisfies the Barkhausen gain criterion. The value of $V_{IN,\min}$ is found by solving the relation $|T(V_{IN,\min})=1$.

In this specific case, we modeled the system as a phase-shift oscillator, because the PT is a two-port linear system. Nevertheless, it can be modeled also as a negative resistance

quartz-based oscillator [41] [42], where the shunt capacitance of the quartz is missing. If the value of (6) is approximately equal to 1, then the circuit is better modeled by a phase-shift oscillator, because T does not depend on Q (and hence on R_M as in quartz-based Pierce oscillators); otherwise if $r_{out,INV} >> Z_{IN,PT}$, then the circuit is better modeled by a negative-resistance oscillator.

In Fig. 6, the VD is composed of two diode-connected n-channel MOSFETs M_3 and M_4 of W/L=80.

The full schematic of the hysteretic voltage monitor VM is depicted in Fig. 8, whereas Fig. 9 reports a circuit simulation of the VM in typical process conditions. The duty of such circuit is to connect an external load R_{LOAD} only when a sufficient voltage is available internally. The voltage level of V_{STORE1} is scaled through a non-linear voltage divider (composed by M_5, M_6 and M_7) and compared with the threshold of an inverter (INV in Fig. 8). In order to drain a negligible current from V_{STORE1} in the order of few nA, several hundreds of MΩ would be necessary and would require a very large area, or off-chip resistors. For this reason, diode-reverse-connected n-channel NatMOS were used instead in the aforementioned voltage divider. The NatMOS M_5 (W/L=20, M_6 (W/L=48) and M_7 (W/L=10) act like a voltage divider made by non-linear resistors of resistance R_5, R_6 and R_7 respectively. M_5, M_6 and M_7 have to be matched even if their body-source voltage is different, in order to have a better accuracy of the resistance ratios. We call V_{Z1} the gate (source) of transistor M_5, and V_{Z2} the gate (source) of M_6.

In Fig. 9 it is possible to note that the circuit switches at V_H= 1.55 V and V_L=1 V. The graph can be divided in four different phases: A, B, C and D. Let us assume that during the initial ramp-up of V_{STORE1} the voltage V_F = 0 V (phase A). This means that $V_{Z1} = V_{STORE1}$, given that M_8 is a pull-up transistor. However, $V_{Z2} = V_{Z1}$ since $R_7 >> R_6$, because M_6 is much larger than M_7 and the body effect of M_6 can be neglected at the beginning. Thus, we have:

$$V_{Z2} = \frac{R_{7A}}{R_{6A}+R_{7A}} V_{Z1} \cong \frac{R_{7A}}{R_{6A}+R_{7A}} V_{STORE1} \cong V_{STORE1} . \quad (7)$$

In (7) the subscript A indicates the first phase. We will use the symbol "¬" to indicate the logic NOT boolean operation.

According to (7), $V_A = \neg V_{Z2}$ is forced to ground and C_A (≅100 fF) is kept discharged. $V_B = \neg V_A$ follows V_{STORE1}, while $V_C = V_A$ is also low, hence the switch S_1 (M_{13} W/L=2000, M_{14} (W/L=2000) is open, and C_{STORE2} is disconnected from C_{STORE1}. The switch S_1 provides about 10 Ω of resistance when it is closed and driven by a controlling voltage of ~2 V.

When V_{STORE1} reaches 1.25 V (B phase) the body effect of M_6 is not anymore negligible, hence a voltage drop between the drain and source of M_6 occurs. By design, this leads to:

$$V_{Z2} = \frac{R_{7B}}{R_{6B}+R_{7B}} V_{Z1} \cong \frac{R_{7B}}{R_{6B}+R_{7B}} V_{STORE1} \cong 1.15\text{V} \quad (8)$$

where the subscript B refers to the values in this phase. Once again, we remark that R_6 and R_7 are non-linear resistances. At this point V_{Z2} saturates at about 1.2 V. By design, when V_{STORE1} reaches V_H = 1.55 V, the voltage difference $V_{STORE1} - V_{Z2}$ = 350 mV is sufficient to partially turn-on the

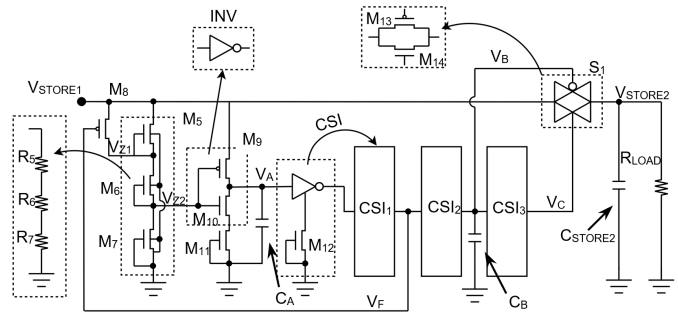

Fig. 8: Schematic of the integrated hysteretic Voltage Monitor.

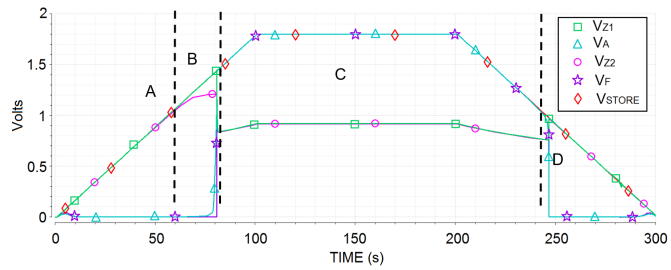

Fig. 9: Spice simulation of the hysteretic voltage monitor. The A, B, C, D phases were highlighted.

p-channel MOS transistor M_9 (W/L=7.35). The presence of M_{11} is necessary to unbalance the Current Starved Inverter (CSI) made by M_9, M_{10} (W/L=3) and M_{11} (W/L=1): the logic threshold of CSI_1 is shifted towards V_{STORE1}, as a matter of fact a voltage difference in the range of ≅ 350 mV is required to switch the inverter. At this point, C_A is charged at the current value of V_{STORE1} and so is V_F. Since V_F goes high, M_8 is turned-off, whereas S_1 closes and connects C_{STORE2} to V_{STORE1}.

Since M_8 is turned-off and since M_6 is much larger than M_5 and M_7, in the following phase (C) phase we have:

$$V_{Z2} \cong V_{Z1} = \frac{R_{7C}}{R_{6C}+R_{7C}+R_{5C}} V_{STORE1} \cong 840\text{mV} . \quad (9)$$

It is worth remarking that the relation linking V_{Z2}, V_{Z1} with V_{STORE1} is strictly non-linear. Nevertheless, both V_{Z1} and V_{Z2} follow the variations of V_{STORE1}.

In order to turn-off M_9 a lower value of V_{STORE1}, compared to the value V_H=1.55 V necessary to turn it on, is needed, given that the input of the inverter made by M_9, M_{10} and M_{11} (V_{Z2}) is now tied at a lower voltage level. By design, when V_{STORE1} reaches V_L = 1 V (phase D), then the circuit switches again and C_{STORE2} is detached from V_{STORE1}. In order to change the switching thresholds of the VM, it is necessary to act on the ratio between M_6 and M_7 for the high threshold V_H, and on the ratio between M_5 and M_7 for the lower threshold V_L. Acting on the dimensions of M_{11} is also possible.

As mentioned at the beginning of the paper, the value of $V_{IN,min}$ for this circuit are −8 mV and +15 mV. Fig. 10 depicts the spice simulation of the circuit showing the start-up for positive values of $V_{IN,min}$. A minimum value of 20 mV is necessary for oscillation with R_S= 0.4 Ω.

C. *Step-up oscillator with common-source amplifying stage*

Figure 11 depicts the schematic of the proposed step-up oscillator for ultra-low voltage (ULV) sources made by an input inverting CS stage coupled in a feedback loop with a PT, along with the picture of the die whose dimensions are

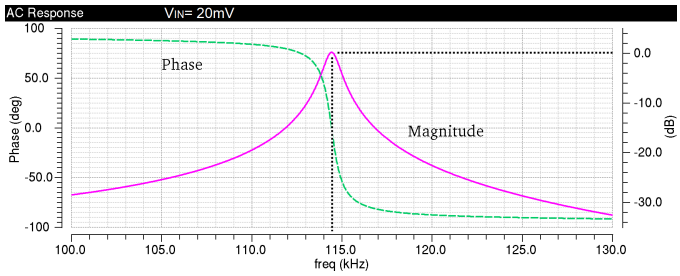

Fig. 10: Loop gain Bode-plots obtained through Spice simulation of the start-up circuit when polarized by a positive input voltage. $V_{IN,\min}$ is around 20 mV.

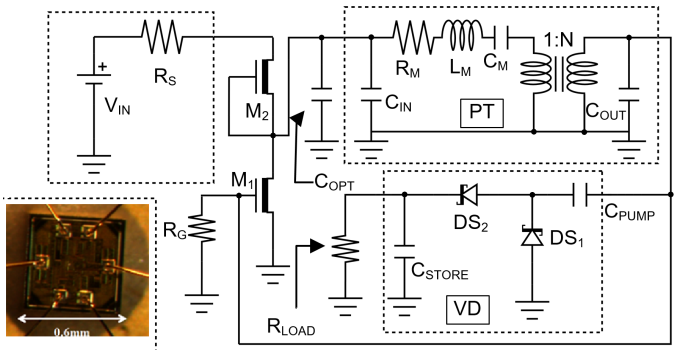

Fig. 11: Schematic of the PT-based boost oscillator with a common-source input stage. PT is the Piezoelectric Transformer, VD is the Voltage Doubler. The die also is shown.

600 µm × 600 µm including the pad frame. The circuit is an integrated version of the circuit based on discrete JFETs previously presented in [33], and is implemented in a STMicroelectronics 0.32 µm CMOS technology. Two DeplMOS build the input inverting CS stage, M_1 is the amplifier transistor and M_2 is the load transistor. In our specific case, M_1 and M_2 have equal sizes with an aspect ratio (W/L) = 150. Higher W/L ratios lead to higher transconductances while lowering the overall output resistance, hence (3) achieves saturation. However, bigger transistors increase the load capacitance at the PT output port, lowering the loop gain, given that the gate capacitance is proportional to W×L. C_{OPT} is a 400 nF capacitor necessary to further increase the loop gain, as explained in [33]. The VD rectifies and boosts the oscillation at the PT's output node $V_{OUT,PT}$. The diodes D_{S1} and D_{S2} in the VD are integrated Schottky diodes, whereas the resistance R_G (~140MΩ, placed off-chip) is used to provide a ~0 V polarization at the gate of M_1. The storage capacitor C_{STORE} is a 4.7 µF low-leakage polypropylene capacitor, whereas C_{PUMP} is a ~100 pF integrated capacitor. The resistor R_G must be high enough to not to provide noticeable load effects at the PT output node, given that PTs are very load-dependent devices [43], but at the same time it must be capable to polarize the gate around 0 V. Since PTs are very load dependent devices, R_G can be lowered down to 100 MΩ, without producing noticeable load effects at the PT's output port. Lower values can be used, but the value of $V_{IN,\min}$ increases accordingly.

By looking at (5) and (6), it is possible to note that a higher Q does not necessarily bring to a higher magnitude of T, because if $Q \to \infty$ then (6) asymptotically converges to 1, moreover the PT gain is independent on Q (see (4)). However, a higher Q PT gives the possibility to modulate $Z_{IN,PT}$, if $Z_{IN,PT} >> r_{OUT,CS}$ by inserting a capacitance C_{OPT} in parallel to the input port of the PT, increasing the value of (4), without affecting the value of (6). This is a main difference with respect to [33]: in our experiment, we used a PT with a Q almost double with respect to that used in [33]. As explained in [33] the value of $|T(s=j\omega_p)|$ can be expressed as:

$$|T(s=j\omega_p)| = k \cdot V_{IN} \cdot \frac{\alpha Q / C_{IN2}^2}{\alpha Q / C_{IN2}^2 + Z_1} \cdot C_{IN2}, \qquad (10)$$

where k, α are constants and Z_1 is the output impedance of the previous stage (the CS in this specific case). If $\alpha Q/C_{IN}^2 >> Z_1$, then $\partial T/\partial C_{IN2} > 0$, hence C_{IN2} can be increased up to the value $C_{IN2(MAX)} = \alpha Q/Z_1$. If $C_{IN2} > C_{IN2(MAX)}$, then $\partial T/\partial C_{IN2} < 0$: high Q-factors PTs, with low values of C_{IN} are necessary in order to modulate its input impedance and voltage gain, hence the maximum value of C_{OPT} is:

$$C_{OPT(MAX)} = C_{IN2(MAX)} - C_{IN} = \frac{\alpha Q}{Z_1} - C_{IN} \qquad (11)$$

Equations (3), (4), (5) and (6) can be used to model the behavior of the circuit, in which the differential parameters of M_INV have to be replaced with those of the CS in order to find the minimum input voltage to trigger an oscillation.

Considering the electromechanical parameters of the second mode reported in Table I, f_{OSC} is found to be 108.1 kHz, with an estimated $C_G + C_{VD}$ around 10 pF.

The inverting voltage gain of the CS stage can be written as:

$$A_{V,CS}(s) \cong -g_{m1} \cdot r_{out1} // r_{out2} = -k_1 \cdot V_{IN} \cdot r_{OUT,CS}, \qquad (12)$$

where $g_{m1} = -k_1 \cdot V_{IN}$ is the transconductance of M_1, the parameter k_1 (A/V^2) is the current gain factor of the transistor, $r_{OUT,CS} = r_{out1} // r_{out2}$ is the output resistance of the CS stage with r_{out1} and r_{out2} being the differential output resistances of M_1 and M_2 respectively. It is worth remarking that due to the very low voltages involved, the transistors are polarized in deep triode (linear) region. Since the devices are polarized in their linear region, the differential output resistance of each transistor equals the DC resistance seen from the source. The current drained from V_{IN} is equal to $V_{IN} / (r_{out1} + r_{out2})$, when the oscillation is about to start. If M_1 and M_2 have the same size, then we may safely state that $r_{out1} = r_{out2}$, hence the amplifying transistor M_1 is polarized with a voltage $V_{IN}/2$.

The main difference between the CS stage made by DeplMOS (or JFETs) and the CMOS inverter stage is that the gain of the CS stage is proportional to V_{IN}, for V_{IN} up to several hundreds of mV, because the transistors operate above V_{TH} whereas in the CMOS inverter stage, such linear dependence is hold for V_{IN} up to few tens of mV, because the transistors operate much below V_{TH} as explained before.

III. Experimental Results

Measurements were performed in order to test the performances of the proposed circuits and to validate the effectiveness of the proposed approaches.

A. Step-up oscillator with CMOS inverter as input stage and integrated voltage monitor

A TTi EL302T Power Supply was used to emulate the TEG.

A FLUKE45 digital Multimeter was used to measure the average current drawn by the circuit. In the ammeter configuration, at very low voltage levels down to few tens of mV, such ammeter presents about 12 Ω of series resistance R_S, more than one order of magnitude of some TEGs [44]. A Tektronix MSO 2024 Oscilloscope was used to visualize and sample the waveforms. Fig. 12 shows the schematic of the measurement set-up. A capacitor $C_P = 1.2$ µF supplies the AC current while keeping the input voltage of the Circuit Under Test (CUT) at a constant level. The average drawn current can be measured through the ammeter.

Fig. 13 depicts the measured unloaded DC transfer function of the main CMOS inverter of the boost oscillator made up by M_1 and M_2 (see Fig. 6). The inverter was designed to have the highest voltage gain around 0 V. The DC transfer function was obtained by applying in input a symmetric duty-cycle triangular waveform at 100 Hz of frequency with 15 mV of DC offset and 60 mV of peak-to-peak amplitude generated by a Keysight 33220A Function Generator. The supply voltage was set to 30 mV. The unloaded voltage gain of the stage is about –0.7 (V/V) around 0 V, being at the least one order of magnitude higher than that of a typical common source made with JFETs or DeplMOS [33].

Fig. 14 depicts the measured characteristic of the hysteretic VM. The actual values of the threshold voltages are $V_H = 1.65$ V and $V_L = 1.1$ V. The capacitance C_{STORE2} was set to 100 nF in order to minimize the charge-sharing effect between C_{STORE1} and C_{STORE2}. The load connected to C_{STORE2} was $R_{LOAD} = 1$ MΩ, roughly corresponding to the intrinsic consumption of recent energy harvesting circuits such as the one in [45]. The ΔV_{STORE}=150 mV in Fig. 14, depends on the fact that the boost oscillator is switched from an unloaded mode to a loaded mode (~1 MΩ). In addition, the value of the series resistance R_S does not affect $V_{IN,MIN}$ given that at 15 mV the average current consumed by the circuit is only $I_{IN} \cong 5$ µA, corresponding to an input impedance seen from the source equal to ~3 kΩ. The drained power from the source is $P_S = V_{IN,MIN} \times I_{IN} = 75$ nW. It is worth noting that as the TEG scales, R_S increases. Since the presence of R_S produces a voltage divider together with the input impedance of the oscillator, as rule of thumb, we might safely neglect the voltage drop on R_S if this resistance lower than 1/20 of the input impedance of the oscillator, otherwise the effects of such resistance need to be taken into account considering the effective voltage drop on it.

Fig. 15 depicts a view of the start-up of the system achieved with a Peltier Cooler Multicomp MCPE1-03108NC-S [44] used as a TEG. One side of the TEG was put in contact with a cup containing hot water at ~60°C, whereas the other side was exposed to an environmental temperature of around 25°C. No load was connected to C_{STORE} (buffered node). The system starts oscillating at $V_{IN} = 15$ mV. V_{STORE1} reaches about 350 mV when V_{IN} is about 25 mV. This start-up voltage is higher than the declared minimum start-up voltage of recent buck-boost converters like that in [45] or the TI bq25504 [46]. Moreover, we remark that at $V_{IN} = 15$ mV with multistage charge-pumps or Villard/Greinacher rectifiers the output voltage V_{STORE1} can be potentially increased even at such low input voltage levels [18] [19]. Concerning [46], it is worth remarking that the converter is able to harvest energy from sources down to 80 mV only once started, but the minimum input voltage from an off-state is 330 mV. Moreover, through

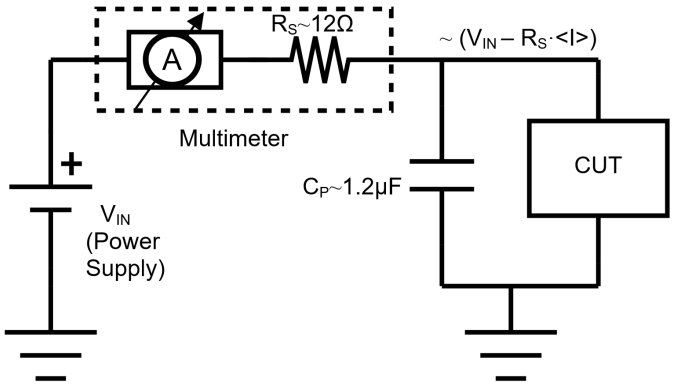

Fig. 12: Schematic of the measurement set-up of the Circuits Under Test, used for both the designed circuits.

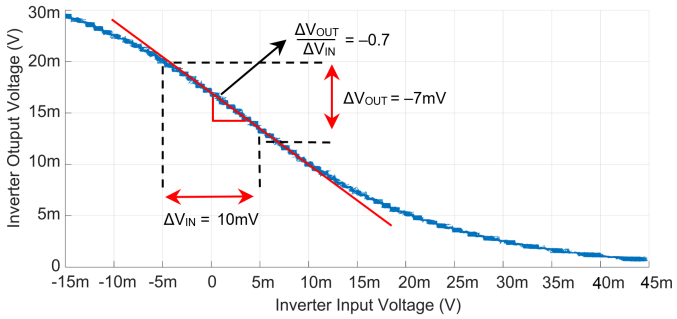

Fig. 13: Measured unloaded DC Voltage transfer characteristic of the CMOS inverter input stage of PT-based step-up oscillator.

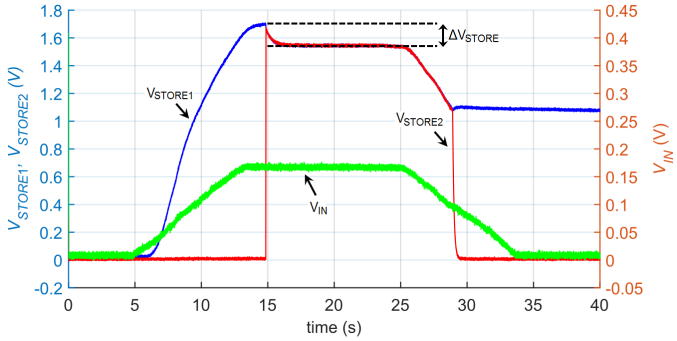

Fig. 14: Start-up of the step-up oscillator with the CMOS inverter as input stage: input and output voltage, and characteristic of the VM. The two threshold voltages are respectively V_H=1.65V and V_L=1.1V. R_{LOAD}=1MΩ.

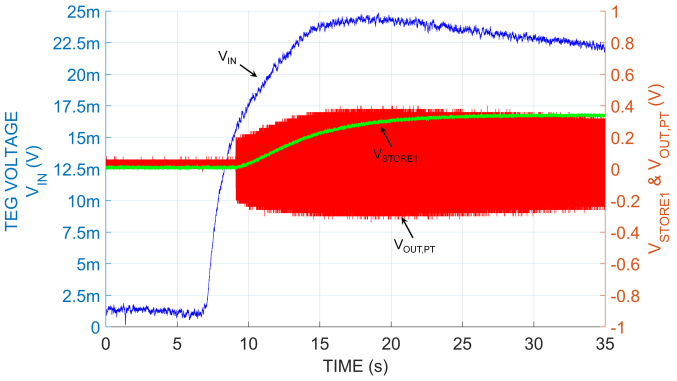

Fig. 15: tart-up of the step-up oscillator based on CMOS inverter obtained with a TEG Multicomp MCPE1-03108NC-S. The system starts oscillating at 15mV. No-load connected on C_{STORE2}.

Spice Simulations we noted that, if the NatMOS are replaced with standard-V_{TH} CMOS devices with same size and channel length, the minimum voltage to start an oscillation is around 250 mV, hence using low-threshold devices is one of critical points of the presented solution. However, if the low-voltage source is able to provide output voltages higher in the range of 250-300 mV, it might have more sense to implement a low-voltage ring oscillator driving a multi-stage charge pump.

The presented system is able to work also if a negative TEG voltage is provided without any need to switch its polarity at the input of the voltage booster (see Fig. 16). This happens because the input inverter is made of low-threshold MOSFETs whose channel is still conducting when supplied by a small negative voltage.

In this specific case, M_INV (see Fig. 8) has a different behavior: the signal from the input of M_INV to its output is experiences a ~0 degrees of phase shift. This happens because the transcondutances are negative: since the polarization of V_{IN} is reversed, the current inside the transistors is reversed as well. The increase in the V_{GS} injects more electrons in the channel that can be collected at the source, hence a positive ΔV_{GS} produces a negative ΔI_{DS}; hence according to (3) the gain of the stage is positive. The oscillation is triggered in the PT capacitive window at a frequency $f_{OSC}<f_S$, because in this window the phase shift of the PT voltage gain is ~0.

By looking at Fig. 16, we see the circuit start-up achieved with a negative TEG voltage: 800 mV at the V_{STORE1} node are obtained when $V_{IN} = -50$ mV. Moreover, the system oscillates at the first mode of the PT as depicted in Fig. 17: we are able to note also that the oscillation waveforms at the PT input and output port respectively are mostly in phase: an oscillation is maintained when $V_{IN} = -8$ mV. However, in this condition, the oscillation has only 130 mV of peak-to peak amplitude.

Fig. 18a depicts the measured average current I_{IN} drained by the source as well as the measured voltage V_{STORE1} for different values of V_{IN}, whereas Fig. 18b depicts the asymptotic voltage step-up ratio and the oscillator input impedance $Z_{IN,OSC}$ seen from the source. A maximum voltage step-up ratio of ~17.5 is obtained around 40 mV.

$Z_{IN,OSC}$ is in the range of few kΩ, meaning that the oscillator based on the CMOS inverter, differently from the version with the CS stage, is also suitable for more resistive power sources such as UHF rectennas [47]. As a demonstration of the statement, we performed an additional measurement with the power supply with a series resistor R_S=3.3 kΩ, emulating a rectenna. In this case the circuit self-starts around V_{IN}=50 mV, given that most of the voltage drop is located on R_S. The circuit has an input impedance $Z_{IN} \cong 1$ kΩ, that is a value congruent with Fig. 18b. When $V_{IN} \cong 220$ mV, the circuit is polarized with $V_{IN2} \cong 50$ mV, providing ~1 V at the node V_{STORE1} (Fig. 19), with a drained current $I_{IN} \cong 48$ µA.

Concerning Fig. 18, it is worth noting that when $V_{IN} \cong 150$ mV, the amplitude of the oscillation saturates due to the presence of the three protecting diodes D_A, D_B and D_C (see Fig. 6) at the gate of the main inverter, hence the increase of V_{IN} has almost no effect on the output voltage, given that the oscillation amplitude cannot increase. Moreover, for negative values of V_{IN}, the maximum value of V_{STORE1} is around 1.05 V, when $V_{IN} = -100$ mV. However, $V_{STORE1} = 1$ V is obtained when $V_{IN} = -80$ mV.

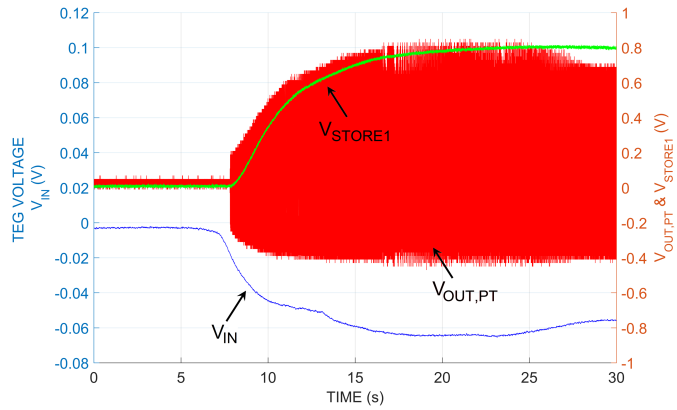

Fig. 16: Start-up of the step-up oscillator with a CMOS inverter input stage obtained with a TEG Multicomp MCPE1-03108NC-S for negative input voltages. The system starts oscillating at –8mV. A moving average was applied to V_{IN} in order to remove the oscilloscope noise.

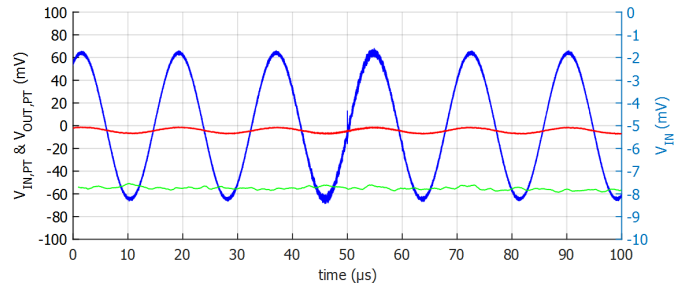

Fig. 17: Input and output oscillation at the PT ports, for $V_{IN} \cong -8$ mV. The signals are almost in phase.

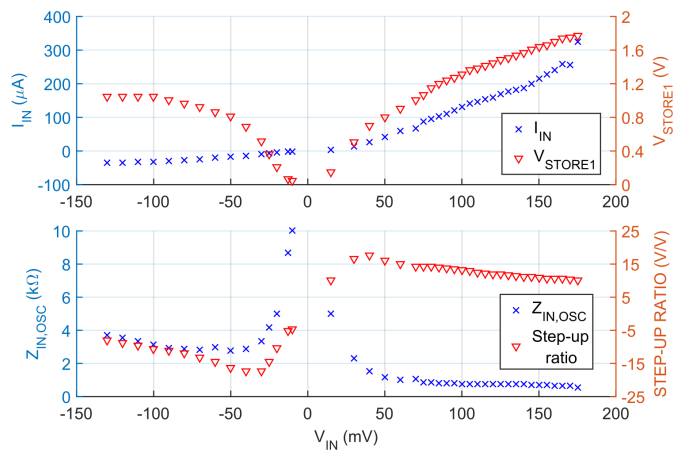

Fig. 18 (a) V_{STORE1} and average current I_{IN} sourced from the TEG as a function of the TEG voltage; (b) oscillator Input Impedance $Z_{IN,OSC}$ and Voltage Step-Up ratio.

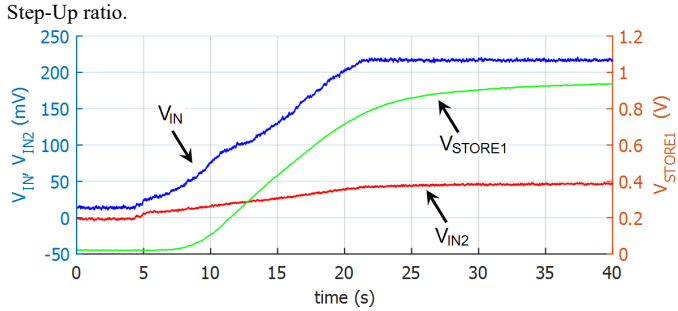

Fig. 19 V_{STORE1}, V_{IN} and V_{IN2} when a R_S=3.3 kΩ. $V_{STORE1} \cong 1$ V when $V_{IN} \cong 220$ mV (emulated rectenna).

Fig. 20 depicts the behavior of the VM when a load R_{LOAD} of approximately 120 kΩ is connected in parallel to C_{STORE2} (100 nF). This is a worst-case in terms of load conditions and it accounts for more complex circuits, e.g. the in-rush current of the conventional DC/DC of Fig. 2. As in Fig. 20, the law describing the voltage across C_{STORE2} can be written as $V_{STORE2}=1.7\cdot\exp(-\Delta t/R_{LOAD}\cdot C_T) = 1.1$V, hence the time interval Δt, between two consecutive actions of the VM is given by $\Delta t=\ln(1.7/1.1)\cdot R_{LOAD}C_T\cong$ 0.25s (Fig. 20 shows ~0.3s). The capacitance $C_T = C_{STORE1}+ C_{STORE2}$. In fact, the system is still able to sustain such worst-case load for about 0.3 s before the VM detaches it from the boost oscillator. If higher stored energy is needed, C_{STORE1} can be increased and Δt in (13) will increase accordingly. In a real application, this consumption represents the current drawn by the conventional power converter when it's being turned on and before it has started extracting power.

Fig. 21 depicts the oscillation at the PT input port (CMOS inverter output port) and PT output port (M_INV input port) obtained at V_{IN} = 40mV. The phase difference is about –175°, meaning that the PT is working close f_p, as explained in [33].

Concerning the efficiency of the circuit, it is not possible to find the efficiency as a function of V_{IN} at the node V_{STORE1} because the VM keeps the load disconnected from the boost oscillator. Moreover, the node V_{STORE2} is connected to the load when $V_{STORE1}\cong$ 1.65 V occurring at $V_{IN}\cong$ 140 mV (see Fig. 18a). The increase of V_{IN} does not affect significantly the voltage at the node V_{STORE1}, because the oscillation amplitude saturates due to the presence of the protecting diodes (see Fig. 6). However, in Table II we report some measured efficiency values for different loads connected at the V_{STORE2} node. The letters B and C indicate the phases as in Fig. 9.

B. *Step-up oscillator with common-source amplifier stage*

The measurements were performed according the set-up depicted in Fig. 12. The measured steady-state oscillation frequency is 103.7 kHz, whereas the estimated frequency from an AC analysis 108.1 kHz. The discrepancy is due to the fact that in the steady-state operation the load seen from the PT is different from the load seen at the beginning of the oscillation, that is the condition in which the oscillation frequency was estimated. Typical oscillation waveforms for the PT-based step-up oscillator with normally-on transistors at the PT input port (CS output port) and PT output port (CS input port) can be found in [33].

One thing worth of attention is that, although the current-voltage equations a n-type DeplMOS are identical to that of a n-type JFET (they both have a negative V_{TH}, or "pinch-off" voltage), there is one intrinsic difference. In JFET-based oscillators such as the one in [33], the peak value of the oscillation at the gate-source voltage node cannot exceed ~0.5 V, otherwise the p-n junction between the gate and source of the JFET can be partially turned on, thus causing the loss of the transistor effect. As a matter of fact, in [33], the oscillation in order to be sustained has a DC offset value much lower than 0V: this implies that the output oscillation falls below the pinch-off voltage of M_1 and once it

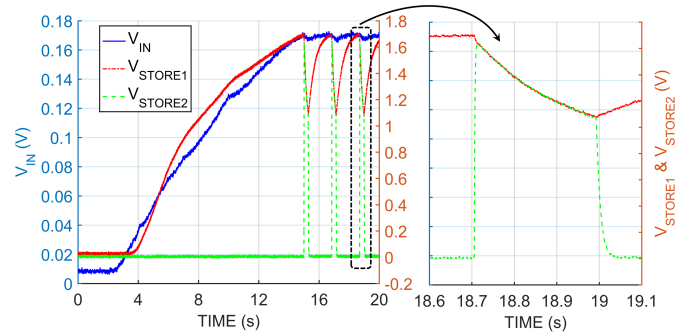

Fig. 20: Behavior of the VM in step-up oscillator based on a CMOS inverter when a 120kΩ load is connected in parallel to C_{STORE2}. When V_{STORE2} and V_{STORE1} are short-circuited, they get discharged according to the discharging law of a RC circuit.

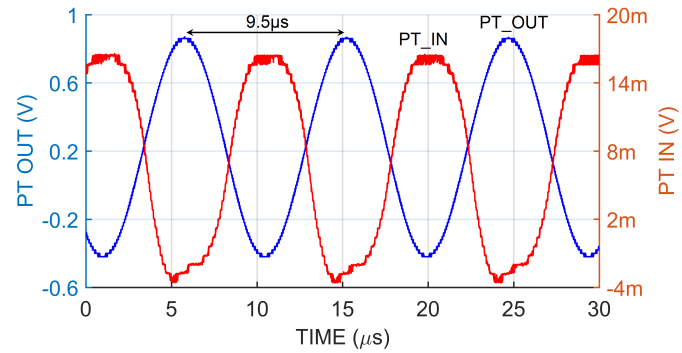

Fig. 21: Oscillation waveforms at the PT output port (CMOS inverter input) and PT input port (CMOS inverter output), when V_{IN}=40mV. The filtering effect of the PT is noticeable.

TABLE II
EFFICIENCY VALUES FOR DIFFERENT LOAD AT THE V_{STORE2} NODE

V_{IN} (mV)	I_{IN} (B) (µA)	P_{IN} (B) (µW)	I_{IN} (C) (µA)	P_{IN} (C) (µW)	R_{LOAD} (MΩ)	V_{OUT} (B/C) (V)	P_{OUT} (C)(µW)	Eff (C) (%)
140	210	29.4	300µ	42	0.9	1.7 /1.5	2.5	6
140	210	29.4	240µ	33.6	5	1.7/1.65	0.55	1.7
140	210	29.4	220µ	30.8	10	1.7/1.68	0.28	0.9
140	210	29.4	215µ	30.1	20	1.7/1.7	0.145	0.5
140	210	29.4	212v	29.7	50	1.7/1.7	0.058	0.2
140	210	29.4	~210µ	~29.4	150	1.7/1.7	0.019	0.07

is in steady-state, the minimum voltage (or power) to sustain oscillation is considerably lower than the minimum voltage (or power) to start the oscillation (hysteretic behavior), because the input circuit behaves as an AB amplifier (the current is off during a portion of the oscillation period, see [33]). With DeplMOS, since there is not any upper boundary limit to the gate-source voltage, the oscillation has a ~0 V offset (see Fig. 22) and it might slightly fall (or maybe will not fall at all) below the threshold voltage of the transistor (according to the oscillation amplitude which in turn depends on V_{IN}): in this case the voltage (or power) required to start the oscillation is essentially the voltage (or power) to sustain the oscillation (no hysteretic behavior). In other words, a JFET-based oscillator as a higher robustness versus time variations of temperature gradients, compared to a DeplMOS-based oscillator.

Fig. 22 shows the start-up of the circuit. V_{IN} is slowly ramped up to 48 mV. Differently from the CS stage reported in [33], the oscillation has not any DC offset. The circuit starts oscillating at $V_{IN}\cong$ 36 mV. In such conditions, with no load connected in parallel to C_{STORE}, V_{STORE} reaches about 2.7 V, corresponding to a stored energy in C_{STORE} equal to:

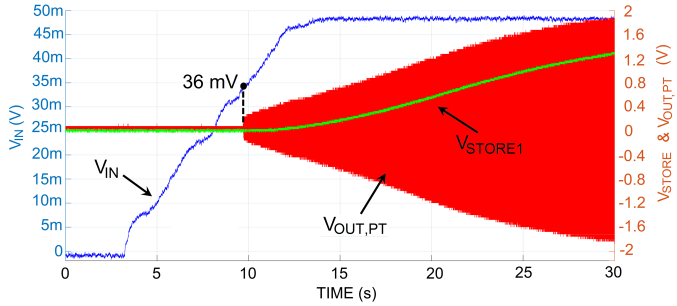

Fig. 22: Start-up of the step-up circuit with a CS input stage and R_S=12Ω. V_{IN} is referred to the left y-axis, whereas V_{STORE} and $V_{OUT,PT}$ are referred to the right y-axis. The start-up occurs at V_{IN} = 36mV. No load on V_{STORE}.

$$E_{STORE} = \frac{1}{2} C_{STORE} \left(V_{STORE}\right)^2 \cong 17\mu\text{J} . \qquad (13)$$

The average current consumption of the circuit in steady state operation is approximately equal to 500 µA at V_{IN} = 36 mV. As a consequence, the voltage drop on R_S is equal to 6 mV. When the power supply (or TEG, see Fig. 23) is directly connected to the circuit, the start-up was found to be around 31 mV, which is a value compatible with the results obtained in [33] with the aid of an inductor, but we remark that in this case the insertion of any magnetic component was avoided, and that we exploited an additional capacitance C_{OPT} in parallel to the PT input port, to modulate the total loop gain, in accordance with (10).

In this case, we used the aforementioned Peltier Cooler MCPE103108NC-S 18.8W [44]. This device has an internal resistance of 0.35 Ω leading to a negligible voltage drop. Fig. 23 depicts the start-up of the circuit achieved with the aforementioned Peltier device. As it can be noted, the start-up value is still found to be about 31 mV, confirming that lower values of R_S yield lower activation voltages.

Fig. 24 depicts the measured V_{STORE} obtained when $V_{IN} = V_{IN,MIN}$ = 31 mV as a function of the load and also the power delivered to the load defined as $P_{LOAD} = V_{STORE}^2/R_{LOAD}$. The maximum output power occurs at around 38 MΩ of load; however, once again the purpose of such boost circuit is not to maximize the output power, but minimizing the operating input voltage. This type of circuit is intended for driving loads in the range of 100 MΩ, like for example, an ultra-low power voltage monitor, or the gate of a power switch in a standard power converter, as it was done in [35]: once the main converter is turned on, the boost oscillator is switched-off.

Fig. 25a depicts the measured current drawn from the source I_{IN}: at input voltages around 70 mV, currents in the range of 1 mA are flowing from the source. Fig. 25a depicts also the asymptotic value of V_{STORE} as a function of the input voltage V_{IN}. In Fig. 16, an equivalent $R_{LOAD} \cong$ 10 MΩ was connected, due to the oscilloscope probe. We remark that an ultra-low power VM presents a significantly higher load resistance (such as ~180 MΩ for the VM presented in this work) . Then, the obtained results should be intended as in a worst-case condition. Fig. 25b is strictly related to Fig. 25, and depicts both the Voltage step-up ratio reaching almost 60 at V_{IN} = 85mV, whereas the average oscillator input impedance seen from the source is around 70 Ω, confirming that the devices are working in their deep triode region.

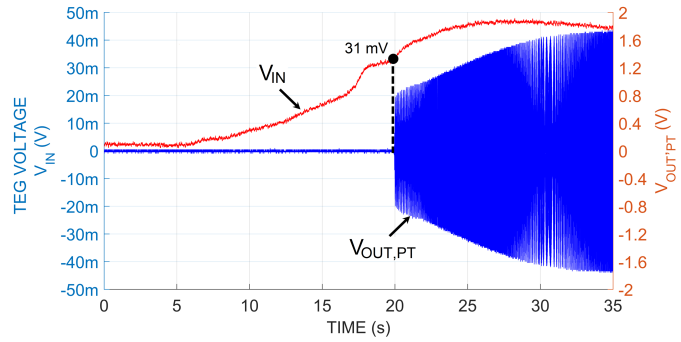

Fig. 23: Start-up of the step-up converter with a CS input stage with a Peltier Cooler used as a TEG (MCPE1-03108NC-S). The start-up voltage is ~31mV.

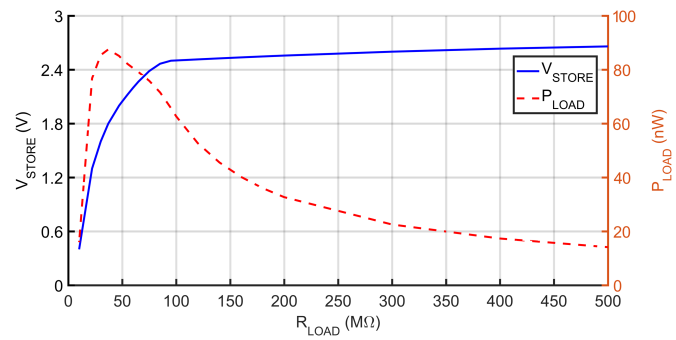

Fig. 24: V_{STORE} and P_{LOAD} as a function of R_{LOAD} for the step-up oscillator with a CS input stage. V_{STORE} is referred to the left y-axis, whereas P_{LOAD} is referred to the right y-axis. Graph obtained with V_{IN} = 31mV (power supply).

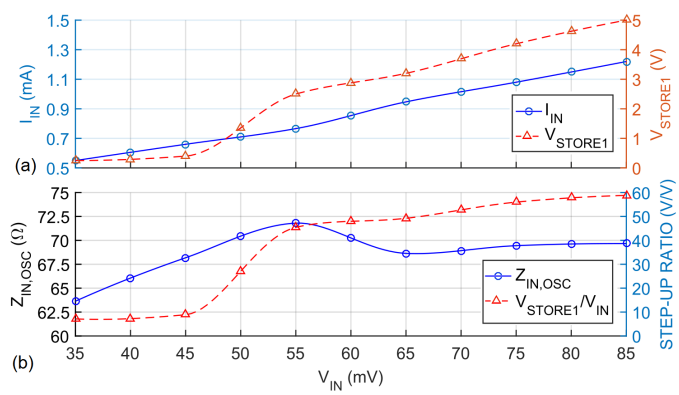

Fig. 25 a) I_{IN} and V_{STORE} for the circuit with a CS input stage with a worst case R_{LOAD} ≅10MΩ placed between V_{STORE} and ground nodes. The current consumption ranges from ~0.5 mA up to 1.2 mA, whereas V_{STORE} ranges from 250 mV up to 5 V when V_{IN} varies from 35 to 85 mV. b) Input impedance $Z_{IN,OSC}$ and voltage Step-up ratio of the oscillator with a CS input stage.

Fig. 26 depicts the measured efficiency for two cases: a) the efficiency is measured for a single input voltage ($V_{IN,MIN}$), and the R_{LOAD} is varied from 10 MΩ up to 500 MΩ. The maximum efficiency is found for loads lower than 50 MΩ, however such circuit is intended for higher loads; b) the load is kept fixed at 10 MΩ, and then V_{IN} is varied from 35 mV to 85 mV: in this case, the efficiency increases as V_{IN} increases, because the oscillation grows in amplitude and might switch-off the transistors.

That the presented system is intended for start-up purposes, hence its efficiency is poor. In [35] the system was used to activate an inductor-based fixed-frequency boost DC/DC converter with efficiencies higher than 40% in the range of 30-50 mV, for loads of 30 kΩ up to 60 kΩ. By comparison in [48], efficiencies up to ~60% with output power in the mW

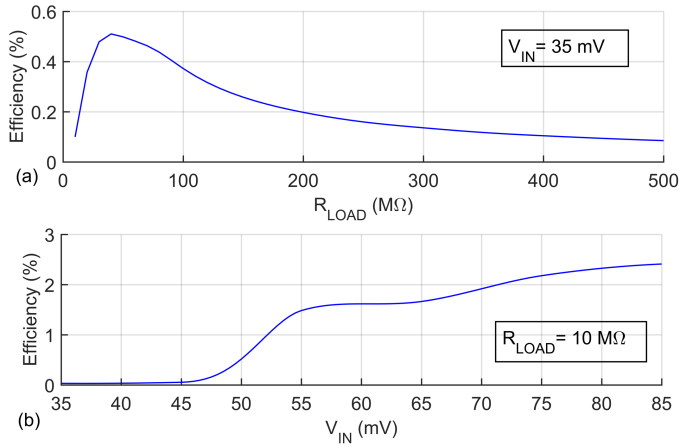

Fig. 26: a) Efficiency of the system as a function of the load for a fixed V_{IN}; b) efficiency of the system as a function of the input voltage for a fixed R_{LOAD}.

range, are achieved exploiting a transformer-reuse technique. The presented topology in this work is fully compatible with a transformer-reuse technique, by using the same PT, after the start-up phase in a resonant power converter for microwatt applications.

IV. CONCLUSIONS

This work has presented two circuit topologies of ICs for EH purposes from ultra-low DC sources exploiting PTs for kick-starting without need of any battery.

The circuit based on the CMOS inverter requires common low-V_{TH} MOSFETs instead of negative-V_{TH} MOSFETs used in the CS inverting stage and is able to work with double polarity input signals without the need of switching matrixes. As a matter of fact, start-up values down to +15 mV and −8 mV where measured, with maximum output voltages of 1.75 V for positive polarization (achieved at 140 mV), and 1.05 V (achieved at −100 mV). Moreover, the design of the system was completed through a VM consuming only 15 nW.

Another advantage is that the boost oscillator based on the CMOS inverter has higher input impedance, in the range of several kΩ, with respect to the inverting CS stages made up by DeplMOS polarized in their deep triode region. This lowers the average power consumed from the source and makes the circuit thus less sensitive to variations of the parasitic series resistance of the harvesting source. The higher input impedance makes this type of oscillator also suitable for harvesting from rectennas as well, given that typical equivalent output resistance of such harvesters is in the order of several kΩ as well. This assertion has been demonstrated with measurements performed with a 3.3 kΩ series resistance. The CS-based step-up oscillator is not suitable for rectennas because of its low input impedance (tens of Ω), that would lead the Rectenna working close to its short circuit condition.

The circuit with the input stage made by a CS stage formed by two DeplMOS achieves a minimum start-up voltage of about 31 mV without using any magnetic components, and can be successfully supplied by a standard miniature Peltier Cooler used as a TEG. One of the advantages of this circuit is the use of integrated Schottky diodes in the rectifier, with lower voltage drops compared to conventional p-n diodes or diode-connected MOSFETs, and with higher voltages in the storage capacitor. Step-up ratios as high as 58 were obtained, when the input voltage is around 85 mV. On the other side, the main drawback is the average current drained by the source (around 1 mA at 70 mV of input voltage), which is reflected in a very low input impedance, between 60 Ω and 70 Ω, given that the transistors in CS stage are polarized in their deep triode region. The low oscillator input impedance seen from the source makes this circuit more sensitive to the parasitic series resistance of the energy harvesting transducer. This makes this particular implementation more suitable for TEG harvesters with output series resistances in the range of few Ohms.

In the experiment, a discrete PT was used. However, the adopted PT was conceived to handle power levels in the order of several W. A tailored PT design for the voltage step-up application, possibly implemented with MEMS technologies for wafer-level of package-level integration, focused in shrinking its dimensions, might bring interesting results. Moreover, according to the electrodes layout and choice of operating mode (thickness or "33" mode, extensional or "31", or both as it happens in Rosen-type PTs) depending on the aspect ratio of the PT, it is possible to design the frequency at which the system should oscillate. Such design should aim at implementing a PT capable of high voltage gains while handling powers in the range from few µW to few mW, which is the typical power managed in EH systems.

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Antonio Camarda received the M.S. degree in Electronic Engineering from the Bari Polytechnic, Italy, in 2010. He has then been a SAP IT Consultant for a year and a half. In 2011 he joined the research lab University of Bologna –ST Microelectronics as a free-lance analog IC designer. In 2013 he was selected for the PhD program. In 2015 he joined the Vienna University of Technology as visiting PhD student for the fabrication of MEMS piezoelectric transformers. He gained his PhD from the University of Bologna in 2016 with a dissertation in the More than Moore context, focused on the integration of both Magnetic and Piezoeletric devices together with the ICs. His research interests include modelling and design of piezoelectric devices, micro-power ICs, energy harvesting systems, ultra-low voltage start-up techniques and power conversion systems.

Marco Tartagni received the M.S. and the Ph.D. degree in Electronics Engineering both from the University of Bologna (Italy). He joined the Electronics Engineering Department at the Caltech in 1992 and in 1994. Since March 1995 he has been with the Electronics and Information Engineering Department, University of Bologna, as Associate Professor. From 1996 to 2001 he has been team leader of the joint STM and University of Bologna lab and, since 2014, member of the scientific committee. He has been local and European coordinator of several FP5-6-7 projects. He was co-recipient of the 2004 IEEE Van Vessem Award. He is co-author of more than 100 peer-reviewed scientific publications and holder of more than 20 US/WIPO patents.

Aldo Romani received the Dr. Eng. degree in Electrical Engineering in 2001 and the Ph.D. degree in Electrical Engineering, Computer Science and Telecommunications in 2005 from the University of Bologna (Italy), where he currently serves as associate professor. He has been working on CMOS integrated sensors, applications of piezoelectric materials, and energy harvesting systems. He is a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference and is author or co-author of more than 60 international scientific publications.