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A Nano-current Power Management IC for Multiple Heterogeneous Energy Harvesting Sources

Michele Dini, Aldo Romani, Matteo Filippi, Valeria Bottarel, Giulio Ricotti, Marco Tartagni

***Abstract*— This paper presents a fully autonomous power converter IC for energy harvesting from multiple and multi-type sources such as piezoelectric, photovoltaic, thermoelectric and RF transducers. The converter performs an independent self-adapting input power tracking process for each source. The peak power conversion efficiency measured during single-source operation is 89.6%. With all sources enabled, the intrinsic current consumption is as low as 47.9 nA/source. A self-starting battery-less architecture has been implemented in a 0.32 µm STMicroelectronics BCD technology with a 2142 µm x 2142 µm die area. The IC only requires a single shared inductor and an external storage capacitor for the basic working configuration. With respect to other multi-source energy harvesters, this design specifically introduces a series of nano-power design techniques for extreme minimization of the intrinsic consumption during operation. The small chip size combined with the limited number of required external component, the high conversion efficiency, and the state-of-the-art intrinsic nano-current consumption make the IC suitable for many critical applications with very limited available power such as wearable devices or unobtrusive wireless sensor networks.**

***Index Terms*—nano-power design, multi-source energy harvesting, piezoelectric transducers, thermoelectric generators, photovoltaic, MPPT, fractional open circuit voltage.**

I. Introduction

Energy autonomous systems are increasingly attracting attention as they can be a viable solution for extreme monitoring in a wide set of applications. Disengaging from typical battery constraints (e.g. charging, leakage, temperature limitations, degradation over time, replacement) can be the starting point for self-powered pervasive sensing and monitoring applications. Several environmental energy sources have been widely investigated in the last decade as vibrations [1], light [2], heat [3] or electromagnetic radiation from communication equipment [4]. All these energy types can be successfully exploited with appropriate transducers, e.g. piezoelectric transducers (PZs) for generating power from vibrations, photovoltaic (PV) cells for sunlight or artificial indoor light, thermoelectric generators (TEGs) for heat flows in wearable and industrial applications, rectifying antennas for incident electromagnetic waves. However, the available power is in most cases constrained down to few µW or less [5]. Hence, in order to achieve sufficient efficiency it is necessary to couple energy transducers with specific power conversion and management circuits [6]-[9] , with very low power consumption. In this context, many energy conversion techniques and circuits have been developed in the last years with the main purpose of enabling autonomous wireless sensing applications.

One specific issue of energy harvesting, in addition to energy shortage, is the irregularity of energy flow. As an example, some energy sources are typically available only during specific parts of a day (e.g. sunlight) or undergo significant intensity variations over time (e.g. vibrations from industrial machinery). When the involved power levels are very low and irregular, the combination of multiple energy sources of the same (e.g. only PZ) [10]-[12] or different types (e.g. TEGs and PV or other combinations) [13]-[16], is an effective solution for increasing the overall input power and the energetic reliability of the system. A multi-source multi-type approach for energy harvesting is also a typical scenario for wearable electronics applications [3],[5],[17] in which energy can be extracted from ambient light, body movements and heat, and RF energy from communication devices. Another area of interest for multi-source harvesting is the integration of both the converter and the transducer in the same package or on the same silicon die as shown in previous works with MEMS piezoelectric transducers [8],[18], micro fabricated thermoelectric devices [19] and solar cells [20].The union of multiple energy flows is not a trivial task. The connection of N independent energy harvesters to a common output node V_{ST} through a unidirectional switch, e.g. a diode, is the simplest method [11],[13],[15],[16], also known as "power ORing" (Fig. 1 (a)). The main drawback is the "winner takes it all" nature: V_{ST} is generated by the energy harvester with the highest output voltage, excluding or limiting the contributions from other harvesters. A more

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M. Dini, A. Romani, M. Filippi and M. Tartagni are with the Advanced Research Center on Electronic Systems (ARCES) and the Department of Electrical, Electronic, and Information Engineering «Guglielmo Marconi» - DEI of the University of Bologna, Cesena 47521, Italy, (e-mail: michele.dini3@unibo.it, aldo.romani@unibo.it, matteo.filippi6@unibo.it, marco.tartagni@unibo.it; phone: +39 0547 339537; fax: +39 0547 339208).

V. Bottarel and G. Ricotti are with STMicroelectronics, Cornaredo 20010, Milan, Italy (e-mail: valeria.bottarel@st.com, giulio.ricotti@st.com).

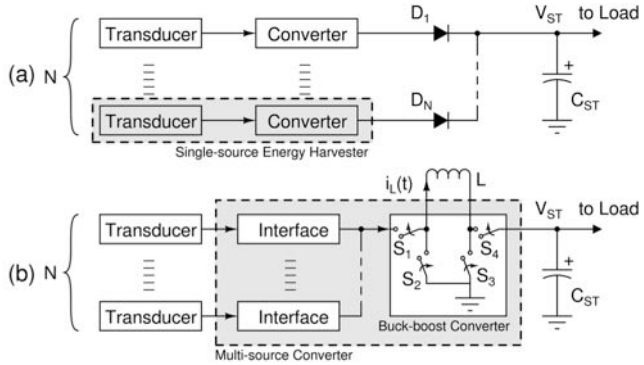

Fig. 1. (a) Basic method for combining energy harvesters output. (b) More efficient method for multi-source energy harvesting.

efficient method is to use a buck-boost converter to join N energy sources with their specific interface [12],[21] to the energy storage C_{ST} as in Fig. 1 (b). This approach allows each source, whatever its output voltage, to charge C_{ST}. On the other hand, an additional interface circuit is needed to match the characteristics of both the source output and the converter input. Furthermore, a controller must ensure that no source can be ever connected with a low impedance path to any other source, wasting energy. The use of a single shared inductor in a multi-source converter for energy harvesting has been previously reported [10],[12],[21],[22]. The inductor can be time shared because the converter typically operates in discontinuous conduction mode (DCM) due to the very low involved power levels.

The low harvestable power requires converter circuitry to draw a small current for its operations for a matter of conversion efficiency. This is a non-trivial task with off-the-shelf ICs and discrete components due to their higher intrinsic parasitic capacitance and their higher power consumption with respect to an integrated optimized custom design. An integrated solution achieves at least a reduction of an order of magnitude in power consumption in comparison to advanced PCB implementations [12],[16] and achieves a considerable decrease of system size as well.

The purpose of this paper is to describe a set of circuital solutions and power reduction techniques suitable for ultra-low-power energy harvesting from multiple and heterogeneous sources, with the focus on energy efficiency of the converter itself. The achieved static consumption of 143.7 nW per source is considerably lower than in recent works on switching converters [21],[23] and active rectifiers [24]-[26]. Such value has been obtained with an energy aware design of each converter block.

That being so, such an optimized IC finds its main application in battery-less systems powered by weak and intermittent environmental power sources, which cannot individually sustain the electronic system under test. Differentiation allows to extract sufficient energy for system operation in a wider range of situations. As a first example, in [27] an airplane structural health monitoring system is powered by vibrations and thermal gradients, since batteries would not be allowed because of harsh environmental conditions. Such systems usually operate with a very low duty cycle [28],[29], with some activations per hour or day while energy is slowly stored, for instance in low leakage super-capacitors. Another possibility for multi-source energy harvesting is the use of multiple differently sized piezoelectric transducers in order to exploit broadband vibrations [11] or different types of human movements [30]. Other attracting applications include environmental or structural monitoring [28],[29], wearable computing and sensing powered by human body [30] or electromagnetic waves [31], implantable bio-systems [32],[33], localization and positioning [34].

II. Principle of Operation

A. Vibrational Energy Harvesting

Several non-linear approaches have been developed for extracting energy from vibrations with piezoelectric transducers (PZ). Converters range from classical full wave rectifiers with an integrated boost converter [35] or with a switched capacitor converter [36] to complex waveform tracking algorithms [37]-[42]. Among the latter category, it is worth to mention synchronous electrical charge extraction (SECE) [12],[38]. The SECE converter, depicted in Fig. 2 (a), is substantially a buck-boost converter, exploiting non-linear techniques and resonant circuits. Among the advantages of SECE, we highlight that: (a) the offset introduced by charge extraction increases the peak-to-peak voltage up to two times; (b) power conversion tracks, by definition, the input vibrations and generally outperforms passive interfaces, especially with irregular and weak vibrations; (c) differently from other approaches, such as passive interfaces [11], synchronized switch harvesting on inductor (SSHI) [37], active energy harvesting [43],[44] and single-supply pre-biasing [45], the power source is kept disconnected from the load. This makes conversion efficiency quite constant in a wide range of conditions. For the purposes of this work, the PZs have been modeled with the first-order capacitive model shown in Fig. 2 (b), which is a reasonable approximation in most

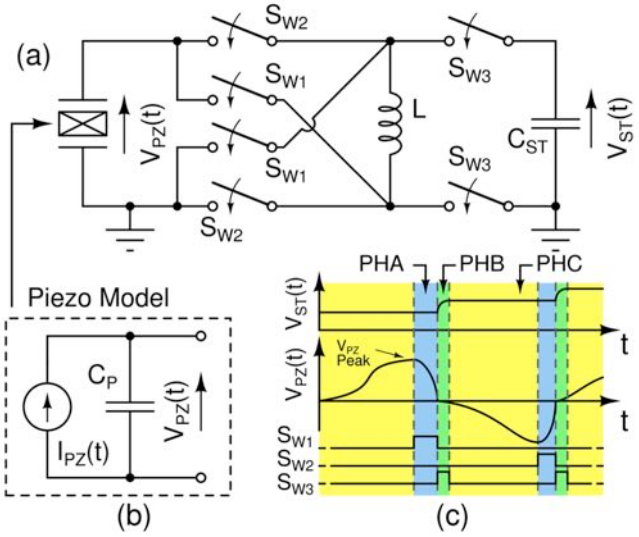

Fig. 2. (a) Circuit schematic for SECE from a PZ, (b) simplified PZ model valid for loosely coupled transducers, (c) sketch of typical waveforms, not to scale, in a SECE converter with energy extraction phases highlighted.

applications. In general, when PZs have a high electro-mechanical coupling, a more complex representation of a PZ [46] should be adopted in order to account for the mechanical damping induced by the power converter. However, for our purposes, the model of a PZ will be satisfactorily composed by the vibration driven current source $I_{PZ}(t)$ connected in parallel with the transducer capacitor C_P. With SECE, energy is extracted synchronously with each peak of $V_{PZ}(t)$ as shown in Fig. 2 (c). Three phases can be distinguished in an energy conversion cycle, namely PHA, PHB and PHC. The latter phase PHC, is an idle phase between two energy extraction cycles. In the first phase PHA, energy is transferred from C_P to the magnetic field in the inductor L. In the second phase PHB, energy is shifted from L into the storage capacitor C_{ST}. Since C_P is discharged at every activation, SECE applies a voltage offset on C_P at the beginning of each elongation. This doubles the peak-to-peak voltage and boosts the available energy [12]. In addition, since the output node is never directly connected to the input PZ source, the SECE converter makes energy conversion efficiency from PZs independent from the values of V_{PZ} and V_{ST}. With respect to a bare passive diode interface, SECE requires an external inductor and an increase of design complexity. However, it will be shown that by exploiting IC technology, the impact of design complexity on the energy consumption of the control sub-system will be extremely weak.

B. Thermoelectric, Photovoltaic and RF Energy Harvesting

Many energy transducers have a DC output voltage, e.g. thermoelectric generators (TEGs), photovoltaic (PV) cells, RF rectennas. A maximum power point tracking (MPPT) circuit is mandatory in order to achieve a high conversion efficiency, which is essential when input power is very limited. Fig. 3 (a) depicts a buck-boost converter in an energy harvesting application storing energy in a capacitor C_{ST}, while Fig. 3(b) shows a resistive model suitable to describe a generic DC source, in which R_S is the internal source resistance. Since we target applications with extremely low input power levels, the buck-boost converter is expected to operate in discontinuous conduction mode. Although the accuracy of the MPPT circuit is important, the power required for the MPP computation should still be a negligible share of the available power, being the shortage of input energy one of the main constraints. In this work, a fractional open circuit voltage technique [26] (FOCV) has been chosen for MPPT. It is a trade-off between accuracy and power absorption, as the FOCV is an a priori technique not requiring on-the-fly computations. Accuracy relies on the assumption that the MPP is predictable and depends only on the open circuit voltage V_{DC0}, which is true for purely resistive sources as TEGs and an acceptable approximation for PV cells [48]-[50]. The MPP voltage is computed as $V_{MPP}=\beta V_{DC0}$, where β depends on the type of transducer: for TEGs and resistive DC sources β=0.5, while for PV cells literature reports values ranging from 0.71 to 0.82 [48],[49], so that β=0.75 was conservatively chosen in order to prevent operation of the PV cells in the region in which the output current is exponentially decreasing.

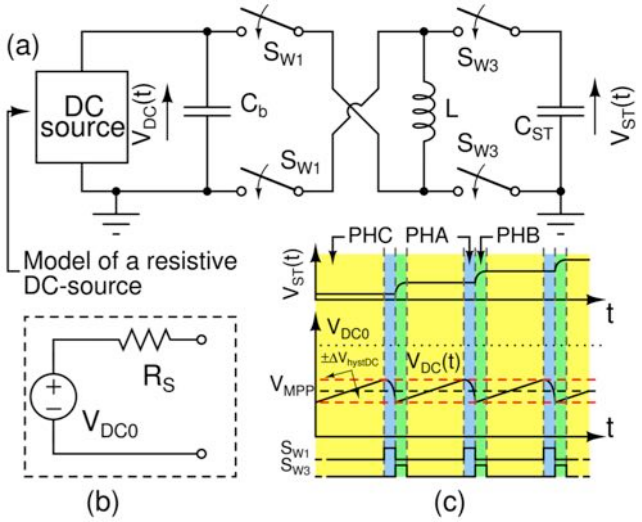

Fig. 3. (a) Circuit diagram for DC-source harvesting; (b) model of a generic resistive DC source; (c) sketch of typical waveforms, not to scale, in a DC harvesting converter, with energy extraction phases highlighted and MPPT references.

Fig. 3 (c) illustrates typical waveforms during energy extraction from a generic DC source. C_b is an energy buffer used to reduce the switching frequency of the converter as dynamic power consumption is proportional to switching frequency. V_{MPP} is kept as a reference and V_{DC} is kept into a $\pm\Delta V_{hystDC}$ range, which is the hysteresis of the comparator that detects the conditions for starting and stopping the energy extraction cycle. As in SECE conversion, three phases PHA, PHB and PHC can be distinguished: in PHA energy is transferred into L and V_{DC} then decreases; in PHB the energy is transferred from L to C_{ST}; PHC, which overlaps PHB, is an idle state in which the DC source charges C_b.

III. Nano-Power Converter Architecture

A. Overview

The block diagram of the proposed buck-boost converter IC is shown in Fig. 4. It features nine input channels, five of which are dedicated to PZ and the remaining four to DC sources. Among the DC input channels, two of them are dedicated to high voltage (HV) sources with 1 V$\leq V_{DC0}\leq$5 V, while the remaining two are optimized for low voltage (LV) sources, typically with 100 mV$\leq V_{DC0}\leq$1 V. Energy can be extracted simultaneously from up to 9 sources and transferred into the energy storage device (e.g. a supercapacitor). A high number of channels was deployed in order to demonstrate the high scalability of the proposed approach and the negligible impact on intrinsic consumption of the power converter. However, unused channels can be disabled. Multiple input channels allow simultaneous energy extraction from multiple and heterogeneous transducers such as PZ, TEGs, RF harvesters and PV cells, in order to guarantee energy coverage with intermittent sources. A specific feature is the buck-boost converter core shared among all the channels, in order to limit die area and energy absorption; moreover, this allows the use of a single external inductor. The inductor value is critical:

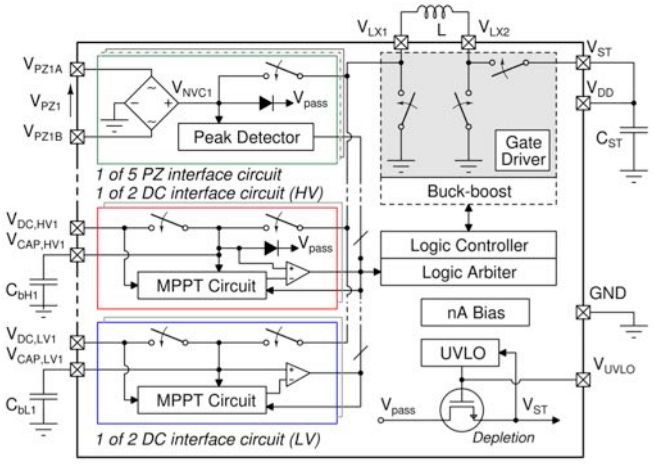

Fig. 4. Block diagram of the proposed heterogeneous multi-source converter.

low values, e.g. tens of µH, require a high reactivity of the switching circuits leading to high power consumptions, while high values, e.g. some mH, translate into a bulky inductor, not suitable for extreme miniaturisation.

The supply voltage V_{DD} of the converter and the energy storage output V_{ST} are shorted in order for the converter to supply itself with the harvested energy, leading to a fully autonomous solution. The energy stored in C_{ST} is also available to an external load such as a low dropout regulator (LDO) supplying a WSN node. In a more complex design like a system-on-chip (SoC), the LDO can be directly integrated within the same chip together with all application circuits. In the following sections of the paper, V_{ST} will be referred to as the energy storage voltage, whereas V_{DD} as the supply voltage of the converter. Moreover, where not specified, the bulk terminal of MOSFETs has to be considered connected to V_{DD} or GND for p-channel and n-channel MOSFET respectively.

The IC has been designed in a 0.32 µm BCD technology from STMicroelectronics. All the transistors in the schematics should be assumed to be 5V MOSFET except otherwise noted. In addition to standard 5V CMOS devices, low threshold CMOS and n-channel depletion MOSFET have been used. The IC has been designed as a general-purpose building block for ultra-low-power systems, compatible with both integrated and discrete electronics. It can also fit into a SoC design as the harvesting core of the IC is based on standard MOS transistors. In case a depletion-mode MOSFET is not available in the chosen technology, it can be replaced by a standard n-channel MOSFET. However, a secondary DC/DC such as a charge-pump would be required in order to provide a sufficient gate voltage to make it conductive initially at the expense of increased complexity, silicon area and leakage current.

The converter starts to operate in passive mode, in which V_{ST} and V_{pass} are shorted by a depletion n-channel MOSFET which acts as a normally-closed switch (Fig.4). All the PZ and HV DC sources are connected to V_{pass} through a diode, so that in discharged states current may flow to C_{ST} through the depletion-mode MOSFET. As V_{ST} rises, the output of an under-voltage lock-out (UVLO) circuit starts following V_{ST}, in order to keep the depletion-mode MOSFET conductive. Such path is then cut off by driving the gate of the depletion MOSFET to 0 V as soon as the UVLO triggers (V_{UVLO} is high during start-up in passive mode), nominally at $V_{DD} \geq V_{DDmin}$ (V_{DDmin}=1.38 V nominal), as this ensures that the supply voltage is high enough for every circuit block to start active operation.. The control flow-chart of the system is depicted in Fig. 5 where the phases of an energy extraction cycle are illustrated, together with the transitions between passive and active state.

Fig. 6 depicts a real-world scenario with the initial start-up of the converter described in this paper and measured with stimulated devices: a Q220-A4-303YB PZ (acceleration a_{RMS}=0.164g, $V_{PZ}(t)$=4.1sin(128πt) V, C_P=52 nF,) from Piezo Systems and an Ixys KXOB22-01X8 PV module (indoor laboratory light, V_{DC0} = 1.2 V) contribute to charge C_{ST}=33 µF. Energy is at first passively harvested and active operations start as soon as V_{ST}≈1.38 V, i.e. on the UVLO signal V_{UVLO} falling edge. The latter phase can be easily recognized in the left part of Fig. 6 by the clipped sinusoids on PZ trace that extend their amplitude once SECE is started.

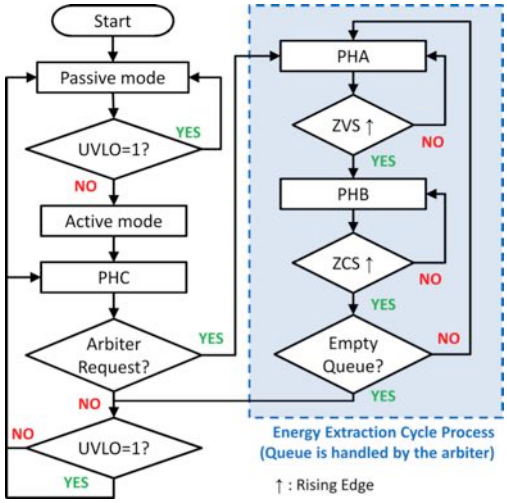

Fig. 5. Control flow-chart of the system.

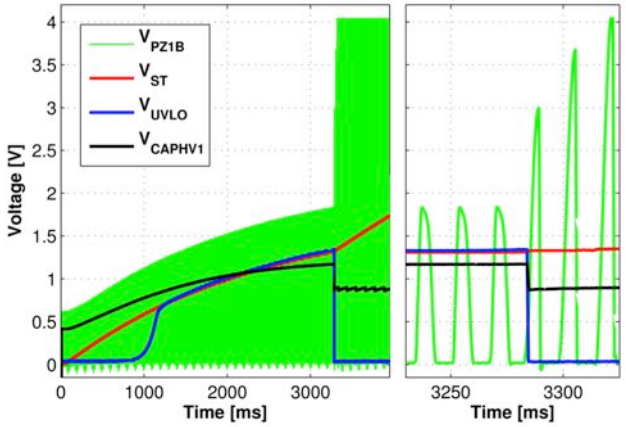

Fig. 6. (left) Start-up of the proposed converter from a zero energy state (V_{ST}=0 V) showing passive and active operating regimes and (right) close up during the transition. Waveforms are acquired from real transducers and a sample of the manufactured IC.

B. Energy-aware design of circuit blocks

1) Bias generator and UVLO

The generation of a stable nano-current reference is crucial for operations in the µW range. Fig. 7 shows the designed circuit diagram for the generation of I_{ref}, set to 16 nA. It is based on a classic supply independent current reference [51] but it is biased in the sub-threshold region and a cascode current mirror (M_{B1}, M_{B2}) has been added to increase the independence of I_{ref} with respect to the supply voltage V_{DD}. In this design R_{BS}=687 kΩ is an on-chip resistor. The bias generator circuit outputs the voltage references V_{biasP} and V_{biasN} which are used by all analog sub-circuit in the IC. Distributing reference voltage instead of reference currents for biasing allows the reduction of quiescent current required by biasing circuits down to 48 nA. The UVLO circuit diagram is shown on the right of Fig. 7. An hysteresis of about 100 mV is provided in order to prevent switching around V_{DDmin} value. The UVLO circuit draws 16 nA.

2) Nano-power comparators

Four different nano-power comparators (Fig. 8) with built-in hysteresis have been designed. They are all driven with the same tail current I_{bias}=I_{ref}=16 nA and they differ for the input common-mode V_{CM} voltage they can properly sense. Differently from other realizations [23],[40],[51], the inputs of comparators are placed on transistor gates in order to show a high impedance on the sensed nodes. Comparators (a) and (b) have nominal hysteresis V_{hyst} = 15 mV and (a) has been designed for sensing voltages up to the positive rail (V_{DD} +0.3 V, n-channel MOSFET input pair) whereas (b) can sense down to the negative rail (GND -0.3 V, p-channel MOSFET input pair). The same applies for comparators (c) and (d), used in DC interface circuits, which have hysteresis V_{hystDC} = 28 mV; furthermore, their tail current can be temporarily increased through a boost input signal (BoostC or $\overline{\text{BoostD}}$) of about 100 nA (exact values are shown in Table I) for reducing their propagation delay only when required. The comparators (a) and (b) do not have a dedicated boost input. They are used in the buck-boost converter core where a bias boost is provided at an higher level by directly increasing I_{bias} = I_{ref} = 16 nA to I_{bias} = 16I_{ref} = 256 nA.

TABLE I PROPAGATION DELAYS OF DESIGNED COMPARATOR WITH DIFFERENT BIASING OBTAINED FROM SIMULATION[1].

Comparator	t_{pdLH} [µs]	t_{pdHL} [µs]	Biasing
Standard N (a)	9.44	11.46	I_{biasA}=I_{ref}
Standard N (a)	0.74	0.76	I_{biasA}=16*I_{ref}
Standard P (b)	12.97	9.98	I_{biasB}=I_{ref}
Standard P (b)	0.86	0.78	I_{biasA}=16*I_{ref}
DC version N (c)	10.40	12.74	I_{biasC}=I_{ref}
DC version N (c)	1.34	2.02	I_{biasC}=7*I_{ref}
DC version P (d)	14.26	10.86	I_{biasD}=I_{ref}
DC version P (d)	1.59	1.19	I_{biasD}=7.66*I_{ref}

[1]Simulation including parasitic capacitances, with T=27 °C, V_{DD}=3 V, V_{CM}=V_{DD}/2, C_{load}=500 f

The hysteresis voltage V_{hyst} is the input voltage difference necessary to balance, in comparator (a), the drain currents of M_{N1}a and M_{N2a}. Propagation delays obtained from simulations are reported in Table I for different bias conditions.

3) Higher Supply

As an autonomous system, the converter relies only on harvested energy. Then, no stable and regulated voltage is available. However, since the IC manages many sources with different voltage levels, several circuit blocks including the gate drivers of MOSFETs require to be supplied or driven with the highest possible voltage in order to operate properly. Thus, a very frequently used block is the Higher Supply (HS) circuit, depicted in Fig. 9. The output V_{HH} is selected as the highest voltage among V_{HA}, V_{HB} and V_{DD}, with a current limit of 12I_{ref}. Transistors M_{h1} and M_{h2} form a standard bulk-regulation circuit, whereas $M_{h3...5}$ (which are low V_{GSth} transistors, V_{GSth}≈200 mV) and the current generator have been added to improve the output voltage level for very similar input voltages. Transistors M_{h3} and M_{h4}, which have a higher leakage current, have been sized with a trade-off between performance (i.e. V_{HH} voltage drop with respect to V_{HA} or V_{HB}) and leakage current in order to limit static current between V_{HA} and V_{HB} to few nA in worst bias conditions. Fig. 10 shows the improvement brought by the added circuitry in the limitation of the voltage drop on V_{HH} for crossing inputs. Transistors M_{h5} and the current generator are mainly useful for analog circuitry requiring low current (i.e. comparators) on slowly variable signals (e.g. PZ voltage).

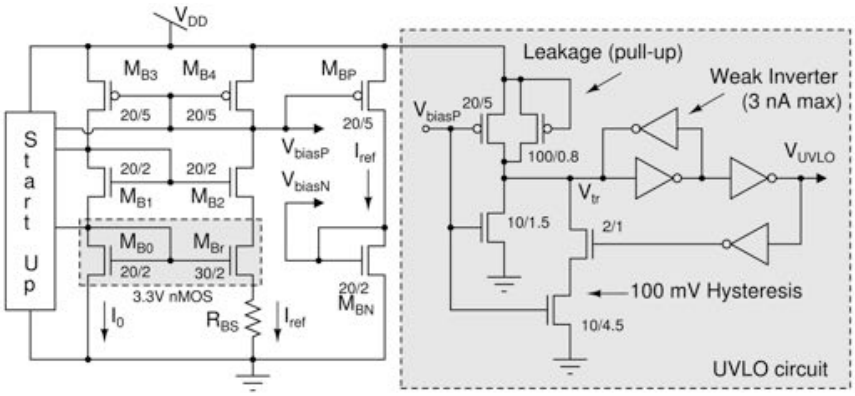

Fig. 7. Circuit diagram of the designed bias generation circuit (left) and of the UVLO circuit (right). The start-up block is used to prevent the undesired condition I_0 = I_{ref} = 0 A when V_{DD} rises. The start-up circuit does not draw any static current.

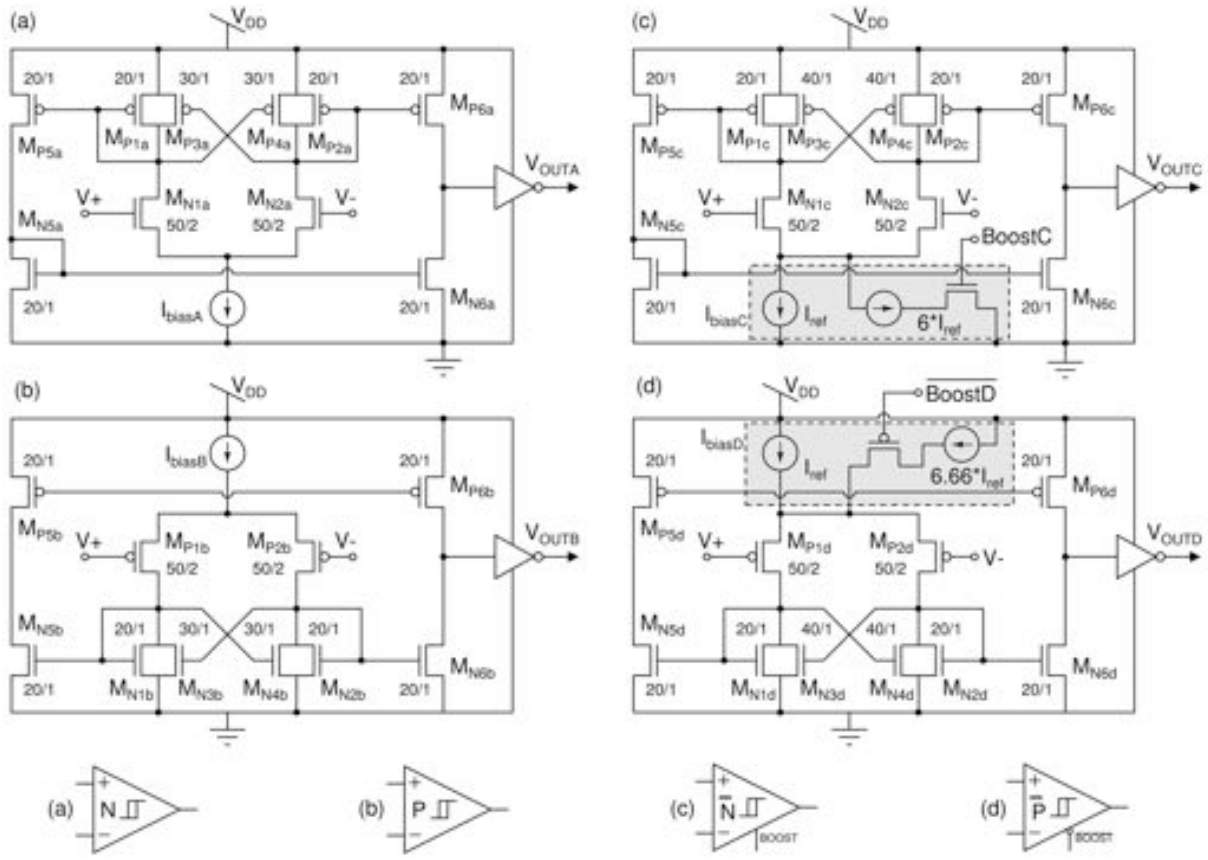

Fig. 8. Circuit diagram of the four comparators. (a) and (b) have V_{hyst}=15 mV and allow signals up to the positive and the negative rail, respectively. (c) and (d) have V_{hystDC}=28 mV, and allow signals up to the positive and the negative rail, respectively, and have an actively tail current boost for reducing propagation delay t_{PD} when required.

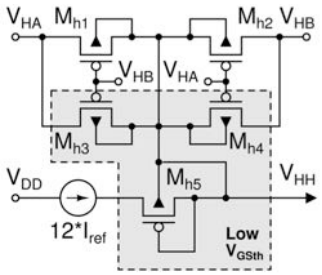

Fig. 9. Higher supply circuit schematic.

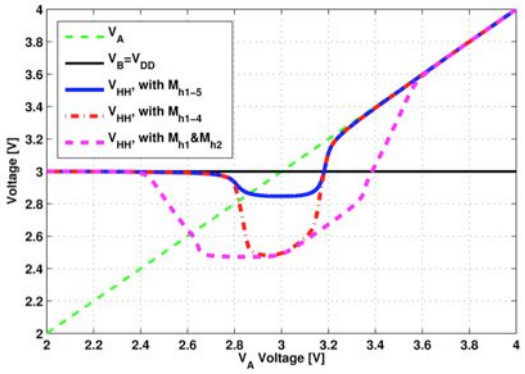

Fig. 10. Simulated output voltage V_{HH} of an HS circuit for V_A sweeping and V_B=V_{DD}=3 V for several configurations.

4) Enhanced NVC

The output voltage of a PZ is generally an AC signal with null average value requiring rectification. Negative voltage converters (NVC) have been already employed in this type of applications [26][52] thanks to their low-drop out, which is due only to the on-resistance of MOSFETs. However, alike standard rectifiers, they have a minimum input voltage (i.e. roughly corresponding to $V_{GS,th}$, typically 0.7 V), thus it is impossible to extract the whole charge on C_P. Moreover, an NVC is not able to force a current direction and cannot simply substitute a diode bridge. Fig. 11 shows the circuit diagram of the enhanced NVC (eNVC) circuit designed to overcome such limitation. Along a standard NVC core (M_{V0}-M_{V3}), four actively controlled switches (M_{Ve0}-M_{Ve3}) have been added. They are activated in pairs (by V_{AON} or V_{BON}) only during energy extraction phases ($V_{CONVACTIVE}$ signal is high) and allow the whole charge on C_P to be extracted (i.e. until V_{PZ}=0 V). The comparator CMP_{NVC} select which pair must be switched on by reading the polarity of V_{PZ} (V_{PZA} and V_{PZB}). The eNVC circuit draws 32 nA or 16 nA, depending on the output state of comparator CMP_{NVC} and thus, as the AC voltage of a PZ has as many positive half-waves as negative ones, an average of 24 nA can be considered in a realistic scenario.

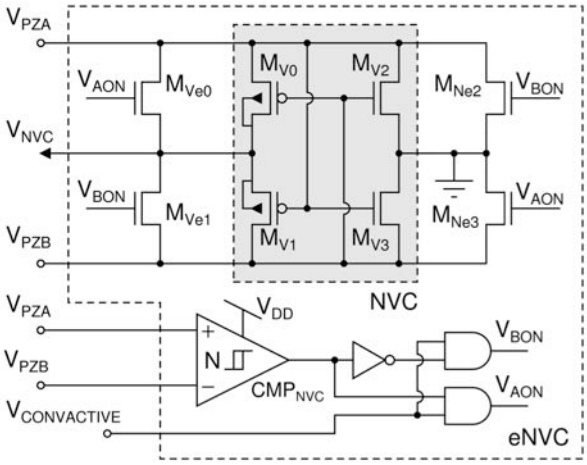

Fig. 11. Enhanced NVC circuit diagram.

5) Peak Detector

The SECE converter requires the tracking of $V_{PZ}(t)$ and the detection of maxima and minima in order to trigger energy extraction cycles. Fig. 12 shows the circuit diagram of the peak detector included in each PZ interface circuit. A design issue is the PZ voltage which can reach values significantly higher than V_{DD}. To overcome this issue, the supply voltage V_{HH} is selected as the highest between V_{NVC} and V_{DD} as described above. The first stage is composed by three diode connected transistors which produce V_{NVCds}, a down-shifted version of the input voltage V_{NVC} (i.e. the rectified version of V_{PZ}), and force it to be in the allowed common mode range (i.e. V_{HH}+0.3 V) of both the input pair M_{k1}-M_{k2} and the input pair of comparator CMP_K. The second stage generates V_{track} as a copy of V_{NVCds}. C_{track} can only be charged by M_{k6} and thus allows the comparator to detect a voltage maximum (peak) as soon as $V_{track}>V_{NVCds}+V_{hyst}$. The built-in comparator hysteresis increases the noise margin and prevents false triggering. The quiescent current drawn by the peak detector is 32 nA. Measurements showed that the circuit is able to track input signals up to 1 kHz which is a quite high frequency for macro-scale PZ and for typical vibrations in industrial or transportation environments [53]. In addition, it offers improved performance with respect to other discrete [12] and integrated implementations [54].

C. PZ-channel Interface Circuit

Fig. 13 shows the schematic of the interface for PZ. This block is replicated for each PZ input channel. The depletion-mode n-channel MOSFET driven by V_{pass} ensures the previously introduced battery-less start-up from discharged states. The first stage of the circuit interface is the enhanced NVC (eNVC) of Fig. 10. The PZ voltage is tracked by the peak detector (Fig. 12) which identifies the local maxima of $V_{NVC}(t)$, i.e. the peaks of $V_{PZ}(t)$, and feeds the control logic, which activates energy extraction on the involved channel by activating $V_{CONVACTIVE}$. In case of simultaneous requests of energy extraction cycles, the delay of the conversions due to the queuing introduced by the control logic has no significant impact on the amount of extracted energy because the duration

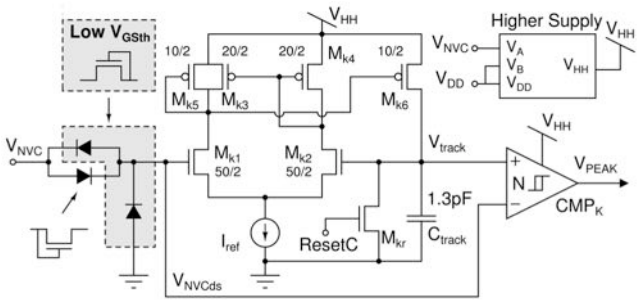

Fig. 12. Peak detector schematic circuit.

of each charge extraction is normally significantly shorter (i.e. less than 0.1%) than the PZ oscillation frequency.

When a conversion is started, phase PHA is applied (Fig. 2) by closing the M_{SP}-M_{SN} switch, so that C_P is discharged through L. The gate of M_{SP} requires a specific gate driver which performs a level shift on its digital control input, driven by the logic controller, from V_{DD} to the highest possible voltage among V_{DD}, V_{NVC} and V_{LX1}, in order to ensure that M_{SP} is completely turned off between energy extractions (phase PHC), so that no charge is transferred among sources. This is of utmost importance because the inductor terminal V_{LX1} is shared among all input channels. The gate of M_{SN} is driven at V_{DD} supply voltage level as M_{SN} carries most of the current when V_{NVC} is less than about 1 V.

One of the main challenges in the design of the converter was related to the huge number of variable voltage supplies for each channel and their sub-block, in particular regarding the gate drivers of the p-channel MOSFET switches. A remarkable care has been used in order to prevent activation of bulk diodes caused by variations of voltage supplies. Similarly, ESD protection devices on pad-ring have been connected to an internal floating rail with protections instead to V_{DD} (or V_{ST}). In this way the voltage of PZ and HV DC sources is allowed to swing at a voltage higher than V_{DD} (or V_{ST}) and preventing charge to flow to V_{DD}. Otherwise, efficiency (for PZ) and correct operations (for HV DC sources) would be compromised.

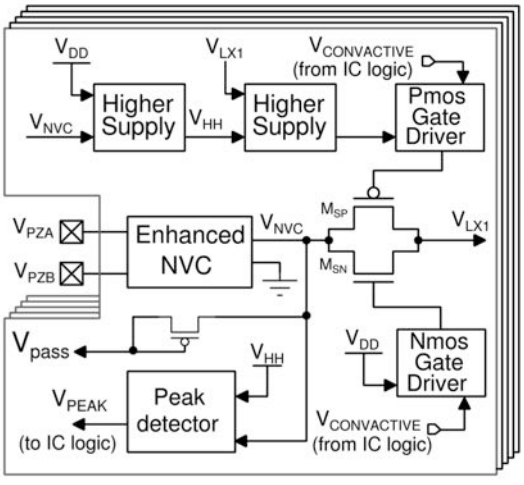

Fig. 13. PZ channel interface circuit diagram.

D. DC-channel Interface Circuit and MPPT Scheme

The main task of the interface circuit for a DC channel is the control of energy extraction from the transducer performing MPPT. The FOCV MPP technique requires a voltage reference $V_{FOCVref}$ obtained as a particular fraction of V_{DC} at open circuit (i.e. V_{DC0}). An external pin $V_{MPPconf}$ is tied to V_{DD} or ground in order to select a fraction of 50% or 75%. A sample and hold circuit has been designed for this purpose and is depicted in Fig. 14 V_{DC0} is sampled on C_S by closing S_{SAMP} for 2 µs. Then, the charge of C_S is shared with C_{H75} (or C_{H50} depending on $V_{MPPconf}$) by closing the switch S_{H75} (or S_{H50}) in order to set $V_{FOCVref}$ to the desired value. The value of C_S=3 pF has been chosen as a trade-off between charging time, in order to allow compatibility with high impedance sources, and both noise immunity and leakage, in order to reduce $V_{FOCVref}$ drift over time while maintaining an high MPPT accuracy. After C_S, the values C_{H75} = 1 pF and C_{H50} = 2 pF were chosen. $V_{FOCVref}$ is refreshed every eight energy extraction cycles in order to quickly track fluctuations on V_{DC0} and, at each refresh, C_{H50} and C_{H75} are discharged. The quiescent current of the reference circuit is only due to the leakage of transistors in the order of some pA. Differently from other MPPT schemes which can draw as much as 5 µW [2],[21], the implemented MPPT scheme offers a negligible power loss at the cost of a slightly lower accuracy on the MPP, resulting in an convenient trade-off for sources in the µW range.

The schematic of the interface circuit for a DC channel is depicted in Fig. 14 and is composed of a MPPT circuit for the generation of $V_{FOCVref}$, a comparator CMP_{DC} (which is, referring to Fig. 8, of type (d) for LV channels and of type (c) for HV channels), and an HS circuit (only for HV channels).The switches S_{CAP} and S_{CONV} are built exactly alike the switch connecting V_{NVC} and V_{LX1} (M_{SN} and M_{SP}) in Fig. 13. S_{CAP} is always closed except during the refresh operation of the threshold $V_{FOCVref}$. This allows the converter not to stop during the update of $V_{FOCVref}$. S_{CONV} is a normally open switch which is closed only during the phase PHA of an energy extraction cycle. Whenever V_{CAP} exceeds $V_{FOCVref}+\Delta V_{hystDC}$, CMP_{DC} activates power conversion (phase PHA), which is stopped when V_{CAP} drops below $V_{FOCVref}-\Delta V_{hystDC}$ (phase PHC). In order to reduce intrinsic consumption, only in phase PHA the associated CMP_{DC} tail current is boosted according to the comparator type by the control logic, increasing temporarily the speed of the comparator itself.

Like in the PZ interface circuit, the gate of p-channel MOSFET in the switches requires to be driven with the highest available voltage for an effective cut off, then HS circuits are implemented between V_{LX1}, V_{ST} and V_{CAP}.

The acquired waveforms from a LV DC source depicted in Fig. 15 show the periodic refresh of $V_{FOCVref}$ every 8 energy extractions and the amplitude of hysteresis ΔV_{hystDC}.

E. Buck-boost Converter

The buck-boost converter core (Fig. 16) has been carefully designed in order to minimize energy consumption per

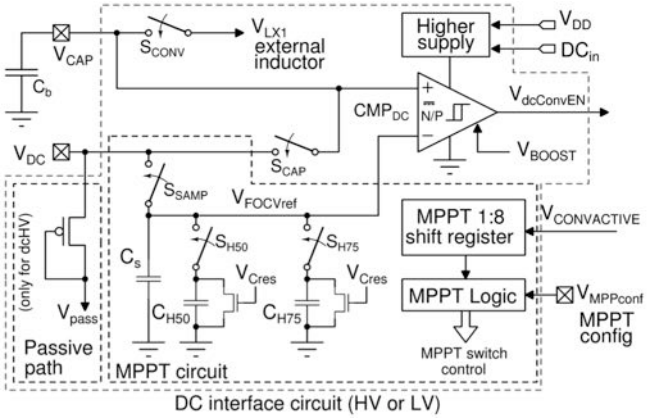

Fig. 14. MPP threshold generator circuit diagram.

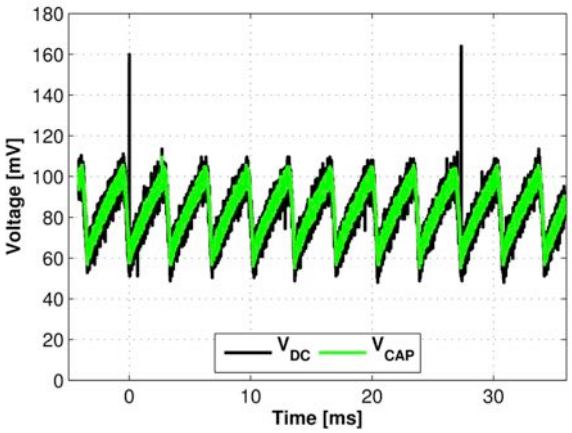

Fig. 15. Acquired waveforms on a LV-DC channel from a Micropelt MPG-D751 TEG chip heated with a fingertip at room temperature (V_{DC0}= 160 mV, C_{bL1}=22 µF) showing MPP tracking and the refresh of the MPP threshold $V_{FOCVref}$ every 8 energy extractions.

operation and to guarantee a robust system. The buck-boost core is shared with all the input channels and is mainly composed of an analog section, the switches with their respective drivers, and a logic controller implemented as a finite state machine (FSM). The three MOSFET switches of the buck-boost converter (M_{X1} , M_{X2} , M_{XA}) are sized to achieve a trade-off between dynamic power consumption and on-resistance, which affects conversion efficiency. Such switches are driven by the output signal of the FSM which marks the correct timings of each phase (PHC, PHA and PHB). The transition from state PHC to state PHA is determined by a start signal generated by the arbiter when an energy extraction cycle is requested by one of the sources. The analog section consists of two comparators (CMP_V, CMP_I) and a bias generator to dynamically increase the bias current of CMP_V, CMP_I in order to reduce their propagation delay. The bias generator has a full shutdown feature: no current is drawn by the buck-boost circuits when the converter is in idle (V_{biasON} signal high) state whereas the bias is set to $16I_{ref}$ during PHA and PHB (V_{biasON} signal low). This dynamic biasing policy offers on one hand a very low quiescent current and on the other hand a fast response time only when needed. In fact the propagation delay t_{pd} of CMP_V and CMP_I decreases, according to simulations, down to 0.74 µs and 0.78 µs

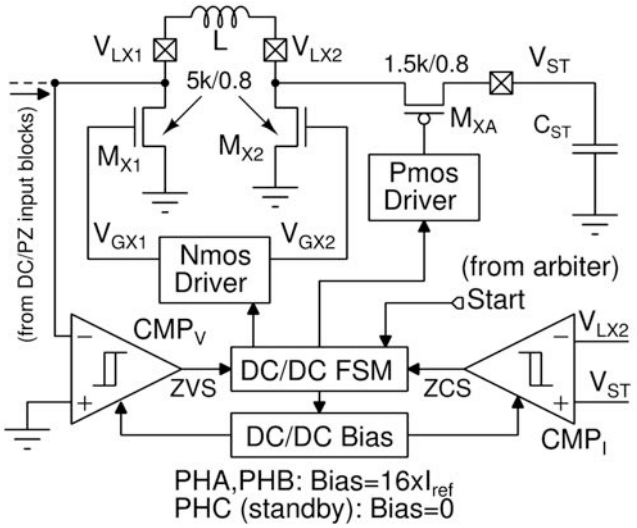

Fig. 16. Buck-boost core circuit diagram.

respectively (Table I). The analog section of the buck-boost core draws no current during PHC and draws 1.2 µA during PHA and PHB. However, PHC typically last longer than PHA and PHB and the system remains in idle state (PHC) whenever there is no energy to harvest.

The converter detects at run-time the end of both PHA and PHB, therefore the system is self-adapting to arbitrary energy transducers (i.e. C_P for PZ and R_S for DC), to the value of the chosen passive components (C_{ST}, L and all four buffer capacitors C_b of DC sources), and to the value of V_{ST} which affects the duration of PHB. The start of PHA is requested by individual input channel interfaces and granted by the control logic (according to the $V_{CONVactive}$ signal). The end of PHA and the contextual start of PHB happen on the zero-crossing of V_{LX1} by CMP_V (signal ZVS, Zero Voltage Switching) whereas the end of PHB is detected by CMP_I (signal ZCS, Zero Current Switching) when drain-source voltage of M_{XA} (V_{ST}-V_{LX2}), which is used as a current sense resistor, becomes lower than $-V_{hyst}$ (i.e. current is flowing from C_{ST} to GND trough the inductor L). Zero voltage and current detection implemented on custom microelectronic circuits grant a significant degree of flexibility at the expense of few tens nW. This represents a clear advantage over existing solutions where timings are statically determined [12].

The inductor L is kept shorted to ground in idle state for preventing false triggering of CMP_V and CMP_I, for dissipating possible unwanted residual energy on L without producing ringing on V_{LX1} and V_{LX2}, and for easing correct state detection on CMP_V and CMP_I for a new energy extraction. The switch M_{XA} is closed (i.e. the gate is driven to V_{ST}) directly from the logic controller through the set input of a D-type flip-flop. The output of CMP_I is used only for the detection of the opening condition and operates directly on the clear input of such flip-flop. Such designed control methodology prevents oscillation and multiple switchings of M_{XA} at the end of PHB which may lead to unstable operations and a worthless switching activity increasing dynamic power. A typical scenario for simultaneous energy extraction cycles is shown on the left of Fig. 17 where two PZ (Q220-A4-303YB from Piezo Systems with about 7 g tip mass, f=60 Hz and a_{RMS}=0.164g) have been stimulated through an electrodynamic shaker while a Micropelt MPG-D751 was heated with a fingertip (cold plate at room temperature). Waveforms were acquired with a digital oscilloscope. An additional measurement with a single PZ (with the same parameters from the previous measurement) has been performed in order to show waveforms and signals of the buck-boost core and the acquired data are shown on the right of Fig. 17.

F. *Arbiter design*

An important block of the system is the logic arbiter. It manages all nine channels and serializes the accesses to the buck-boost converter core. In case two or more sources concurrently request the execution of an energy extraction cycle, the arbiter chooses the one with the highest priority and creates a priority-based queue for the remaining requests. The priority has been selected at design stage with the PZ channels

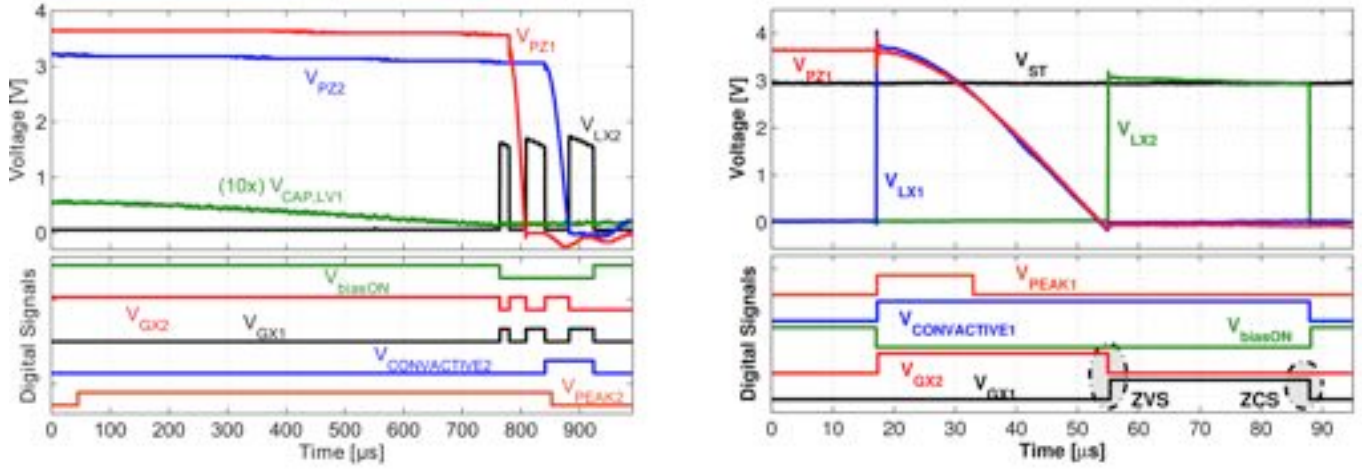

Fig. 17. (left) Example of acquired signals during simultaneous requests of energy extraction from a LV-DC channel and two PZ channels obtained from real transducers. (right) Waveforms and internal signals acquired during an energy extraction cycle from a PZ. ZVC and ZCS signals are not directly shown and their effect on the buck-boost converter is highlighted in gray ellipses (transitions from PHA to PHB due to ZVS and transition from PHB to PHC due to ZCS).

having higher priority over DC channels. Moreover, PZ on channel 1 has the highest priority over PZ, followed by channel 2, channel 3, and so on. A simplified diagram of the arbiter circuit is shown in Fig. 18.

The arbiter is composed of sub-arbiters which grant priority in this order: first the A channel, then B, and at last C. Sub-arbiters are sequential circuits with their internal memory (i.e. edge-triggered flip-flops) used to generate and store the queue. A combinational logic (i.e. chains of and gates) processes the state and the requests in order to select the most priority channel. The outputs of the sub-arbiters A_{out}, B_{out} and C_{out} are all '0' or mutually exclusive (e.g. if A_{out} is '1', B_{out} and C_{out} are '0') with the output corresponding to the chosen active channel set to '1'. If new requests arrive when another output is active, the sub-arbiter waits for the current selection to be completed before changing its state. Looking at the top-level arbiter, the structure of priorities is highlighted. Then, priority is wired in the circuit. The sub-arbiters communicates among them with a start-stop signaling.

Asynchronous logic is exploited in order to minimize energy consumption in both logic arbiter and logic controller, implementing a finite state machine (FSM) which handles the phases PHA, PHB and PHC.

The global reset signal $MASTER_{RESET}$ (Fig. 18) is used to reset all the logic at the transition between passive and active mode in order to avoid false triggering of energy extractions.

Clock-less digital circuits can exploit their maximum speed without the energy overhead necessary for clock signal generation and distribution, which can easily be quantified in some µW for a clock frequency of 125 kHz at a supply voltage of 3 V, corresponding to a low consumption scenario. An additional drawback of a clocked circuit would be the discretization of the converter switching times: low clock frequencies would consume less power but would lead to a loss of conversion efficiency because of timing inaccuracies.

The implemented logic does not provide information on the power levels of each source to external devices such as a microcontroller unit (MCU). However, for DC sources this could be implemented by: (i) providing the MPP voltage to an ADC of the MCU and (ii) by placing a counter for each channel and by incrementing it at every energy extraction. Then, through a communication interface, a MCU may read such values and their variations over time.

G. *Input power range*

The converter has been designed for energy harvesting applications with input power ranging from tens to hundreds of µW. Furthermore, the converter is designed to operate only in discontinuous conduction mode. However, the converter can work with higher power levels if some rules are respected.

The first and main limitation is the utilization factor D_L of the inductor defined in (1) as the fraction of time during which the inductor is in use:

$$D_L = \sum_{i=1}^{9} f_i \left(t_{PHA,i} + t_{PHB,i} \right) \le 1 \quad , \; i = 1,2,..,9 \tag{1}$$

In the above equation, $t_{PHA,i}$ and $t_{PHB,i}$ are the durations of phases PHA and PHB for the i-th source, and f_i is the number of energy extraction cycles per second. In a multi-source scenario, D_L must be evaluated in order to safely satisfy (1). In the following derivation, (2) and (3) assess t_{PHA} for PZ and DC sources respectively. Equation (4) determines t_{PHB} with the assumption that the inductor current is approximated to a ramp and no losses occur while transferring an energy packet E_{CY} from the inductor to the capacitor. A more accurate analytical analysis for SECE with PZ is provided in [38].

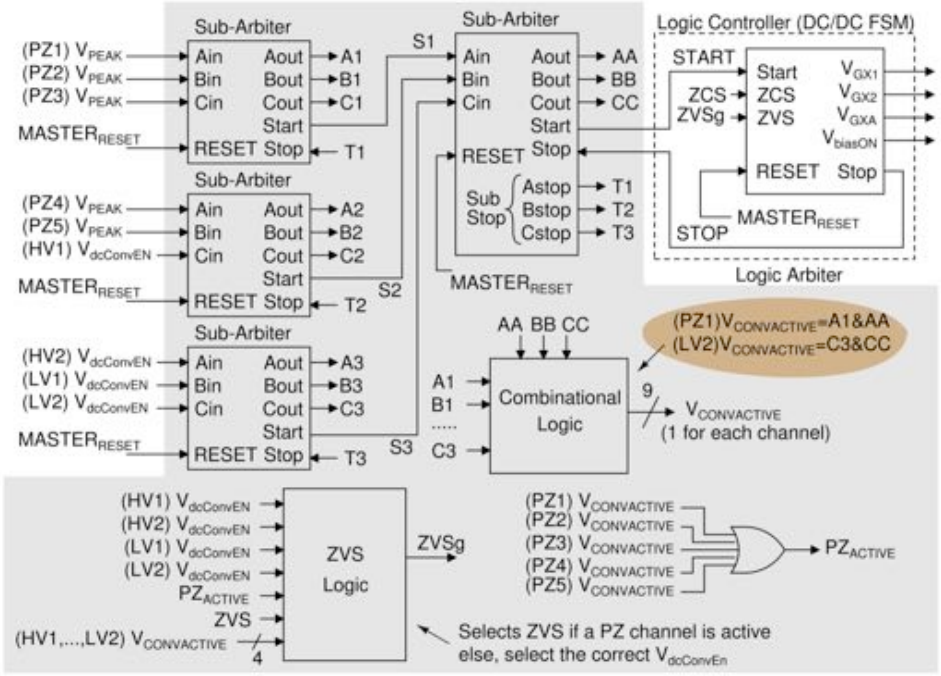

Fig. 18. Simplified schematic of the logic arbiter and logic controller (DC/DC FSM). For the sake of simplicity, the generation of $V_{CONVACTIVE}$ has been exemplified for two cases. The operations of the ZVS combinational logic is explained in the note.

$$t_{PHA,PZ} = \frac{\pi}{2}\sqrt{C_P L} \tag{2}$$

$$t_{PHA,DC} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{\beta V_{DC0}} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{V_{MPP}} \tag{3}$$

$$t_{PHB} = \sqrt{L}\frac{\sqrt{2E_{CY}}}{V_{ST}} \tag{4}$$

The PZ maximum input power is easily expressed by (5), where f_{PZ} is the vibration frequency and V_{PZ}=5 V is a circuit constraint. The resulting inductor duty cycle is shown in (6) in which t_{PHA} is given by (2).

$$P_{PZ\max} = 2f_{PZ}\overbrace{\frac{1}{2}C_P V_{PZ}^2}^{energy\ per\ cycle} \tag{5}$$

$$D_{L,PZ} = f_{PZ}\left(t_{PHA,PZ} + t_{PHB}\right) = f_{PZ}\left(\frac{\pi}{2} + \frac{V_{PZ}}{V_{ST}}\right)\sqrt{C_P L} \tag{6}$$

The same is applied to DC sources and results are shown in (7) and (8), in which f_{DC} is the switching frequency (i.e. the number of energy extraction per second, which depends on input power).

$$P_{DC\max} = f_{DC}\overbrace{2C_b V_{MPP}\Delta V_{hystDC}}^{energy\ per\ cycle} \tag{7}$$

$$D_{L,DC} = 2f_{DC}\frac{V_{ST}+V_{MPP}}{V_{ST}V_{MPP}}\sqrt{V_{MPP}\Delta V_{hystDC}}\sqrt{C_b L} \tag{8}$$

From the above equations, a graph showing the maximum input power for a single source is provided in Fig. 19 for the chosen 10 mH inductor (Murata 1410604) in several configurations: (a) PZ with C_P=52 nF with V_{PZ}=5 V; (b) LV source with V_{MPP}= 0.75V_{DC0}, V_{DC0}=1 V and C_b=150 µF; (c) LV source with V_{MPP}= 0.50V_{DC0}, V_{DC0}=1 V and C_b=120 µF; (d) HV source with V_{MPP}= 0.75V_{DC0}, V_{DC0}=5 V and C_b=180 µF; (e) HV source with V_{MPP}= 0.50V_{DC0}, V_{DC0}=5 V and C_b=180 µF. All the above configurations have D_L=0.9.

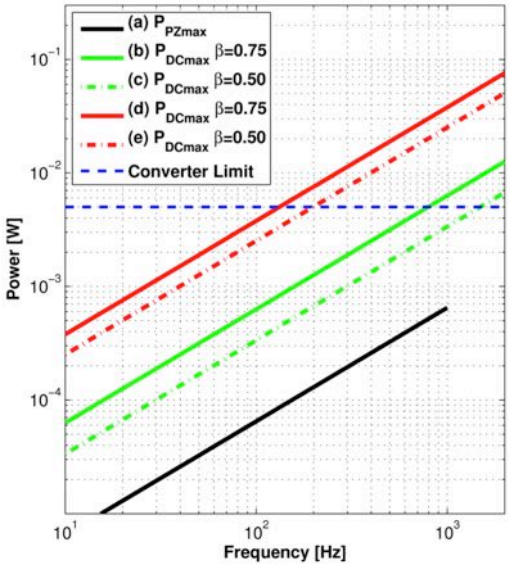

Fig. 19. Graph showing the theoretical maximum input power that can be handled by the converter operating with a single source.

However, the internal switches (with the exclusion of M_{X1} and M_{X2} in Fig. 16 with R_{DSon}=0.8 Ω) have not been sized for currents of hundreds of mA. Then, because of their resistance, the maximum input power is limited to about 5 mW. This limitation descends from the S_{CONV} switch in

Fig. 14. For DC input power above 5 mW, the current in the resonant circuit L-C_b would lead transistors in S_{CONV} to saturation, preventing correct energy transfer and, in the end, the functionality of the converter. The intrinsic efficiency of converter remains almost the same in the µW to mW range because the energy transfers are performed with resonant circuits with a constant quality factor. In addition, an increased input power in the mW range makes the IC consumption even more negligible and therefore an increase of efficiency is expected. Furthermore, the heat generated by losses on switches is not an issue for input power of some mW, even if the package has a very high thermal resistance.

IV. Experimental Results

The proposed heterogeneous multi-source converter has been designed and fabricated in a 0.32 µm BCD technology from STMicroelectronics. A micrograph is shown in Fig. 20, and the die measures 2142 µm on each side with an overall area of about 4.6 mm^2.

A functional test setup with the converter test board, two Q220-A4-303YB transducers from Piezo Systems with 7 g tip masses, an Ixys KXOB22-01X8 PV cell and a Micropelt MPG-D751 TEG is shown on the left of Fig. 21. On the right of Fig. 21, waveforms of acquired input voltages are shown with a forced external load consuming 40.5 µW (13.4 µA at V_{ST}=3 V) with the following input conditions applied: a fingertip heating the TEG at room temperature, typical indoor office illumination and the PZ driven with an acceleration with a_{RMS}= 0.2g at 60 Hz.

An additional performed measurement is the quiescent current I_{DDq} of the converter. The IC was supplied with an external voltage provided by a Keithley 2601 SMU, which also measured the corresponding drawn current. Two cases have been evaluated in order to account for the different possible sign of PZ voltage V_{PZ}, which has been forced as

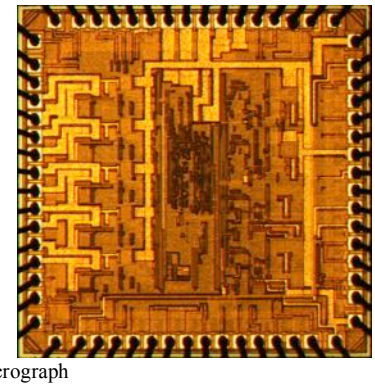

Fig. 20. Die micrograph

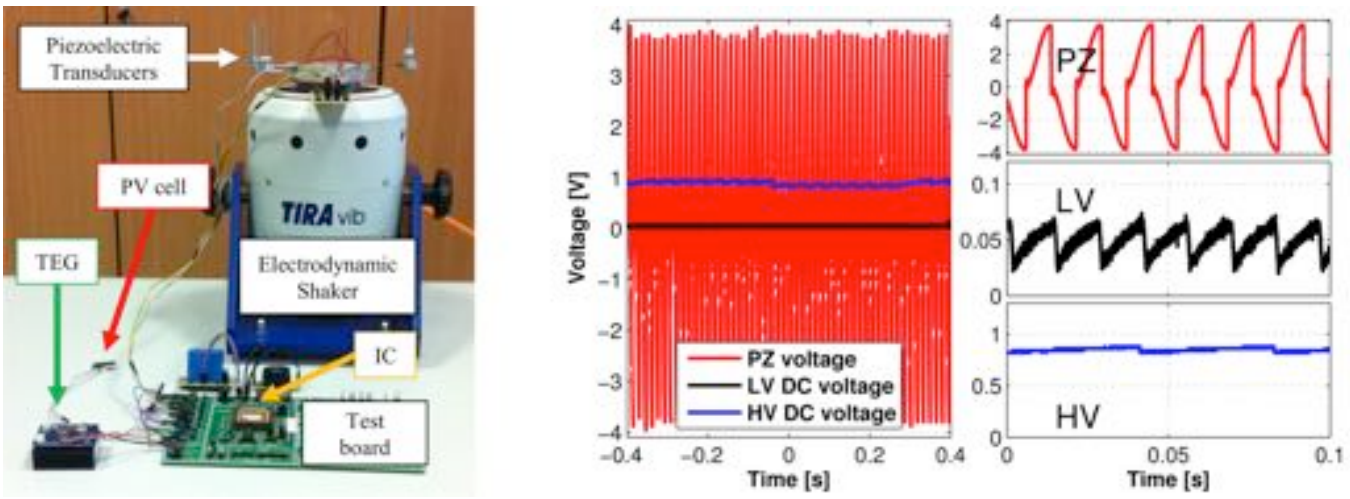

Fig. 21. (left) Setup for functional tests and (right) acquired waveforms showing: MPPT on the DC HV and LV channels and the sliced sinusoid resulting from SECE from a PZ.

$V_{PZ} = \pm 1$ V externally and $V_{DC} = 1$ V for HV DC inputs while $V_{DC} = 1$ V for LV DC inputs. The results, obtained on a fabricated device, are shown on top of Fig. 22 and point out an overall value of 431 nA, at V_{DD}=V_{ST}=3 V, corresponding to an average value of 47.9 nA per source. This remarkable result of 143.7 nW of static power per source is of vital importance in self-supplied energy-limited applications and is considerably lower with respect to other ICs for harvesting [40],[55] which have a static consumption for a single source of about 1.5 µW. The generated I_{ref} is inferred from obtained data and is compared with simulations on bottom of Fig. 22, in which a satisfactory matching is observed. However, I_{ref} exhibits a stronger dependence on V_{DD} than expected.

The converter is able to operate without a pre-charged energy reservoir as illustrated in Fig. 6 and therefore is suitable for battery-less applications. The minimum V_{ST} for active operation is $V_{ST} \geq 1.38$ V. Hence, because of the internal diodes at least one of the PZ and HV sources should provide a voltage higher than 1.65 V. Once the system switches to active operation such value is decreased down to about 0.7 V for PZ and 1 V for HV DC sources, while the lower limit for LV sources is about 60 mV, mainly due to the intrinsic ±28 mV hysteresis of the comparator in their interface circuit.

A third experiment has been performed in order to assess converter efficiency η as the ratio between the power output on V_{ST} pin (i.e. power drawn from load, emulated with a Keithley 2601 SMU, and self-consumption from V_{DD} pin) and analytical input power. Fig. 23 shows the obtained efficiency for single source operation. The PZ was emulated with a $V_{PZ} = 4.42$ V peak voltage sinusoid on a $C_P = 47.7$ nF at $f_{PZ} = 64$ Hz, corresponding to a Q220-A4-303YB with a 7 g tip mass stimulated at 64 Hz with $a_{RMS} = 0.164g$. The HV-DC source has been emulated with $V_{DC0} = 2.7$ V and $R_S = 32.9$ kΩ to imitate a Sanyo AM1407 solar cell in standard laboratory light (about 300 lux), whereas the LV-DC source has been emulated with $V_{DC0} = 330$ mV and $R_S = 264$ Ω to simulate a Micropelt MPG-D751 TEG chip at room temperature with a thermal gradient of approximately 3 °C. Input power has been calculated with (5) and (7) as 59 µW for PZ, 55 µW for HV-DC, and 101 µW for LV-DC. The external components used in the setup are: $C_{ST} = 66$ µF, $L = 10$ mH, $C_{bHV1} = 2.7$ µF and $C_{bLV} = 22$ µF. The leakage of C_{ST} was found to be < 1 nA and therefore has not been considered.

The energy absorbed by the IC in the aforementioned conditions has been measured by connecting a shunt resistor on the V_{DD} pin and by subtracting I_{DDq} from the resulting average current. The corresponding power was divided by the conversion frequency. The resulting energy consumption E_{cycle} per energy extraction is illustrated in Fig. 24 for each channel. The data show that the energy spent for an energy extraction cycle is only a small part of the available energy. In particular, in the tested scenario and in the worst condition ($V_{DD} = V_{ST} = 5$ V) the IC uses only the 2.36%, 2.75% and 2.48% of the energy per extraction cycle available respectively from PZ, HV-DC and LV-DC. Moreover, the energy usage follows a quadratic law, and then the amount of energy

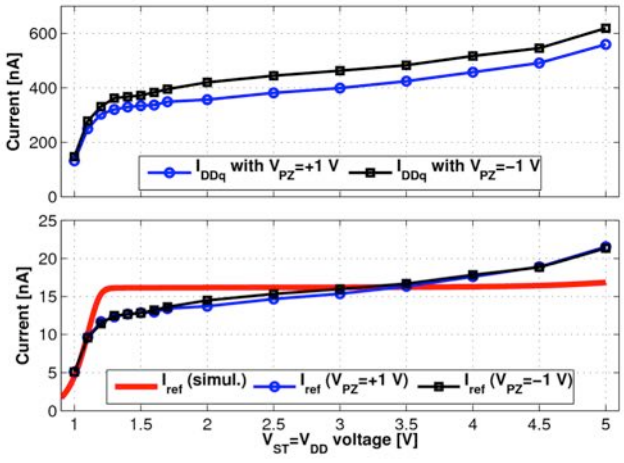

Fig. 22. (top) Quiescent current I_{DDq} drawn by the IC in an idle state (no conversions are performed) with PZ inputs polarized with +1 V or -1V and $V_{DC} = 1$ V for HV DC inputs while $V_{DC} = 1$ V for LV DC inputs (bottom) Comparison between inferred and simulated I_{ref}.

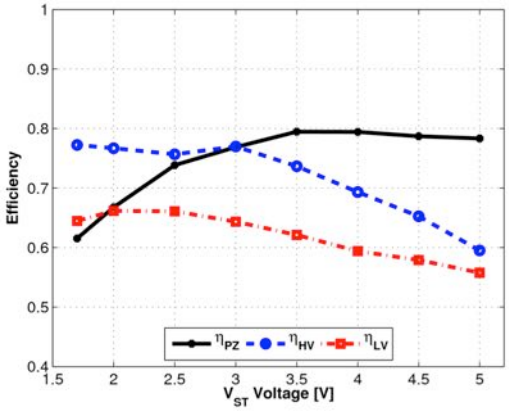

Fig. 23. Efficiency of the converter for each input channel type.

consumed at $V_{DD} = V_{ST} = 3$ V is even lower: 0.38%, 0.78% and 0.58% respectively. A comparison of energy consumption, losses and usable harvested energy is illustrated in Fig. 25.

The efficiency of the converter and its energy consumption have been investigated for other input configurations. Fig. 26 shows the obtained efficiency results for the converter operating with a single channel, PZ, DC HV and DC LV respectively and for the converter consumption during such measures. The used set-up is the same used in previous experiments with emulated sources and parameters and external components are listed in Fig. 26. The graphs show that the efficiency is in substantial agreement with Fig. 23 and variations are mainly due to variations of source characteristics (input power, frequency). The peak efficiency for PZ is 89.6% with input power ranging from 6.9 µW to 111 µW, 81% for HV DC channels with input power ranging from 30 µW to 122 µW, and 63.8% for LV DC channels with input power ranging from 21 µW to 116 µW.

The measurements on dynamic power absorbed by the converter are consistent for all the configurations. For example the energy used by the converter for a single energy extraction from a PZ agrees with data in Fig. 24 ($E_{cycle} \cong 12$ nJ at $V_{ST} = 5$ V, and $E_{cycle} \cong 5$ nJ at $V_{ST} = 5$ V). The same holds for DC channels (for example in LV channels $E_{cycle} \cong 4.5$ nJ at V_{ST}=5 V, and $E_{cycle} \cong 2$ nJ at $V_{ST} = 4$ V).

The nano-power design of the IC allows very weak source to supply and keep fully-functional the converter. The minimum required power, once the converter has switched to active-mode, was found to be about 3 µW with the above mentioned transducers. In a non-optimal case the converter can be supplied by a single PZ (Q220-A4-303YB PZ from Piezo Systems) driven at 60 Hz with an acceleration a_{rms}=0.04g with a 7g tip mass or, similarly, with a Micropelt MPG-D751 TEG chip with less than 1 K between its plates (generating V_{DC0}=60 mV). In an further measurement, a stable working condition at $V_{ST} = 1.5$ V, using the previously reported external components (C_{bLV}=22 µF, C_{ST}=33 µF, L=10 mH), was achieved with a drawn power of 0.77 µW by emulating a LV DC source with V_{DC0}=400 mV and R_S=52 kΩ which represents the minimum input power for a single source to keep the converter active.

The maximum power capabilities of the IC have also been investigated experimentally. By emulating a LV DC source with $V_{DC0} = 850$ mV and $R_S = 55.1$ Ω, which results in an input power of 3.275 mW, the converter was able to output 2.124 mW at V_{ST}=3 V with a 64.8% efficiency. The obtained efficiency agrees with the values in Fig. 23. The measurement was carried out with C_b=69 µF, the frequency of energy extraction was 1540 Hz and the duty-cycle D_L of the inductor was about 93%.

The obtained results highlight two main causes for energy loss: resistivity and back-current in the inductor. The first issue depends on the resistance of the inductor L and on the sizing of all the integrated switches in the IC, for which a die area constraint applies. The second issue is due to delays in detecting the zero current condition in L (i.e. the end of phase PHB) and could be partially mitigated by increasing the tail current of comparator CMP_I in the buck-boost core. Future work may consider the optimization of switch sizing in order to reduce their on-resistance at the cost of a larger die area.

Table II summarizes the obtained results, which are compared to the other realizations of integrated converters for energy harvesting applications.

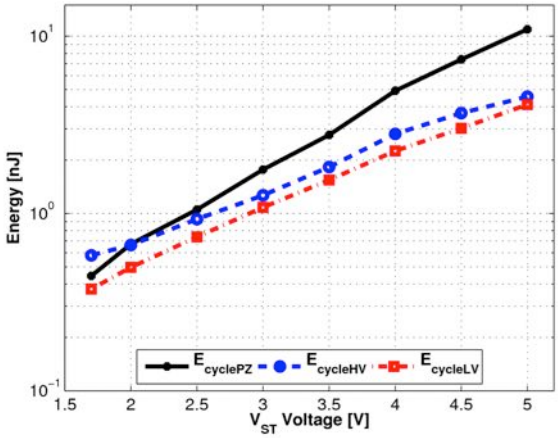

Fig. 24. Energy consumed during a single energy conversion.

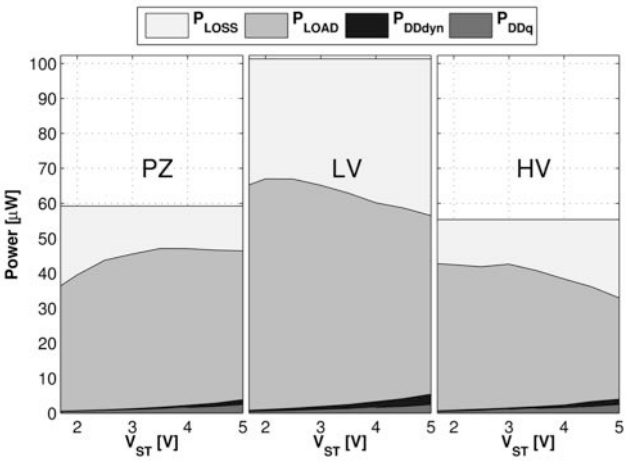

Fig. 25. Break-down of all contributions of the power conversion process for PZ, HV and LV DC sources. P_{DDq} is the static power of the converter due to I_{DDq}, P_{DDdyn} is the dynamic power associated to energy extraction cycles, P_{LOAD} is the net output power, and P_{LOSS} is the power lost in the conversion process.

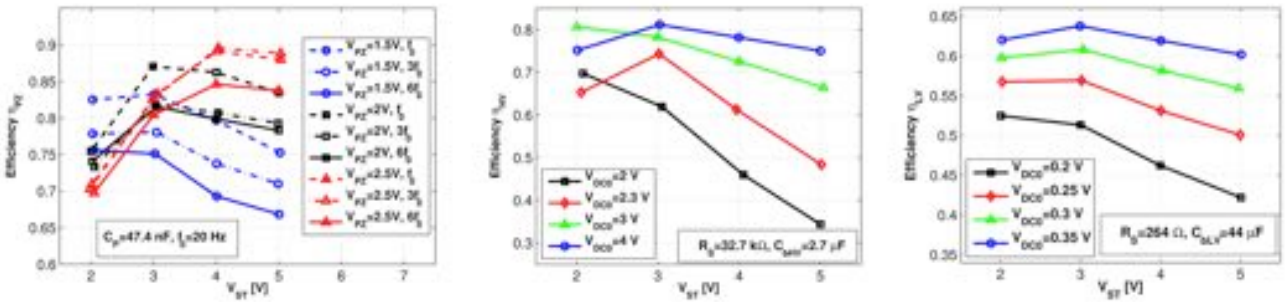

Fig. 26. Measured efficiency and current absorbed for different input configurations: (left) single PZ, (center) single HV DC, (right) single LV DC.

TABLE II. COMPARISON OF MULTI-SOURCE INTEGRATED CONVERTER FOR ENERGY HARVESTING.

Parameter	[27]	[21]	This work
Technology	0.35 µm HV CMOS 0.8 µm SOI	0.35 µm CMOS	0.32 µm BCD
Input channels	2	3	9
Type of sources	PZ, TEG	Piezoelectric, TEG, PV	Piezoelectric, TEG, PV, RF
Voltage Range	≥4 V	PZ: 1.5-5 V TEG: 0.02-0.16 V PV: 0.15-0.75 V	PZ: 0.7-5 V LV: 0.1-1 V HV: 1-5 V
Converter type	Rectifier + LDO	Switching	Switching
Peak Efficiency	66 %	83 %	89.6 %
Quiescent current	300 nA	1.5 µA (5µW at 3.3 V)	431 nA
MPPT type	n.a.	Hill-Climbing	FOCV (DC), SECE (PZ)
Maximum Output Voltage	> 4 V (2.4 V regulated)	3.3 V	5 V
Maximum Output Power	n.a.	2.5 mW	2.12 mW

V. CONCLUSIONS

An integrated converter for energy harvesting from multiple and heterogeneous sources has been designed and diffused in a 0.32 µm BCD technology from STMicroelectronics. The extreme low quiescent current, experimentally determined as 431 nA corresponding to 47.9 nA per source, allows the system to effectively exploit power sources down to 0.77 µW. The converter features a peak conversion efficiency of 89.6%, achieved in single source operating mode. Nonetheless, efficiency is increased in multi-source operation because the impact of power consumption of common circuital block is shared among multiple sources. In perspective, miniaturized energy autonomous systems can be implemented as in [56], due also to the availability of passive components, energy storage elements [57] and energy transducers [58],[59] in footprints of a few mm^2.

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Michele Dini received the B.S. and M.S. degrees in electrical engineering from the University of Bologna, Cesena, Italy, in 2008 and 2011 respectively. Since 2012, he has been working towards his Ph.D. degree in electrical engineering at the Advanced Research Center on Electronic Systems and at the Department of Electrical, Electronic, and Information Engineering of the same university. He has been involved with energy harvesting systems, design of CMOS power converters and power management circuits.

Aldo Romani received the Dr.Eng. degree in electrical engineering and Ph.D. degree in electrical engineering, computer science, and telecommunications from the University of Bologna, Bologna, Italy, in 2001 and 2005, respectively. In 2008, he joined the University of Bologna, Cesena, Italy, as an Assistant Professor. He has authored or coauthored more than 40 international scientific publications. He has been involved with CMOS integrated sensors, applications of piezoelectric materials, and energy harvesting systems. Dr. Romani was a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference.

Matteo Filippi received the degree in electrical engineering in 2011 from the University of Bologna, Cesena, Italy. Since 2012, he has been with the Advanced Research Center on Electronic Systems and with the Department of Electrical, Electronic, and Information Engineering, University of Bologna, Cesena, Italy, where he has been involved in energy harvesting systems, micropower electronics, and CMOS design.

Valeria Bottarel: not available.

Giulio Ricotti: not available.

Marco Tartagni (M'98) received the M.S. degree in electrical engineering in 1988 and the Ph.D. degree in electrical engineering and computer Sciences in 1993 both from the University of Bologna, Bologna, Italy. In 1994, he joined the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA, USA, as a Research Fellow. Since March 1995, he has been with the Department of Electronics, University of Bologna, where he is currently an Associate Professor. In 1997, he designed the first silicon-only fingerprint capacitive sensor. In 1999, he co-founded the company Silicon Biosystems active in the field of lab-on-a-chip devices. From 2005 to 2008, he was an European coordinator of FP6 Receptronics in the Nanotechnology thematic area. Since 2008, he has been a coordinator of the Working Group on Energy Autonomous Systems within the European CATRENE initiative. Since 2014, he has been a Member of the Scientific Board and Team Leader of the joint STMicroelectronics and Bologna University lab for sensor design. He has coauthored more than 100 refereed scientific publications, 18 granted U.S. patents, and 11 European and WIPO patents. Prof. Tartagni was a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference.