A Nanocurrent Power Management IC for Low-Voltage Energy Harvesting Sources

A Nano-Current Power Management IC for Low Voltage Energy Harvesting Sources

Michele Dini, Aldo Romani, Matteo Filippi, and Marco Tartagni, *Member, IEEE*

***Abstract*— This paper presents the nanopower design of an integrated 1 µW-to-5 mW power management circuit. The circuit integrates a boost converter with maximum power point tracking, a low drop-out voltage regulator (LDO), and a start-up circuit for battery-less activation from discharged states. The IC implements a dynamic two-way power routing policy that ensures a fast start-up from discharged states even with very large energy storage capacitors. In order to reduce the intrinsic power, asynchronous control logic was adopted. The circuit was implemented in a STMicroelectronics 0.32 µm microelectronic technology. The power conversion section and the LDO draw respectively stand-by currents of 121 nA and 414 nA in the active modes. The circuit achieves a peak conversion efficiency of 77.1% and a minimum start-up voltage of 223 mV.**

***Index Terms*—energy harvesting, nano-power circuits, DC/DC conversion, MPPT, photovoltaic, power management, RF harvesting.**

I. Introduction

ACCORDING to a widely diffused vision of the future of information technology, portable electronic devices are soon expected to scavenge the power required for operating from their surrounding environment. The most frequently envisaged applications include monitoring of physiological parameters [1], long-term environmental sensing [2], structural health monitoring [3][4], and industrial automation [5]. At present, most portable devices rely on electrochemical cells, and the potential of energy harvesting is still far from being fully deployed. One of the main hurdles is the difficulty of achieving a positive power budget, especially in size-constrained systems. Since energy transducers and materials deliver limited power densities down to few µW/cm^2 [6], the available power is reduced as system geometries shrink. On the other hand, the baseline system consumption is set by the intrinsic consumption of the power converter and by the stand-by consumption of application circuits. In fact, in order to harvest as much energy as possible, the power converter should always be enabled. In addition, even if arbitrarily low duty-cycles of activation may significantly decrease the power consumed by application circuits, system stand-by or sleep modes should at least be sustained. It is also worth to mention that in micropower harvesting applications an additional problem to deal with is battery-less circuit startup from fully discharged states when source voltages are lower than the minimum supply voltage of the power conversion control circuits. Until recently, a successful exploitation of micropower and nanopower sources has been prevented by the significantly higher intrinsic consumption of power conversion and management circuits. However, a new trend of reductions of such intrinsic consumption has started, with the additional goal of defining trade-offs with power conversion efficiency.

In the context of intrinsic power reductions, solutions based on discrete electronics components have been proposed. However, in order to achieve a positive power budget, this type of solutions typically requires input power in the order of tens of microwatts. A power management system for RF energy harvesting based on discrete components and an ultra-low power microcontroller unit (MCU) was reported in [7], where maximum power point tracking (MPPT) was performed with internal peripherals such as analog-to-digital converters and timers. A similar solution implementing a fractional open-circuit voltage (FOCV) MPPT technique is reported in [8]. In both cases the minimum required input power was about 10 µW. Furthermore, in the same application field, a discrete and self-powered resonant DC/DC converter based on coupled coils demonstrated operation with voltages as low as 100 mV and input power levels below 4 µW [9]. However, resonant converters do not achieve MPPT over a wide range of input conditions. Very low power consumptions are also achieved by piezoelectric energy harvesting circuits based on synchronized-switch techniques [10], mainly due to the very low activation rates of the switching converter in the range of tens of hertz typically. The lowest reported intrinsic consumptions for discrete implementations are lower than 3 µW [11][12].

In order to break the µW barrier, it becomes essential to exploit the very low parasitics offered by modern microelectronic processes, along with the development of specific nanopower circuit design techniques. Many integrated power converters tailored for different types of energy transducers have been reported in literature. As an example, in [13][14] an integrated power management circuit for DC sources is reported to consume 330 nA with the ability of handling battery charging and cold startup from input voltages

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Michele Dini, Aldo Romani, Matteo Filippi, and Marco Tartagni are with the Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" of University of Bologna, Cesena, Italy. (e-mail: michele.dini3@unibo.it, aldo.romani@unibo.it, matteo.filippi6@unibo.it, marco.tartagni@unibo.it).

TABLE I
RECENT NANOPOWER ICS FOR ENERGY HARVESTING APPLICATIONS

Work	Type of sources	Type of converter	Additional Features	Quiescent current/power	Minimum input power	Efficiency	Input voltage range
[17]	RF	Buck	MPPT with on-off time regulation, V_{OUT} regulated with APL comparator	181 nA	n.a.	< 95%	1.2-2.5 V
[19]	DC	Charge pump	Dynamic body bias, adaptive dead time	< 0.5 µW	n.a.	34%/72% at 0.18V/0.45V	> 0.15 V
[13]	DC	Boost	FOCV MPPT, battery charger, cold start-up	330 nA	5 µW	38%/>80% at 0.1 V/5 V	80 mV – 3 V (330 mV startup)
[23]	Thermoelectric	Boost	Variation-tolerant FOCV MPPT, no output voltage regulation, battery required	n.a.	n.a.	72%	70-600 mV
[27]	PV	Boost	On-chip PV cell, double-boost converter	n.a.	1 µW	65 %	> 0.5 V
[29]	PV	Battery Charger	Reconfigurable circuit power and speed	390 nW	n.a.	90 %	0.9-2 V
[16]	Thermoelectric, PV, piezoelectric	Boost converter	Single shared inductor with asynchronous arbiter logic	431 nA (9 sources)	3 µW	89.6 %	< 5.5 V (1.65 V startup)
This work	DC	Boost converter	Asynchronous control logic, fast battery-less startup, nanopower LDO, active 223 mV start-up circuit	121 nA	935 nW	77.1 %	74 mV- 2.5 V (223 mV startup)

n.a. = data not available

down to 300 mV. Other solutions with comparable power consumption and able to deal with multiple types of transducers are reported in [15][16]. In all the above cases, boost switching power conversion was adopted, and FOCV MPPT was assumed to be a good compromise between converted and consumed power. An alternative buck switching converter with dynamic on-off time calibration and a regulated output voltage was reported to consume 217 nW [17]. However, differently from boost converters, buck topologies are not suitable for long-term energy accumulation because of the intrinsically limited voltage achievable on the output capacitor. Other types of power converter circuits based on inductor-less charge pumps [18] have also been proposed with comparable intrinsic consumption and lower activation voltages down to 150 mV [19]. However, the efficiency of charge pumps is typically lower than that of switching converters, and reaches values up to 72% in the latter case. Lower activation voltages have been obtained by exploiting low-threshold MOSFETs for implementing multiple-stage boost converters [20] or advanced charge pumps [21][22]. The problem of activation voltage is particularly relevant in thermoelectric energy harvesting, as the TEG voltage can be as low as some tens of mV. However, once the converter has started, e.g. with an application specific cold start circuit as in [13] or with the use of a charged battery as in [23], the input operating voltage can be considerably lowered as long as the power budget remains positive. For input voltages lower than 100 mV, solutions based on step-up oscillators have been reported in literature [24]–[26].

Another possibility offered by the use of microelectronic substrates is on-chip photovoltaic generation with integrated photodiodes [27][28]. In this case, a power converter circuit should manage source voltages as low as few hundreds mV and power levels up to tens of µW. A nanowire solar cells power battery charger with reconfigurable circuit power and clock speed has been presented in [29]. Table I summarizes the main properties of recent state-of-the-art power conversion and management ICs.

Besides power conversion, a power management circuit should perform other important tasks such as providing stable regulated voltages to the output, implementing policies for power storage and distribution, managing cold start-up from low input voltages in battery-less systems, or handling battery charging [13].

This paper presents the nano-power design of a power management IC implemented in a 0.32 µm microelectronic process and the techniques adopted for extreme reduction of intrinsic power. The IC targets battery-less applications and is able to manage DC power sources lower than 1 µW thanks to an energy-aware circuit design with nano-power circuit blocks. Furthermore, it can self-start from sub-threshold voltages as low as 223 mV, which is a particularly important feature in consideration of the output voltages of many energy harvesting sources. Single PV cells/photodiodes have output voltages of some hundreds of mV in indoor environments (e.g. a BPW34 photodiode has an open circuit voltage of 268 mV in typical office light), and similar values can be obtained from RF rectennas [8], or from TEGs like [30] with small temperature gradients in the order of 1-2 K. The bootstrap circuit is based on a capacitive charge pump. Power conversion relies on a boost converter with FOCV MPPT. The circuit also implements a dynamic power routing policy that ensures a very fast startup from discharged states even in presence of large buffer capacitors. All control logic is asynchronous and does not require continuously running clock oscillators. Additionally, the IC also provides a selectable regulated output voltage with a nano-power low-drop out regulator (LDO) circuit. The proposed IC integrates all the necessary blocks for implementing a fully autonomous application based on energy harvesting applications, and requires a very limited number of external passives.

This paper will focus on the adopted nano-power circuit design techniques, and will describe the trade-offs between efficiency and intrinsic power. With respect to other similar implementations in literature, as it will be shown later on, the presented IC adopts different circuit topologies, and implements alternative policies for power management and self-powering. As a first example, in [13][14], although the

adopted MPPT algorithm is still FOCV, the reference voltage is computed with an external resistive voltage divider and updated every 16 s, current sensing is implemented by mirroring the inductor current, the converter is disabled for 256 ms while refreshing the reference MPP, and a synchronous clocked control logic is used. In this work, design techniques ensuring a lower consumption have been developed: the reference MPP is computer with an internal capacitive divider every 8 cycles (i.e. much more frequently), current sensing is performed by monitoring the voltage drop on switches with no mirrored current branches, the converter is only disabled for few µs while refreshing the MPP, and an asynchronous control logic is adopted so that any unnecessary switching power is canceled. Such choices allow for a lower intrinsic power consumption as well as a lower start-up voltage. In addition, as it will be shown later on, the energy conversion efficiency of the proposed IC is significantly higher than that of [13][14] for input power levels in the order of few µW and input voltages up to few hundreds of mV. However, it is also worth to note that the circuit in [13][14] is capable of sustaining a higher power rating up to 300 mW. In general, the proposed work is specifically optimized for input power ranges down to few µW and up to 5 mW. With respect to other implementations proposed by our group in [16] and [31], this work introduces new elements such as an active low-voltage cold start-up circuit, a nano-power LDO, and an application-specific control logic. In addition, this work focuses on low-voltage DC sources, whereas [16] deals with multiple heterogeneous sources and [31] with single piezoelectric transducers. In a previous conference paper [32], simulations of a preliminary version of this circuit lacking relevant blocks were only briefly reported.

II. System Architecture

The overall system architecture is shown in Fig. 1. The converter is composed of three main blocks: the start-up (SU) circuit, the main DC/DC buck-boost converter (MC) and a low drop-out regulator (LDO) in order to provide a stable voltage to the load. The IC requires an external inductor L_1 for the MC and four capacitors. The IC operates with two storage capacitors C_{DD} and C_{ST}, as in [11], [31]. The power conversion and management circuits are supplied by C_{DD} (IC supply), while C_{ST} provides the bulk energy storage (e.g. a supercapacitor) for the application circuits. This choice allows the use of a small capacitor for C_{DD}, which ensures faster activation times and independency from the energy stored on C_{ST}. The capacitor C_{buf} is employed as an energy buffer for MPPT, and C_{REG} provides LDO loop stability compensation and filtering. With the exception of C_{ST}, which is sized upon user application constraints, the other external capacitors have a small footprint and tiny SMD components can be used. The inductor L_1 used by the MC should have a sufficient inductance value, and the chosen one is 10 mH. The reason of such value is the necessity of operating in discontinuous conduction mode (DCM) as energy is transferred from the energy source (ES) and from C_{buf} to C_{ST} or C_{DD} by exploiting resonant LC circuits. Low inductance values would lead to

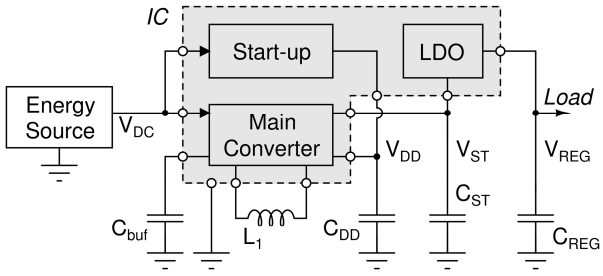

Fig. 1. Architecture of the low voltage converter.

very fast switching periods, in the order of the hundreds of ns, which are not compatible with ultra-low power circuit consumptions.

As the minimum operating voltage of the MC is V_{DDmin} = 1.36 V, while the ESs considered in this work typically output $V_{DC} \leq 1$ V, a voltage booster circuit is required for initial start-up. The SU circuit is a fully integrated charge pump and has the purpose of charging C_{DD} from 0 V up to V_{DDmin}, where the MC can be started. At this point, the MC disables the SU circuit. In this phase, the power consumed by the SU is only due to leakage currents.

The IC has been designed in a STMicroelectronics 0.32 µm microelectronic technology and makes use of CMOS devices.

III. Main Converter

The MC is basically a buck-boost converter and its circuit diagram is shown in Fig. 2. This topology was chosen in order to keep the ES disconnected from the energy storage, and to allow operation at MPP. It has been designed in order to draw a nominal quiescent current I_{DDq} = 96 nA at V_{DD} = 1.4 V. The reference current I_{ref} = 16 nA is generated by the bias block in Fig. 2. Such current is then mirrored and used as tail current in comparators, delay generators and under-voltage lock-out circuit (UVLO).

The MC is kept disabled by an UVLO circuit that triggers when V_{DD} rises above V_{DDmin} and enables the MC, which performs efficient energy extractions at MPPT. The UVLO

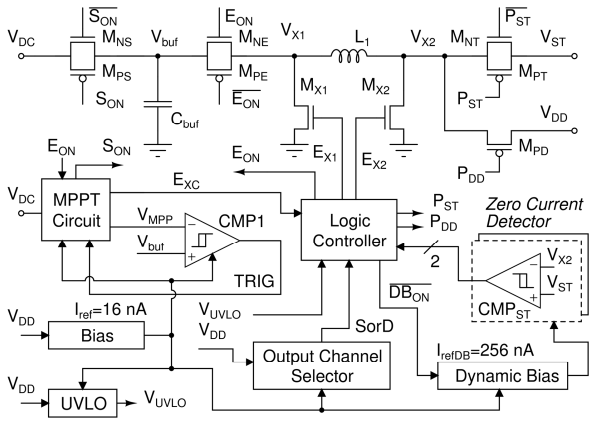

Fig. 2. Circuit diagram of the MC.

provides an output $V_{UVLO} = V_{DD}$ when $V_{DD} < V_{DDmin}$, and $V_{UVLO} = 0$ V otherwise.

A. Two-way Energy Storage Policy

The MC has two possible output channels for the extracted energy stored in inductor: V_{DD} and V_{ST}. This power management policy has been named Two-Way Energy Storage. When the MC is active, C_{DD} gets progressively discharged. As long as the power budget is positive, the priority of the control logic of the MC is to keep V_{DD} over 2 V in order to remain in active mode. While the supply voltage V_{DD} is greater than 2 V, the extracted energy is directed towards C_{ST}. As V_{DD} drops below this value, the extracted energy is directed towards C_{DD} until it is recharged to 2.5 V. This mechanism, operated by the Output Channel Selector block in Fig. 2, allows a faster start-up as the SU needs to charge only C_{DD} to V_{DDmin}. The value used for C_{DD} is 200 nF and can be increased up to some µF, whereas C_{ST} is usually much larger due to applications constraints. Higher values of C_{DD} would increase the start-up time with no benefits on converter performance. Moreover, the dual output channel topology allows C_{ST} to be completely drained if the LDO is replaced with a boost converter regulator. Other two-path architectures have been recently presented [33], where the supply voltage of the converter is directly linked to the voltage of the storage capacitor. Differently, this work keeps V_{DD} and V_{ST} independent, so that the intrinsic power does not increase with V_{ST}. The behaviour of this policy is shown in Fig. 3, where the acquired waveforms on an IC sample are reported. The benefit of a small value of C_{DD} is noticeable: V_{DD} rises quickly into its operative range while V_{ST} ($C_{ST} = 33$ µF) increases slowly.

B. Maximum Power Point Tracking

The chosen technique for MPPT is FOCV because it requires a very limited amount of energy for processing with respect to other techniques as it is based on intrinsic characteristics of the ES. The drawback is a limitation on the tracking accuracy. However, it allows saving power on the control circuit, so that the overall effect is advantageous. The selectable fractions of V_{DC0} are 75% for PV cells, 50% for resistive source and, additionally, 40% for non-linear rectennas, as observed experimentally in [8] [32]. The circuit diagram of the MPPT circuit is shown in Fig. 4. The open circuit voltage of the source V_{DC0} is sampled on C_S for the first time when the MC is activated (i.e. when V_{DD} rises above V_{DDmin}, as shown in Fig. 3). Then, the reference voltage V_{MPP} is generated by sharing the charge $Q_S = C_S V_{DC0}$ on the combination of appropriate capacitors chosen among C_{75}, C_{50} and C_{40}. The capacitor C_{75} is always used for V_{MPP} generation, whereas C_{50} is used only for MPPT at 50% and 40% of V_{DC0} and C_{40} is used only for MPPT at 40%: this approach allows to save silicon area. The capacitor values in Fig. 4 have been chosen in order to scale V_{DC0} to the appropriate value, according to the MPPT configuration.

The open circuit voltage is controlled by pulses on signals S_{ON} and $\overline{S_{ON}}$. The circuit diagram of the pulse generator circuit is shown in Fig. 5. C_{pul} and the transistors have been sized to obtain pulse durations of 2 µs. The static current of this block is almost 0 nA, since it is due only to the leakage currents of junctions, and as no path from V_{DD} to ground exists because of the presence of the switches M_{np} and M_{pp}. In order to cancel charge injection from the latter switches on C_{pul}, a pair of dummy switches M_{npr} and M_{ppr} driven in counter phase has been included in the design.

The reference voltage V_{MPP} is refreshed every 8 energy extraction cycles, in order to track voltage fluctuations, as shown in Fig. 6. During normal operation S_{ON} and E_{ON} are low, so that $V_{DC} = V_{buf}$, and V_{buf} is compared with V_{MPP} (Fig. 2). An energy extraction cycle is started when the E_{XC} signal (i.e. the TRIG signal, disabled during the V_{DC0} sampling phase in order to avoid undesired energy extractions, as shown in

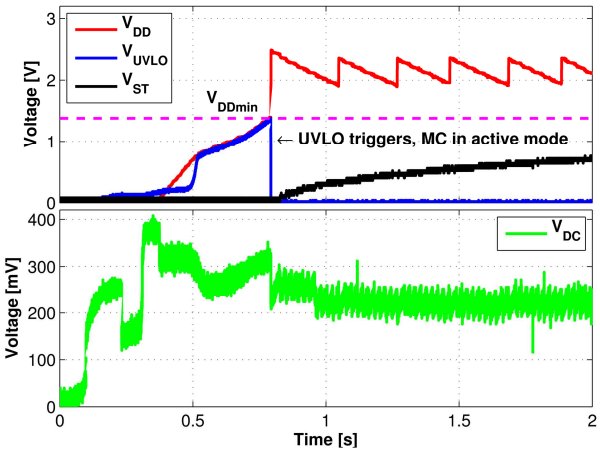

Fig. 3. Acquired waveforms of V_{DC}, V_{DD}, V_{ST}, and V_{UVLO} from an IC sample showing the start-up phase and the behavior of the two-way energy storage. The ES used is a tiny BPW34 photodiode under a table lamp, operated at the estimated MPP after the MC switches to active mode (V_{UVLO} falling to ground).

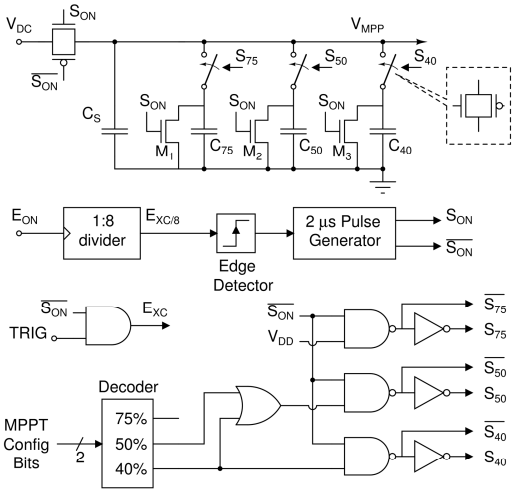

Fig. 4. Circuit diagram of the MPPT block that generates the reference voltage V_{MPP}. For simplicity of representation, the diagram does not include the level shifters required for properly driving the p-channel MOSFETs of the CMOS switches, which will be presented later on.

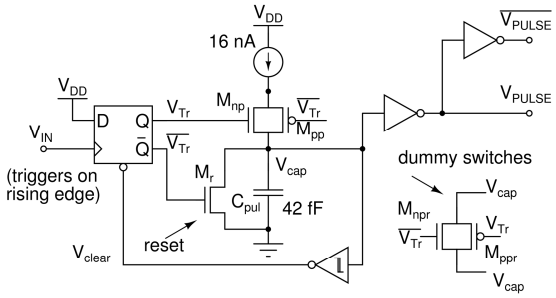

Fig. 5. Pulse generator circuit used in the MPPT block for periodically sampling of the open circuit voltage V_{DC0}.

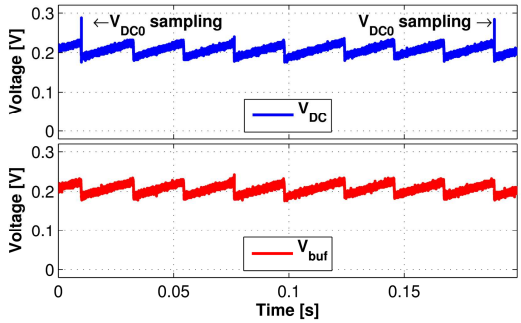

Fig. 6. Acquired waveforms of V_{DC} and V_{buf} from an IC sample showing the MPP being refreshed every 8 energy extraction cycles. The ES is a BPW 34 photodiode under the light of a table-lamp with a 50 W halogen lamp, half-power, at a distance of 45 cm. The noise on the waveforms is due to the oscilloscope (Tektronix MSO2024, no filter or bandwidth limitation).

Fig. 3) goes high, i. e. when $V_{DC} = V_{MPP} + V_H$, where $V_H = 28$ mV is the hysteresis of comparator CMP1 in Fig. 2. The energy extraction from the ES (and C_{buf}) ends when $V_{DC} = V_{MPP}$ - V_H. The ES voltage is kept in a window of size V_H centered in its approximated MPP. The maximum input voltage at MPP $V_{DC,max}$ is limited by the internal p-channel differential pair of comparator CMP1 [16]. The limit is mainly due to the threshold voltage of the p-channel MOSFETs. The maximum allowed open circuit voltage is $V_{DC0,max} = 2.5$ V with the MPPT circuit configured to operate at 50% of V_{DC0}, and $V_{DC0,max} = 1.7$ V for MPPT at 75% of V_{DC0}.

C. Energy Extraction Cycle

During the first phase P1 of the energy extraction cycle, shown in Fig. 7, energy is transferred from C_{buf} and from the ES to the inductor L_1 by turning M_{X2} on and M_{X1} off. M_{NE} and M_{PE} are also turned on (E_{ON} signal high). In the second part P2 of the cycle, M_{X2} is turned off and M_{X1} is turned on, so that energy flows from L_1 to the selected output capacitor, either C_{ST} or C_{DD}, while M_{NE} and M_{PE} are turned off. The process ends when the zero current switching is detected on M_{PT} or M_{PD}, depending on the selected power path. The output channel is selected with the signal SorD, which makes the logic controller choose the correct Zero Current Detector (ZCD) with the signals P_{ST} and P_{DD}. Fig. 7 shows waveforms of V_{X1}, V_{X2}, V_{DD} and V_{buf} acquired during the energy extraction cycle after the UVLO has triggered (V_{DD} is shown to rise from 1.4 V). Phases P1 and P2 are highlighted along with the status of E_{ON}, M_{X1} and M_{X2}.

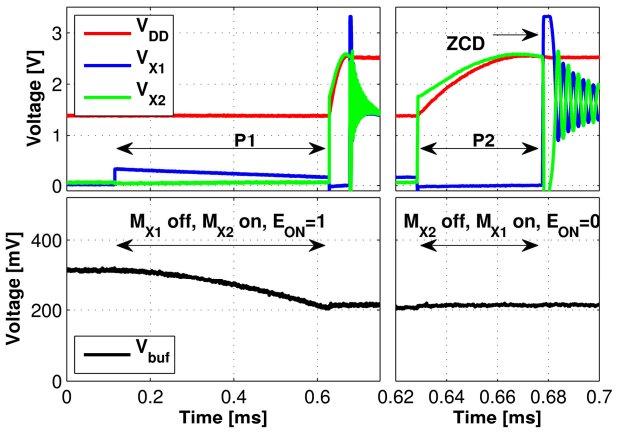

Fig. 7. Acquired waveforms of V_{DD}, V_{X1}, V_{X2} and V_{buf} during an energy extraction cycle. A zoomed view of the ZCD is illustrated on the right part of the figure. As it is the first energy extraction after the MC has switched to active mode, $V_{ST} = 0$ V.

The ZCDs are normally turned off and their static current is negligible, since they are biased by the Dynamic Bias block, which is activated only during energy extraction cycles by the Logic Controller (LC). However, in order to increase the comparator speed, the Dynamic Bias is set to provide a boosted bias current $I_{refDB} = 16 I_{ref}$ (i.e. $I_{refDB} = 256$ nA) to ZCDs, in order to reduce their propagation delay.

D. Logic controller

A simplified circuit diagram of the LC is shown in Fig. 8. The LC implements a finite state machine that controls the energy extraction phases (represented by the state of P1 and P2 signals) and has been designed as a fully asynchronous logic block. This choice allows to spare the energy consumption due to clock generation and to minimize the delay between an event and the corresponding response. A simplified state diagram of the LC is depicted in Fig. 9 with the indication of the triggering events (e.g. the LC moves from the Idle state to state P1 on the rising edge of E_{XC}). The LC also implements specific gate drivers (GD) circuits that provide a proper voltage for driving the p-channel FETs of the

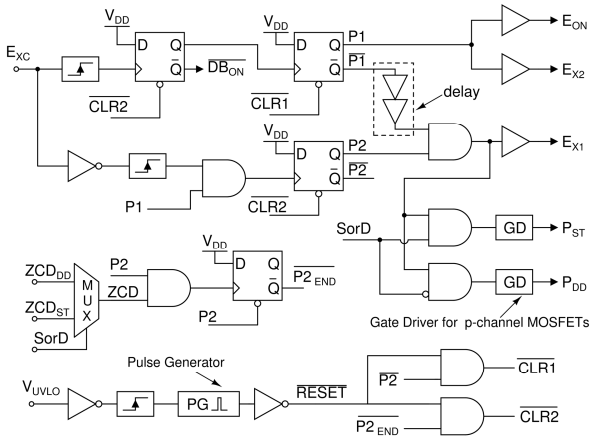

Fig. 8. Simplified circuit diagram of the LC.

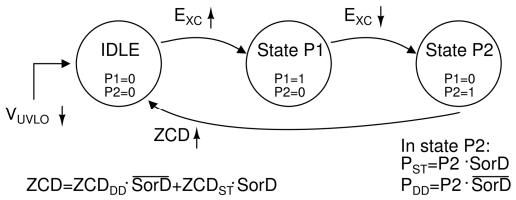

Fig. 9. State diagram of the LC. The upward or downward arrow after a signal name specifies whether the state change occurs on rising or falling edge of such signal.

CMOS switches, i.e. either 0 V or the maximum voltage available in the circuit.

The RESET signal is generated from the high to low transition of V_{UVLO} and is used to clear all memory elements during the transition between passive and active mode in order to ensure the correct state of the circuit.

Due to the presence of variable voltages at each power node (V_{DD}, V_{ST}, V_{X2}, etc.) the pMOS switches have to be driven with the highest available voltage between its source and drain terminals in order to keep the switch open. Specific circuitry was devoted to this purpose. Fig. 10 shows the diagram of the gate drivers blocks depicted in Fig. 8. This type of gate driver was also used with the output of the sub-circuit of Fig. 4. The highest voltage between V_{pS} and V_{pD} is brought to the node V_{DDH} that supplies the level shifter based on a DCVSL-like stage and a buffer driving the switch gate.

IV. Low Voltage Start-up

The SU is required in order to initially charge C_{DD} up to V_{DDmin}. It is a 16-stage charge pump based on [34] and its circuit diagram is shown in Fig. 11. The SU is supplied directly by the ES through the V_{SUin} pin. The output of the charge pump V_{SUout} is connected to V_{DD}.

Low threshold MOSFETs have been used in the SU, in order to reduce the minimum value of V_{SUin} that allows $V_{SUout} \geq V_{DDmin}$. The number of stages has been evaluated from simulations in order to provide an output impedance lower than 14 MΩ at V_{SUin} = 0.25 V, which is the value of the input impedance of the MC seen from its power supply input port (V_{DD} and GND).

A 33-stage ring oscillator generates the clock signal *CK,* which is then used to generate the two phases required by the

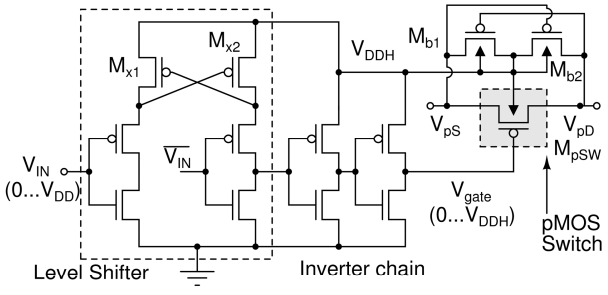

Fig. 10. Circuit diagram of the gate drivers with the level shifter input stage used for scaling signals from the 0-V_{DD} range to 0-V_{DDH}, where V_{DDH} is the highest voltage between the voltages at the source V_{pS} and at the drain V_{pD} terminals of the switch.

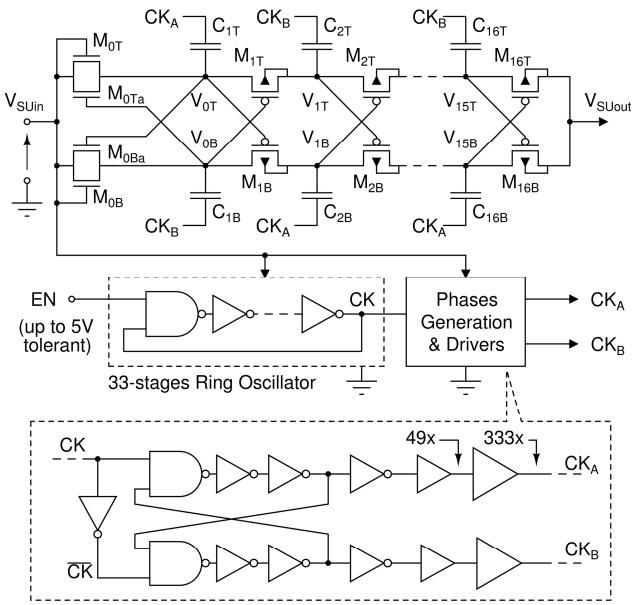

Fig. 11. Circuit diagram of the SU block.

charge pump branches. The generated frequency f_{CK} depends on V_{SUin}. According to simulations, f_{CK} = 770 kHz at V_{SUin} = 250 mV. The ring oscillator can be disabled by driving the *EN* input to 0 V. The circuit generating the non-overlapping phases with the buffers is depicted on the dashed box on bottom of Fig. 10, with the indication of the overall driving strenght of the buffers at the annotated nodes.

The active area of the SU is 0.192 mm^2. The 32 flying capacitors $C_{1T},\ldots C_{16B}$ are 2.52 pF each and occupy the 62% of the overall area of the SU. The remaining area is occupied by the buffers driving the CK_A and CK_B clock signals and by empty space required to separate the n-wells of $M_{1T},\ldots,M_{15B}$ since each one of them is at a different potential.

The connection of the SU with the MC is shown in Fig. 12. The EN signal is connected to the ES through a resistor R_{ENS} = 44 MΩ, and to the V_{UVLO} signal through R_{ENU} = 0 Ω. The resistor R_{ENU} can be substituted with a short-circuit because, at start-up, the inverter driving V_{UVLO} is in a high-impedance state until $V_{DD} \approx 0.6$ V. As V_{DD} rises above this value, V_{UVLO} follows V_{DD}, keeping the SU active. When the UVLO triggers, V_{UVLO} = 0 V and also EN gets close to 0 V as R_{ENU} is far less resistive than R_{ENS}. In this implementation, for testing purposes, R_{ENU} and R_{ENS} are external resistors. The high resistance of R_{ENS} is necessary in order to cause only

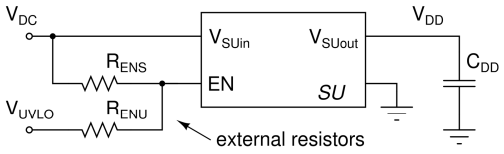

Fig. 12. Schematic of the connections of the SU block with the MC.

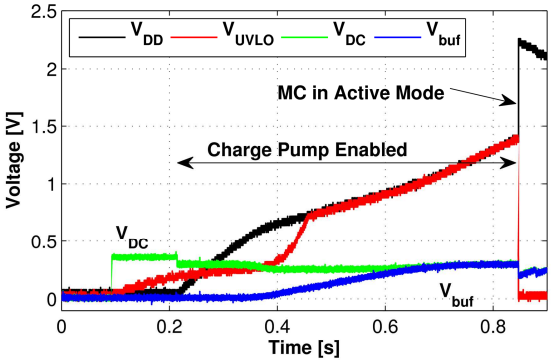

Fig. 13. Acquired waveforms of V_{DC}, V_{UVLO}, V_{buf} and V_{DD} during the start-up phase with a BPW 34 photodiode as ES. After the MC switches in active mode, the operation at MPP (set to 75% of V_{DC0}) is observable. External components values are: C_{DD} = 200 nF, C_{buf} = 22 µF, and C_{ST} = 33 µF.

negligible perturbations on the ES, since the typical current drawn is less than 12 nA at V_{DC0} = 0.5 V. However, it is estimated that they might be integrated in a fraction of mm^2.

Fig. 13 shows the waveforms acquired in a realistic case, where a start-up from V_{DC} = 0 V (V_{DC0} = 383 mV after the ES is illuminated) and V_{DD} = 0 V (V_{buf} and V_{UVLO} are 0 V by consequence) is performed. The ES is a 7.5 mm^2 BPW34 photodiode exposed at indoor light at time t = 0.1 s. In the initial phase the ES charges the parasitic capacitance, which is mainly due to the probe in this case, on the EN pin (i.e. the V_{UVLO} signal as R_{ENU} = 0 Ω) and, subsequently, the SU is then activated. C_{DD} and C_{buf} are charged. As V_{DD} = V_{DDmin}, the V_{UVLO} signal falls to 0 V and the MC is activated.

V. Output Regulation

A regulated output voltage is necessary for supplying application circuits such as wireless sensor nodes. For this purpose, a low quiescent current LDO has been designed and integrated. The circuit diagram of the LDO is shown in Fig. 14. The circuit has been implemented as an independent block and thus some of the bias circuitry of the MC has been replicated. The LDO draws a nominal static current of 251 nA. However, in a future version of the IC, sharing the bias block with the MC would reduce the static current to 203 nA. The LDO active area is 0.147 mm^2. Differently from existing nano-current commercial solutions [35], which use arrays of floating gate transistors programmed during manufacturing to precisely set the desired output voltage, the designed LDO uses standard CMOS. The choice of a LDO as a voltage regulator is motivated by the envisaged applications of this circuit, i.e. low duty-cycle wireless sensor nodes with a very low average current consumption. In this type of low-current applications, alternative topologies such as switching regulator would introduce higher power consumption to precisely regulate the voltage with loads of few µA and increased circuit complexity. On the other hand, LDOs present simpler control circuits and high efficiencies when input and output voltage are close to each other: since supercapacitors are typically used for energy storage, and since their maximum voltage should not exceed ≈2.5 V which is close to the supply voltage of low-power electronics, the efficiency of the LDO would remain high. In addition, given the high capacitance, an activation of the load would not cause significant voltage drops. However, switching regulators would be more appropriate and more efficient with loads demanding higher currents or with higher drop-out voltages to compensate. Nonetheless, this would require additional external components (e.g. a second inductor), as well as more complex internal control circuits (e.g. for generating the switching control waveforms).

The only required external component is a capacitor with minimum value C_{REG} = 10 µF, required for ensuring stability. The LDO has an external enable input (EN_{LDO} signal in Fig. 14). Moreover, the LDO features an internal UVLO that forces the transistor M_{PR} to be turned-off (i.e. V_{GR} is driven to V_{IN}) and thus forces, at steady-state, V_{REG} = 0 V. In a similar fashion to the MC, the UVLO disables the LDO if $V_{IN} \leq V_{DDmin}$. A second UVLO circuit, shown in Fig. 14, disables the LDO if there is not a sufficient input voltage, i.e. if $V_{IN} \leq V_{REG} + V_{SAFE}$, where the voltage V_{SAFE} is a safety margin set to about 350 mV. This feature, which can be externally disabled, has a positive effect on the energy budget of the system as it limits the static and leakage currents of both the load and the LDO when the input voltage V_{IN} is lower than required for operations.

The output voltage divider is fully integrated and is composed of a fixed resistor R_1 = 2.4 MΩ and a second resistor R_2, which is programmed by the configuration logic in order to provide the desired output voltage V_{REG}. The possible options for V_{REG} are 1.8 V, 2.5 V, 3.0 V and 3.3 V. The different values of R_2 generate the same current I_{fb} = 230 nA in each configuration. The overall nominal static current of the LDO is 481 nA. The LDO is stable in a no external load condition. A short-circuit protection with a current limit of 50 mA has also been implemented: the sense resistor R_{SENSE} = 500 mΩ is a chunk of a metal track. On top of Fig. 14 the circuit diagram of the current limiter circuit is shown. The static current of the current limiter is only 32 nA (when the sensed current is lower than 50 mA) and flows through M_{Pc1} and M_{Pc2}. The comparator has been implemented with a current mirror and the mismatch of the devices sizing (1:3 ratio) generates an offset of about 25 mV, which sets the maximum voltage drop allowed on R_{SENSE}. If such value is exceeded the current limit triggers and a current is sourced to V_{GR}, reducing the V_{SG} of M_{PR}.

The generation of the reference voltage V_{REF} is based on the threshold voltage of the n-channel MOSFETs. V_{REF} is obtained from the voltage drop on two identical series connected transistors. The first one is diode-connected, with its drain and gate connected to V_{REF}. The second is used as a source degeneration with the gate connected to V_{REF} in order to improve the independence of V_{REF} with respect to V_{DD}. The circuit is simple and effective in case a very high precise output voltage is not necessary. Montecarlo simulations showed that the mean voltage reference V_{REF} is 552.6 mV with a standard deviation of 6.12 mV at room temperature and

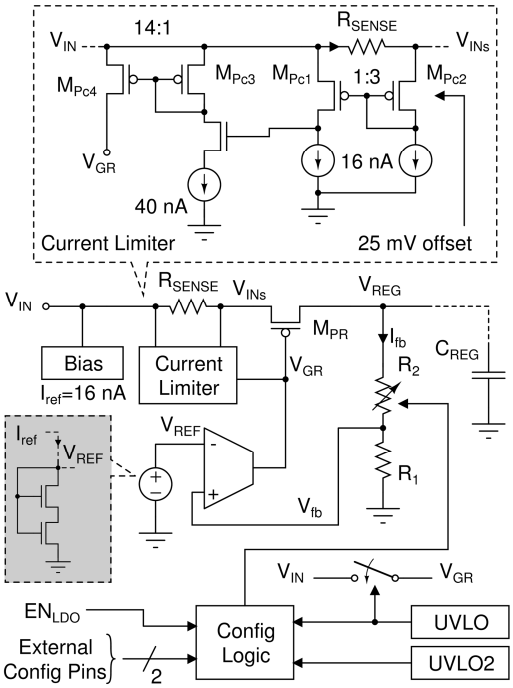

Fig. 14. Architecture of the low drop-out regulator.

V_{IN} = 2.5 V. This tolerance does account for the generation of V_{REF} and I_{ref} from the bias circuitry. However, it does not account for amplifier input offset, typically 7 mV, and for mismatch of R_1 and R_2, which were found to be negligible.

VI. Experimental Measurements

The experimental measurements in this section have been performed on samples of manufactured devices. A photograph of a manufactured die and of a packaged sample (CLCC68 package) is shown in Fig. 15 together with a BPW34 photodiode with 7.5 mm^2 of active area that was used for functional testing. The die area, a substantial part of which is taken by the pad ring, is 4.58 mm^2 while the active areas are respectively 0.588 mm^2 for the MC, 0.192 mm^2 for the SU, and 0.147 mm^2 for the LDO. The total active area is 0.93 mm^2.

A. Functional tests

Functional tests have been performed with a BPW34 photodiode as ES, which was illuminated by a 50 W halogen lamp placed over the photodiode at a distance of 45 cm. The maximum output power of the ES at 75% of V_{DC0} = 373 mV was 14.8 µW (measured with a Keithley 2601A SMU). The external components of the circuit are C_{DD} = 200 nF, C_{ST} = 33 µF, C_{buf} = 32 µF, L_1 = 10 mH.

Fig. 3 shows the acquired waveforms of V_{DD}, V_{ST}, V_{DC} and V_{UVLO} with the aforementioned setup: the two-way energy storage policy can be clearly seen as V_{DD} quickly enters in its operative range after the start-up phase while V_{ST} raises slowly as C_{ST} >> C_{DD}. Fig. 13 shows the same process, acquired in a second time, with the focus on the operations of the SU and the subsequent energy extraction at MPP after the UVLO trigger. In a third test, the waveforms associated to the MPPT circuit have been recorded, in order to show the periodic refresh of the open circuit voltage V_{DC0} (depicted in Fig. 6) and the waveforms of inductor nodes V_{X1} and V_{X2} during an energy extraction cycle of the MC (depicted in Fig. 7).

B. Quiescent current

Firstly, the characterization of the MC is presented. The first measurements is the converter quiescent current and it has been measured with a Keithley 2601A SMU forcing V_{DD} and is I_{DDq} = 121 nA at V_{DD} = 2.0 V, while I_{DDq} = 101 nA at V_{DD} = 1.4 V (i.e. slightly above V_{DDmin}, when the MC is in active mode). The equivalent input resistance R_{MC} of the MC seen from its power supply input and corresponding to its intrinsic current consumption, is useful for validating the SU, as it allows to estimate whether the SU can sustain the MC during the start-up phase. In order to characterize R_{MC}, the quiescent current I_{DDq} has been measured in a range of V_{DD} values closely centered on V_{DDmin}. Fig. 16 shows the measured values of R_{MC} and its minimum value is R_{MCmin} = 10.28 MΩ at V_{DD} = 1.36 V.

C. Efficiency

In a second experiment the converter efficiency has been also investigated at different input power levels and voltages V_{DC0}. For this purpose, a constant current was sunk from V_{ST} with a SMU in order to set the output voltage at a desired value. The efficiency was assessed as the ratio between the output power flowing from the V_{ST} node and the maximum theoretical input power (i.e. $V_{DC0}^2/4R_S$). Five input configurations are shown in Fig. 17. In order to better control source characteristics, in these measurements the ES has been emulated with a voltage source with a series resistance and with the FOCV MPPT circuit configured at 50% of V_{DC0}. The MC has been tested with five different input configurations

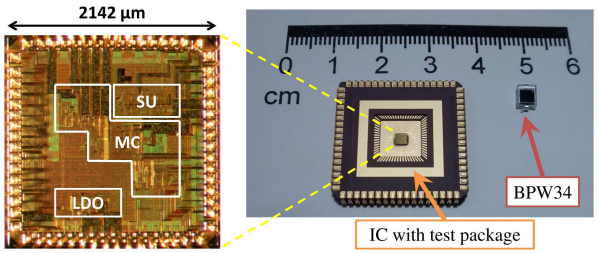

Fig. 15. Die micrograph and photograph of a packaged IC sample and of a BPW34 photodiode used as ES.

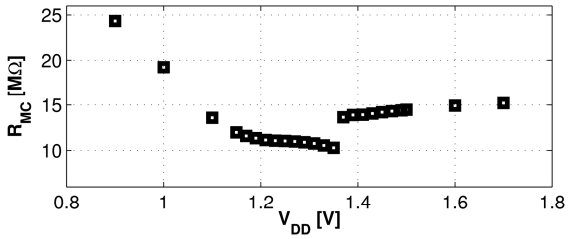

Fig. 16. Measured input resistance R_{MC} of the MC. The abrupt variation of R_{MC} at V_{DD} = 1.36 V (i.e. V_{DDmin}) is due to the change of state of the UVLO circuit.

with input power ranging from 10.5 µW to 437 µW, with several values for V_{DC0} (from 248 mV up to 1.6 V) and R_S (from 267 Ω up to 4.607 kΩ). The parameters of the ES used in each measurement are shown in the legend of Fig. 17. The chosen value of R_S are comparable with the resistance of several low-voltage transducers (e.g. BPW34, Micropelt MPGD751, [8], [32]). The measured peak efficiency is 77.1% when the MC is self-supplied, i.e. the system is fully autonomous, whereas it reaches 79.3% if V_{DD} is provided externally (V_{DD} = 2.4 V).

Differently from off-the-shelf power converter components, the presented IC has still high efficiencies at these very low power regimes. We remark that typical DC/DC components target significantly higher power regimes and normally operate in continuous conduction mode, whereas the proposed IC has been designed for operation in discontinuous conduction mode in the sub mA region. For this purpose, the inductor and switch sizings were carefully selected in order to reduce losses in the resonant circuit.

The above results also highlight, as discussed beforehand, the efforts made in order to reduce the power consumption of the MC, mainly the static one. The converter efficiency has a strong dependency on the input voltage V_{DC}. However, this can be mitigated, in a future version, by increasing the conductivity (i.e. the size) of the switches M_{NE} and M_{PE} at the cost of a slight increase of dynamic switching consumption. Another aspect that influences the MC efficiency is the relationship between the amount of energy E_{CYC} extracted per cycle and the ZCD delay: such delay has a noticeable effect on efficiency when $V_{ST} \geq 3.5$ V because it becomes comparable with the duration of phase P2. Then, if the operations at $V_{ST} \geq 3.5$ V are prevalent, an improved ZCD circuit should be used. Moreover, this effect is more evident when the amount of energy per cycle E_{CYC} is small, in the order of 100-200 nJ, since the ZCD delay introduces an amount of energy losses related to the value of V_{ST}.

An approximation of such energy loss can be expressed considering a linear decrease of the inductor current after the real zero crossing (i.e. $i_{L1} = 0$ A). A minimum back current $i_{ZCDnom} = V_{hyst}/R_{XT}$ is required for the detection of the zero-crossing, where V_{hyst} = 15 mV is the hysteresis of comparator CMP_{ST}, and R_{XT} = 7.5 Ω (nominally) is the equivalent resistance of switches M_{PT} and M_{NT} in Fig. 2. However, the back-current further increases due to the propagation delay t_{PDcomp} of the comparator CMP_{ST} in Fig. 2, which is about 800 ns. The back-current also increases faster as V_{ST} raises, because the ideal duration of phase P2 becomes shorter and, as a consequence, the slope of current becomes steeper. A simplified expression of such losses is shown in (1) and $E_{ZCDloss}$ can easily reach some tens of nJ. Furthermore, R_{XT} is not constant with respect to V_{ST} but inversely proportional to it, because the transistors undergo a higher overdrive with higher V_{ST}.

$$E_{ZCDloss} = \frac{1}{2} L \left(\frac{V_{hyst}}{R_{XT}} + \frac{V_{ST}}{L} t_{PDcomp} \right)^2 . \quad (1)$$

As (1) points out, $E_{ZCDloss}$ is independent from the input power, and so from E_{CYC}. Comparing $E_{ZCDloss}$ with E_{CYC} allows a fast evaluation of the upper bound of MC efficiency. The above equation helps understanding the reason of the higher measured efficiency of the MC with an input power of 34.6 µW with respect to the same test but with an input power of 57.6 µW. In fact, in the first condition E_{CYC} = 270 nJ with a measured activation frequency of 128 Hz, whereas in the latter case E_{CYC} = 181 nJ with a measured activation frequency of 318 Hz. As can be seen in Fig. 17, in the condition for the lowest efficiency (V_{DC0} = 248 mV and R_S = 1464 Ω) it results E_{CYC} = 154 nJ with a measured activation frequency of 68 Hz, whereas the condition for the highest efficiency (V_{DC0} = 248 mV and R_S = 1464 Ω) corresponds to E_{CYC} = 908 nJ with a measured activation frequency of 480 Hz. Therefore, the efficiency depends on the ratio between the energy converted per cycle E_{CYC} and the associated losses (fixed and proportional, e.g. Joule effect). E_{CYC} can be estimated as $E_{CYC} = 2C_{buf}V_{MPP}V_H$. A method for increasing E_{CYC} is the use of a larger C_{buf}: however, this action also extends the duration of P1, increasing the losses due to Joule effect on switches and inductor resistance.

A simple solution for mitigating the losses due to the excessive delay of the ZCS circuit would be an increase of I_{ref} in order to reduce the propagation delay of comparator CMP_{ST}. However, in micro-power applications such losses do not necessarily represent a significant limitation because external circuits typically operate at lower supply voltages obtainable with $V_{ST} < 3.5$ V.

D. Energy consumed per conversion cycle

In a third experiment, the energy E_C drawn by the MC during an energy extraction cycle has also been measured. In order to evaluate the MC dynamic consumption, the MC has been externally supplied (V_{DD} = 2.4 V) and the average current drawn I_{avg} has been measured with an Agilent E34401A multimeter as the drop voltage on a 6.8 kΩ sense resistor. The

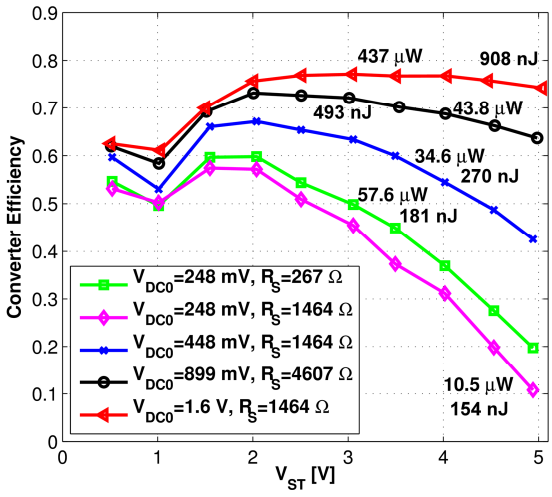

Fig. 17. Measured efficiency of the MC for different power levels (input voltage V_{DC0} and series resistance R_S). The reported efficiency is related to the self-supplied MC. The energy per cycle E_{CYC} is also shown along with the input power.

frequency f_e of energy extractions was also measured with a digital oscilloscope. The dynamic current I_{dyn} drawn by the MC is then obtained by subtracting I_{DDq}. E_C can be evaluated from measurements as:

$$E_C = V_{DD}\left(I_{avg} - I_{DDq}\right)f_c^{-1} = V_{DD}I_{dyn}f_c^{-1} \quad (2)$$

The MC uses $E_C = 6$ nJ (at $V_{DD} = 2.4$ V and $V_{ST} = 1$ V) to perform a complete energy extraction cycle while supplying the LC, the analog circuits, and the switch drivers. However, when V_{ST} rises above 2.5 V, some energy is subtracted also from C_{ST}, mainly for driving the switches. This may reduce the energy drawn from C_{DD}, but also increases the overall energy consumption. However, E_C also depends on the choice of external components as C_{buf} and L, on the series resistance R_S, and on the open-circuit voltage V_{DC0} of the ES.

E. Minimum and maximum input power

The minimum input power, required for sustaining active operation of the MC, once the MC has started, has been investigated in a fourth experiment. The source was emulated with $R_S = 1464$ Ω and a decreasing V_{DC0} until the circuit ceased operating. A minimum input power of 935 nW, computed as $V_{DC0}^2/(4R_S)$, was found at $V_{DC0} = 74$ mV. In this case, no power was delivered to C_{ST}. However, such a low V_{DC0} voltage does not allow the MPPT circuit to work efficiently as the voltage swing required for conversion is comparable with V_{DC0}. The swing of V_{buf} (and hence V_{DC}) has been measured as 42.5 mV, which is the 57.4% of the open circuit voltage V_{DC0}. Data elaboration from acquired waveforms showed that the average input power from the ES was, in the experiment, about 838 nW, with a drop of 10% with respect to theoretical maximum.

The maximum input power that can be handled by the MC has been experimentally evaluated in a fifth experiment. An ES was emulated with $R_S = 267$ Ω and an increasing V_{DC0} until the circuit ceased operating. A maximum input power of 4.95 mW was found at $V_{DC0} = 2.3$ V, $R_S = 267$ Ω, and with $C_{DD} = 200$ nF, $C_{ST} = 33$ µF, $C_{buf} = 32$ µF, MPPT at 50%. The voltage on V_{ST} settled at 3.15 V with a load resistor of 3227 Ω connected to V_{ST}. The MC was self-supplied and the net output power has been measured as 3.07 mW, with an efficiency of 62%. However, an optimum output load was not used. This power limit is mainly due to the time required for energy extraction (energy transfer between RLC circuits) and can be increased by reducing the inductance value of L_1: the drawback is a decrease of efficiency, especially for $V_{ST} > 3$ V, due to ZCD delay as shown in Fig. 17.

The maximum input voltage $V_{DC0,max}$ allowed by the converter has been investigated in a sixth experiment and the MC operates correctly up to $V_{DC0} = 2.5$ V, with $R_S = 4.7$ kΩ and the MPPT configured at 50%.

F. Start-up Circuit

Fig. 18 shows the steady-state output voltage of the SU for several values of V_{SUin} with a load $R_{SUL} = 10$ MΩ on V_{SUout}. The load R_{SUL} was imposed by the Agilent E34401A multimeter used in the tests, and is suitable to emulate the MC ($R_{MCmin} = 10.28$ MΩ). The minimum measured voltage

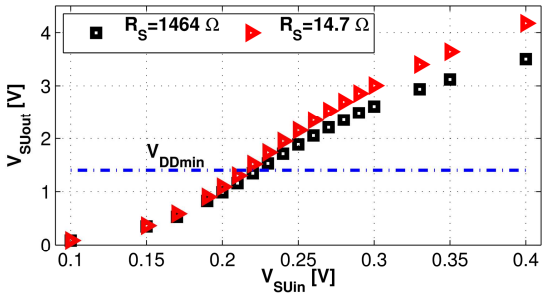

Fig. 18. Measured V_{SUout} with a load of 10 MΩ as a function of V_{SUin} and source resistance R_S.

required by the SU to reach $V_{SUout} \geq V_{DDmin}$ is 223 mV for $R_S = 1.46$ kΩ. In order to verify the ability of the SU to supply the MC, the output resistance R_{SUout} of the SU, which can be modelled as a voltage source with a series resistance R_{SUou}, has been evaluated from two different sets of measurements. The first set was obtained with $R_{SUL} = 10$ MΩ, whereas the second set in open circuit with $R_{SUL} > 10$ GΩ, corresponding to an additional setting of the multimeter. The obtained results are illustrated in Fig. 19. The minimum value of R_{MC} (i.e. R_{MCmin}) is highlighted in the graphs and shows that R_{SUout} is always lower than R_{MC} in the useful input voltage range ($V_{SUin} > 223$ mV), especially when $V_{DD} \leq 1$ V, hence the designed SU is suitable as start-up block for the MC.

The efficiency of the SU, evaluated in a further experiment as the measured output power on a 10 MΩ load divided by the measured input power, has also been investigated and the results are depicted in Fig. 20. However, the low efficiency of this block is not an issue as the SU is not the main energy path from the ES to C_{ST}. It must only provide the conditions (i.e. $V_{DD} = V_{SUout} \geq V_{DDmin}$) for the start of the MC, whenever the system falls in a fully discharged state.

G. Low Drop-out Regulator

The performance of the LDO has been tested. Fig. 21 shows the measured quiescent current of the LDO for each output voltage. The graph clearly illustrates the operation of the UVLO that disables the LDO output and limits its quiescent current to the expected value (i.e. 251 nA). However, the LDO

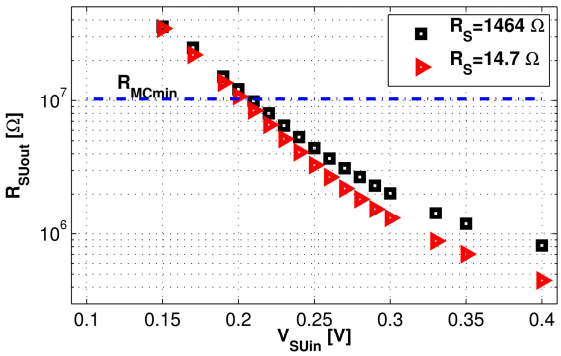

Fig. 19. Measured output resistance R_{SUout} of the SU in different input conditions.

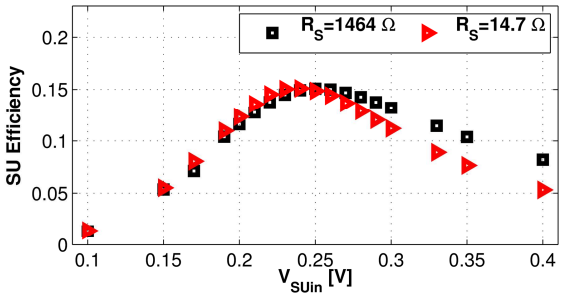

Fig. 20. SU power conversion efficiency.

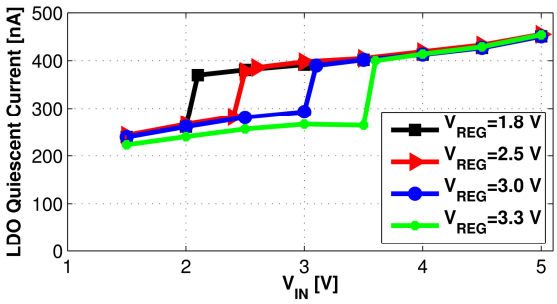

Fig. 21. LDO quiescent current for each output voltage configuration.

quiescent current graph discloses a dependency on V_{IN} much stronger than expected from simulations.

Another set of experimental measurements has been performed on 12 samples of the IC in order to verify the output voltage spread with respect to the nominal value. The measured average output voltage is about 7.2% lower than in simulations for each configuration. The standard deviation is 1.9% of the nominal V_{REG} value. Hence, the circuit is suitable for applications that do not require a high precision, and where minimization of intrinsic power is the main goal. However, since the standard deviation is quite low, the normalized output values are quite close to the average value with low dispersion. Then, different sizings in future designs are expected to improve the accuracy on the output voltage, while providing sufficient repeatability.

The line regulation of the LDO is less than 10 mV/V with a load current of 1.17 mA and V_{REG} set to 1.8 V. The measured load regulation, with the same set-up, has been measured to be 5.31 mV/mA, with a load current variation from 1.17 mA to 115 µA.

VII. Conclusions

This work presents a power management IC for low-voltage DC/DC energy harvesting with a dedicated bootstrap circuit enabling battery-less cold start-up from input voltage down to 223 mV and with an output voltage regulation stage. Once cold start-up is performed, is the boostrap circuit is automatically disabled and the main converter starts operating, so as to increase efficiency and to limit the power absorption. The main converter is based on a buck-boost topology and features a static current of 121 nA with a peak efficiency higher than 77%. The IC was tested with input voltage ranges from 74 mV up to 2.5 V. Thanks to nano-power design techniques and to a careful control of the energy consumption, the circuit can operate with an input power of less than 1 µW.

We remark that, with respect to other similar works in literature or to off-the-shelf power converter ICs, this designs was specifically conceived for achieving sufficient efficiencies at very low input power regimes. For this reason, the design had to account for several design trade-offs between efficiency and power consumption. Decreasing the minimum manageable power to such low levels paves the way towards the deployment of a new class of applications based on tiny and weak environmental sources that could not be efficiently exploited up to now.

A series of design optimizations could still be possible, for example the ones suggested in the previous sections to mitigate some of the undesired factors affecting performance. Additionally, other types of blocks could be successfully integrated in case of different specifications: start-up circuits based on step-up oscillators might allow start-up from significantly lower voltages, while regulating the output voltage with switching converter could grant additional advantages in different operating conditions.

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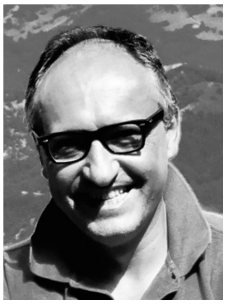
Michele Dini received the B.S. and M.S. degrees in electrical engineering and Ph.D. degree in information technologies from the University of Bologna, Cesena, Italy, in 2008, 2011 and 2015, respectively. Since 2012, he has been with the Advanced Research Center on Electronic Systems and at the Department of Electrical, Electronic, and Information Engineering of the same university. He has been involved with energy harvesting systems, design of CMOS power converters and power management circuits.

Aldo Romani received the Dr.Eng. degree in electrical engineering and Ph.D. degree in electrical engineering, computer science, and telecommunications from the University of Bologna, Bologna, Italy, in 2001 and 2005, respectively. In 2008, he joined the University of Bologna, Cesena, Italy, as an Assistant Professor. He has authored or coauthored more than 40 international scientific publications. He has been involved with CMOS integrated sensors, applications of piezoelectric materials, and energy harvesting systems. Dr. Romani was a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference.

Matteo Filippi received the degree in electrical engineering in 2011 from the University of Bologna, Cesena, Italy. Since 2012, he has been with the Advanced Research Center on Electronic Systems and with the Department of Electrical, Electronic, and Information Engineering, University of Bologna, Cesena, Italy, where he has been involved in energy harvesting systems, micropower electronics, and CMOS design.



Marco Tartagni (M'98) received the M.S. degree in electrical engineering in 1988 and the Ph.D. degree in electrical engineering and computer Sciences in 1993 both from the University of Bologna, Bologna, Italy. In 1994, he joined the Department of Electrical Engineering, California Institute of Technology, Pasadena, CA, USA, as a Research Fellow. Since March 1995, he has been with the Department of Electronics, University of Bologna, where he is currently an Associate Professor. In 1997, he designed the first silicon-only fingerprint capacitive sensor. In 1999, he co-founded the company Silicon Biosystems active in the field of lab-on-a-chip devices. From 2005 to 2008, he was an European coordinator of FP6 Receptronics in the Nanotechnology thematic area. Since 2008, he has been a coordinator of the Working Group on Energy Autonomous Systems within the European CATRENE initiative. Since 2014, he has been a Member of the Scientific Board and Team Leader of the joint STMicroelectronics and Bologna University lab for sensor design. He has coauthored more than 100 refereed scientific publications, 18 granted U.S. patents, and 11 European and WIPO patents. Prof. Tartagni was a co-recipient of the 2004 Jan Van Vessem Award of the IEEE International Solid-State Circuits Conference.