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Trapping Dynamics in GaN HEMTs for Millimeter-Wave Applications: Measurement-Based Characterization and Technology Comparison

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Abstract: Charge trapping effects represent a major challenge in the performance evaluation and the measurement-based compact modeling of modern short-gate-length (i.e., ≤0.15 µm) Gallium Nitride (GaN) high-electron mobility transistors (HEMT) technology for millimeter-wave applications. In this work, we propose a comprehensive experimental methodology based on multi-bias large-signal transient measurements, useful to characterize charge-trapping dynamics in terms of both capture and release mechanisms across the whole device safe operating area (SOA). From this dataset, characterizations, such as static-IV, pulsed-IV, and trapping time constants, are seamlessly extracted, thus allowing for the separation of trapping and thermal phenomena and delivering a complete basis for measurement-based compact modeling. The approach is applied to different state-of-the-art GaN HEMT commercial technologies, providing a comparative analysis of the measured effects.

Keywords: semiconductor device characterization; gallium nitride; transient measurements; pulsed measurements; charge trapping; low-frequency dispersive effects

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1. Introduction

The advent of the 5G standard and its Frequency Range 2 (FR2) implementation in the Ka-band has recently prompted the development of advanced semiconductor technologies necessary to provide suitable radio-frequency (RF) power, linearity, and efficiency in the millimeter-wave frequency range. In this context, high-electron mobility transistors (HEMT) technologies based on Gallium Nitride (GaN) are particularly investigated given their outstanding properties in terms of RF power density, high cut-off frequency (f_t), and the capability to efficiently dissipate heat [1].

With respect to the previous generation of GaN HEMTs featuring 0.25-µm gate-length mainly targeting X-band applications [2], GaN processes for 5G FR2 must implement gate lengths ≤ 0.15 µm to provide $f_T > 35$ GHz and an effective performance in the Ka-band [3]. At the same time, they must become economically viable for low-cost communications applications. In this sense, while Silicon Carbide (SiC) substrates provide state-of-the-art Monolithic Microwave Integrated Circuit (MMIC) design performance [4], a whole new generation of GaN-on-Si RF devices is being developed with the aim of reducing the cost of the substrate and of exploiting the established Si-based RF and digital process technology [5–10].

Despite the attention dedicated to 0.25-µm GaN HEMTs, a relatively small amount of literature data is available for performance assessment and compact modeling of sub-0.15-µm devices [11–15]. However, it is well-known that GaN devices inherently suffer from low-frequency dispersive phenomena due to self-heating and charge trapping, and that these effects involve a complex nonlinear dependency with respect to the instantaneous voltages applied to the device ports [16,17]. Although commercial MMIC solutions

and proprietary process design kits (PDKs) are available for sub-0.15-µm devices, PDKs do not usually include an accurate description of trapping-related phenomena. Nevertheless, these effects greatly impact RF power amplifier and RF switch applications [18–20] and will become even more problematic for 5G linearity requirements. Indeed, 5G standard will feature frame duration (10 ms) and sub-carrier spacing (down to 15 kHz) falling on the same range with respect to the typical low-frequency time constants, impacting error-vector magnitude (EVM) across GHz-wide bandwidths (BWs) [21]. Moreover, sub-0.15-µm gate lengths are more prone to short-channel effects, such as poor electron confinement and punch-through phenomena, in presence of high electric fields [22,23].

Pulsed-IV (PIV) measurements are normally used for obtaining iso-thermal HEMT characteristics. However, fast charge capture times (down to the ns-range) combined with slow charge release (in the ms-range and above) cause each point on the PIV to belong to a different trapping state [24], preventing the acquisition of reliable datasets for GaN device modeling. Whereas specific multi-pulse techniques for trap state conditioning [25,26] based on tailored pulsed setups [27] have been proposed, and provided that classical single-pulsed PIVs from different quiescent points are still useful to quantify gate- and drain-lag effects [28,29], PIV measurements can only provide a steady-state snapshot of the device, not accounting for the time evolution of the state (i.e., the trap capture/release time constants).

Such low-frequency dynamic effects characterization might involve small-signal (Y-parameters) [30] or noise [12] measurements in the dispersion range, but biasing constraints often restrict the characterization to a limited part of the safe operating area (SOA). Moreover, the small-signal regime does not easily allow to characterize the global nonlinear dynamic dependencies on the applied voltages. An alternative method consists in the analysis of current transients after the application of specific voltage steps for deep-level current transient spectroscopy (I-DLTS) [31,32]. This technique allows for the extraction of time constants and activation energies of thermally-assisted de-trapping mechanisms. However, small-signal techniques and I-DLTS can display conflicting results [12,33] and, despite providing key information for the physics-based understanding of the device, their usage is not straightforward for measurement-based compact modeling. Other approaches include swept two-tone test at variable frequency spacings around the RF carrier [13,34], or pulsed-RF radar-like excitation and the measurement of the subsequent RF power or drain current transients [13,16,20]. Nevertheless, also these methods can only provide a local behavioral description around the imposed steady-state conditions and might, as well, reveal contradicting information on the time constants [13]. Unless an a-priori model formulation or a physics-based explanation is adopted, these characterizations alone cannot easily provide a global behavioral assessment of the large-signal trap dynamics.

This work proposes a general-purpose, black-box characterization useful to assess the global large-signal behavior of low-frequency dispersive effects, without any a-priori knowledge of the trap mechanics, nor any physics-based assumption. The approach exploits the wideband behavior and arbitrary generation capabilities of the proposed setup in order to devise a generalized transient testing procedure. A step-like excitation, namely a 50% duty-cycle waveform, is used. It implements a sufficiently large period so that any trap capture or release transient can be assumed to be extinguished, while the rise/fall time is minimized compatibly with the broadband capabilities of the hardware. The excitation is applied at both gate and drain ports, and all combinations of a user-defined subset of gate and drain voltages are generated, so that an extensive understanding of the global trapping behavior can be achieved. The method is applied to four state-of-the-art sub-0.15-µm GaN HEMT processes. The characterization is performed at different baseplate temperatures, investigating the temperature dependence and evaluating the characteristic time constants as from I-DLTS techniques. To the best of the authors' knowledge, this is the first comparison of trap dynamics behaviors among these many state-of-the-art sub-0.15-µm GaN HEMT processes for millimeter-wave applications.

The article is organized as follows. Section 2 introduces the technologies under test. Section 3 presents the custom on-wafer measurement setup and describes the characteriza-

tion approach. Section 4 depicts the extraction and the evaluation of trapping dynamics under large-signal conditions, as well as a comparison among the different technologies under test. Finally, conclusions are drawn in Section 5.

2. Description of the Samples under Test

Among the many variants of GaN process available, in this work, we measure four state-of-the-art processes from four different manufacturers, in which nominal values are reported in Table 1. In particular, all considered devices have the same number of fingers and periphery (4 × 50 µm). Three devices, labeled as **A**, **B**, and **C**, are 0.15-µm AlGaN /GaN HEMT devices on a SiC substrate. As such, they have superior thermal dissipation properties, displaying thermal resistances in the ∼50–60 K/W range.

Table 1. Details of the measured Gallium Nitride (GaN) devices. All devices-under-tests (DUTs) have a 4 × 50 µm periphery.

Label	A	B	C	D
Process	AlGaN/GaN	AlGaN/GaN	AlGaN/GaN	AlN/GaN/AlGaN
Substrate	SiC	SiC	SiC	Si
Gate Length (nm)	150	150	150	100
RF Power (W/mm)	3.5	3	4.2 @ 30 GHz	3.3
Gain (dB)	12 @ 30 GHz	13 @ 29 GHz	9 @ 35 GHz	13 @ 35 GHz
PAE (%)	>45 @ 30 GHz	>50	>50 @ 30 GHz	50 @ 35 GHz
Pulsed I_{DSS} (A/mm)	1.2	0.7	1.25	1.2
f_t (GHz)	>35	>35	>65	110
R_{TH} (K/W)	54 @ 25 °C	56 @ 25 °C	61 @ 25 °C	128 @ 25 °C
V_{BD} (V)	>70	>120	>60	>36
V_{TH} (V)	−3.5	−1.8	−2.5	−1.5

More in detail, devices **A** and **C** can handle similar pulsed current densities (I_{DSS}) in the order of 1.2 A/mm, and alike breakdown voltages (V_{BD}) in the 60–70 V range. At the same time, **C** shows a much higher nominal f_t and a slightly higher RF power density. Device **B**, instead, shows a much greater breakdown voltage ($V_{BD} > 120$ V), at the expense of a substantially lower current density (0.7 A/mm) and RF power density. Finally, **D** is a different technology employing a 0.1-µm AlN /GaN/AlGaN double-heterostructure on a Si substrate (with a process stack similar to the one reported in Reference [15]), displaying $R_{TH} \sim 120$ K/W, which corresponds to more than double with respect to the device on SiC substrate. This configuration can deliver a much higher $f_t > 120$ GHz and similar levels of RF power (at lower base plate temperature) and current densities, yet at the expense of lower V_{BD}. All devices feature peak power-added efficiency (PAE) levels of ∼50% and similar gain at millimeter-wave frequencies.

The static output characteristics at 40 °C for the four devices under test are reported in Figure 1a,b, while the measured voltage thresholds are reported in Table 1. Device **A** displays the smallest reduction in dc current with respect to the nominal pulsed values of pulsed I_{DSS}. This fact, together with the absence of a visible self-heating effects, highlights the good thermal performance of this process. Instead, Device **B** and **C** display the largest self-heating effect on the current, with its dc value decreasing for higher V_{DS} values and being significantly different from the pulsed I_{DSS}. Device **D** has been characterized in a restricted SOA due to thermal and voltage ratings of the double hetero-structure of the GaN-on-Si device. Nevertheless, the device displays a significant knee walkout at lower gate voltages, together with a single kink in the knee region. Both signatures have been linked to trapping behavior in GaN HEMTs [35].

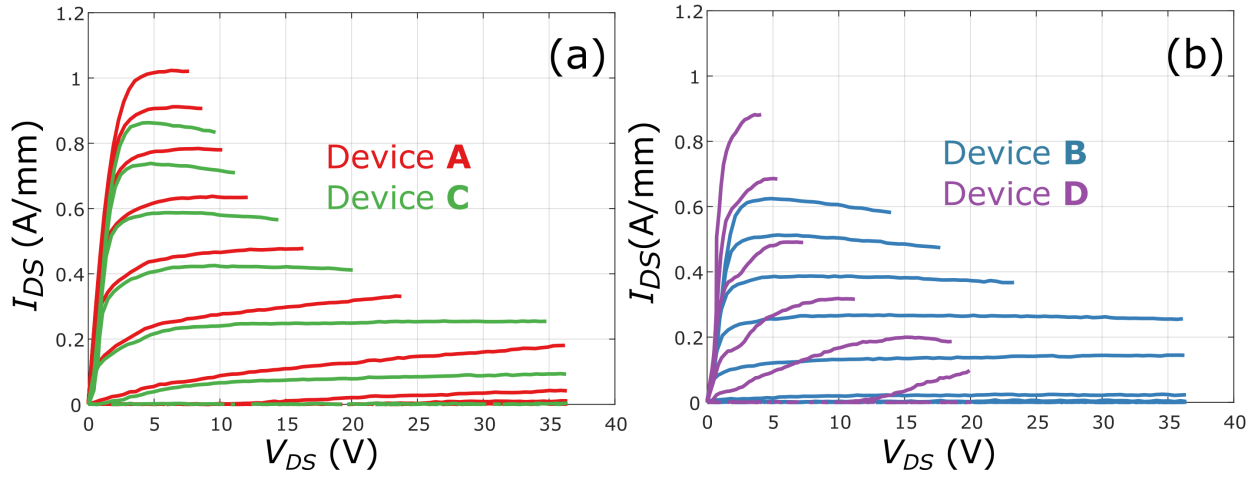

Figure 1. Output static characteristic for the four devices-under-tests (DUTs) at 40 °C. (**a**) Device **A** and **C**, V_{GS} swept from −5 V to 0 V in 0.5 V increments. (**b**) Device **B** and **D**, V_{GS} swept from −3.5 V to 0 V in 0.35 V increments.

3. Transient Multi-Bias Characterization Method

3.1. On-Wafer Measurement Setup

The proposed characterization takes advantage from a custom on-wafer measurement setup, reported in Figures 2 and 3 and firstly presented in Reference [15]. The devices-under-test (DUT) are on-wafer HEMTs in common source configuration (see Table 1 in Section 2), where gate and drain are accessed by 150-µm-pitch ground-signal-ground (GSG) probes. The excitations are concurrently applied at both gate and drain ports with a two-channel, 120-MHz arbitrary function generator (AFG) by Agilent (Santa Clara, CA, USA) (81150A), which features dc, pulsed, and arbitrary generation modes. Its output stage can deliver up to 20 V on an open-circuit load, hence the gate port can be directly controlled by one of the AFG channels without any additional conditioning. At the drain port, an analog driver based on a wideband current feedback amplifier (Analog Devices (Norwood, MA, USA)) ADA4870), featuring up to 50-MHz LS BW with I/V swings of up to 1 A and ∼38 V, is adopted for handling the electrical characteristics of the DUTs examined in this work. The pulsed excitations are applied through the low-frequency path of connectorized diplexers (SHF (Berlin, Germany) DX45) with 25-MHz nominal BW (dc coupled) on the low-frequency port, while the RF port of the diplexers are terminated to 50 Ω to enhance device stability.

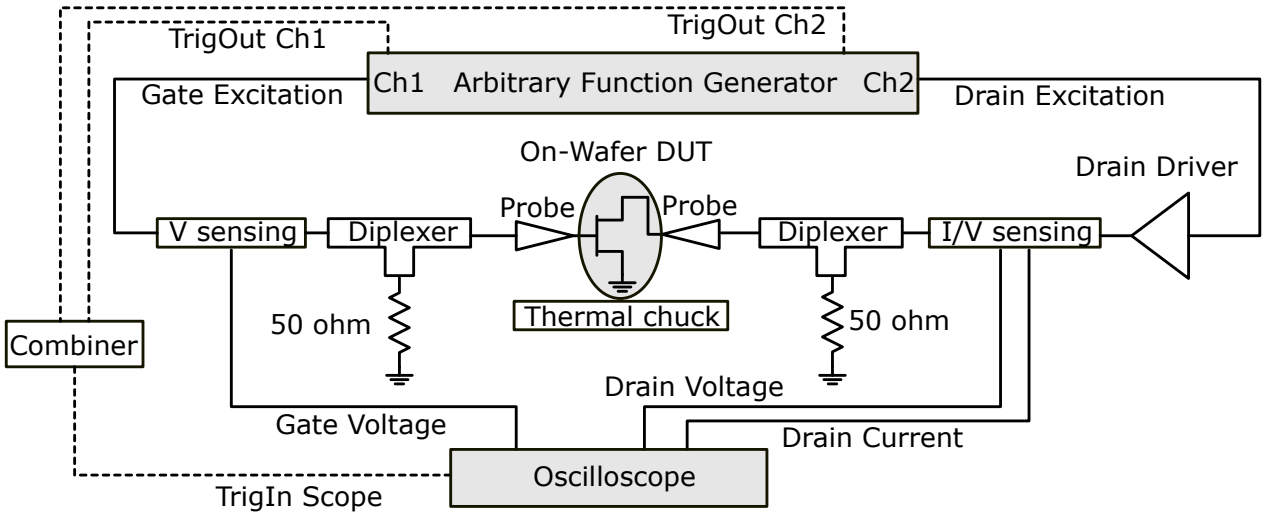

Figure 2. Block diagram of the measurement setup (10-MHz reference not shown).

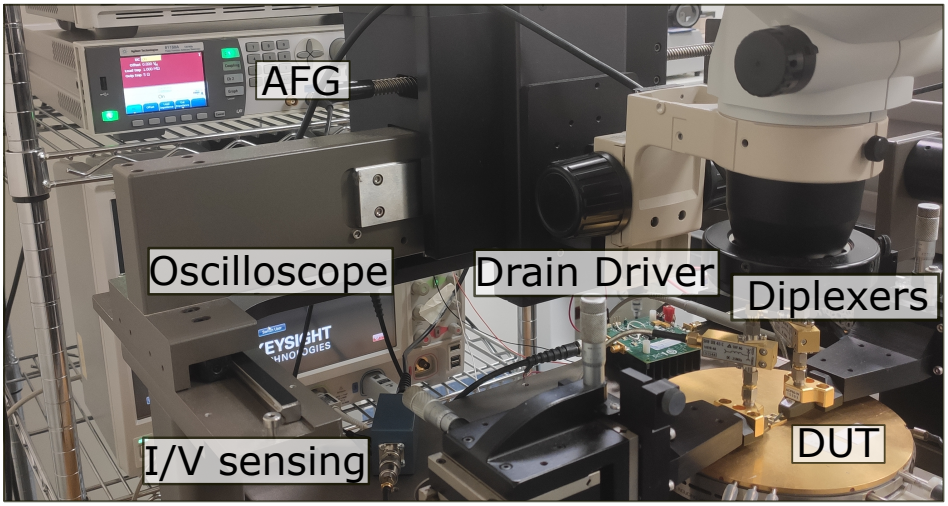

Figure 3. Photo of the on-wafer measurement setup.

The dynamic voltage waveforms are measured with commercial passive voltage probes, and the drain current is acquired with a 100-MHz current clamp probe (Keysight (Santa Rosa, CA, USA) N2893A). All the probes are connected to a 2.5-GHz BW, 20-GSa/s digital sampling oscilloscope (Keysight 9254A), which allows for wideband pulsed-waveform acquisition, as well as sufficient data memory, to capture ms-range pulse periods at high sampling rates. Hence, the setup allows us to accurately apply and measure step-like voltage waveforms with rise/fall times down to 100 ns without using pulse pre-emphasis techniques.

3.2. Measurement Technique

The flexibility of the proposed setup allows us to fully explore bias voltages across the safe-operating-area of the DUT, hence providing global device performance and complete assessment of the spurious behavior due to dispersive effects. In this work, the proposed characterization of dynamical effects is performed using two-level pulsed voltage excitations with 50% duty cycle applied concurrently on the gate and drain of the device. The chosen period for the excitation is $T = 100$ ms, which is deemed sufficiently large for practical compact modeling. Indeed, any additional current instabilities with duration of several seconds or more should rather be treated as long-term drifts. The chosen value for T allows for the concurrent measurement from all three channels (gate voltage, drain voltage, and current) in a single oscilloscope acquisition at a sufficiently high sampling speed, here selected at 100 MSa/s (10-ns sampling time). The edge-time of the excitation is set to 100 ns as a trade-off between the theoretical requirement for fast transitions and the available setup BW. An example of the employed excitation and generated current transient is shown in Figure 4, showing clean pulsed voltages. In Figure 4, a slow current recovery transient can be observed when the device is pulsed with the voltage transition $(V_{GQ,2}, V_{DQ,2}) = (-2, 36)$ V $\rightarrow (V_{GQ,1}, V_{DQ,1}) = (0, 8)$ V.

The idea behind the use of such waveforms is that, at equilibrium, the internal trapping state of the device is set exclusively by the applied voltages (and possibly, by the baseplate temperature T_c). The equilibrium is then perturbed by the stepped-voltage excitation, and the current transient is measured in order to behaviorally characterize the internal dynamics before a new equilibrium (i.e., the one set by the voltages after the step) is reached. In this respect, the drain current is used to probe the inaccessible internal trapping and thermal state of the device. If the period of the pulsed excitation is long enough to allow the current to recover to its dc value, the observed transient will only depend on the gate and drain voltages before and after the pulse (i.e., four variables in total, plus possibly T_c). If N points (V_{GQ}, V_{DQ}) are considered on the gate-drain voltage domain, a global characterization of the overall dynamical behavior can be obtained by applying pulsed

excitations among all the $\frac{N(N+1)}{2}$ possible combinations of two such points and recording the resulting current transients [36]. Given that the number of measurements increases quadratically with the number of points of interest, a subset of meaningful voltage points have to be selected to provide a reasonably small measurement time and manageable dataset size. This global excitation allows us to finely capture and analyze both the slow release and the fast charge capture transients, together with any superimposed dynamic self-heating effects.

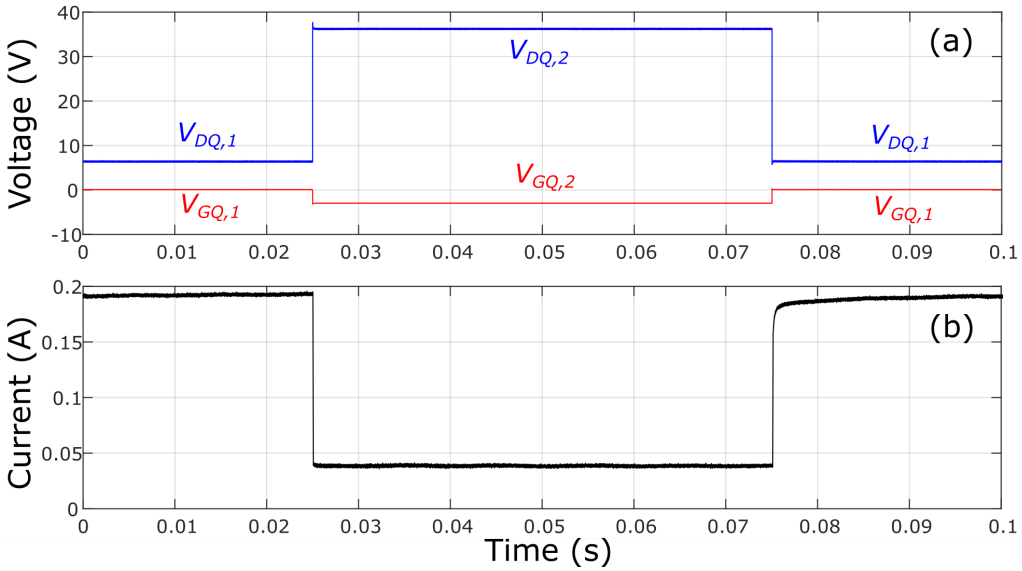

Figure 4. Example of (**b**) current transients acquired for (**a**) 50% duty-cycle voltage excitation applied at both gate and drain port. Each acquisition allows us to evaluate the response to the step-like transition $(V_{GQ,1}, V_{DQ,1}) \rightarrow (V_{GQ,2}, V_{DQ,2})$ and the complementary one $(V_{GQ,2}, V_{DQ,2}) \rightarrow (V_{GQ,1}, V_{DQ,1})$.

The main advantage of this method with respect to existing current-transient characterization techniques [13,25,26] lies in the ease of design of experiments. As long as steady-state conditions are reached, no prior hypotheses on the relative value of trapping, de-trapping and thermal time constants has to be made in order to design specifically-tailored multiple filling pulse durations or amplitudes. Therefore, the proposed technique is well-suited for a general-purpose behavioral characterization of dynamical effects in GaN devices, in which specific behavior [36], as it will be discussed in Section 3, strongly depends on the details of the fabrication process and the applied voltages. Moreover, many of the well-known characterizations will be available as a subset of this complete dataset.

As an example, let us consider Figure 5, reporting the V_{GS}-V_{DS} plane (Figure 5a) and the corresponding output characteristic (Figure 5b) of the HEMT for the device **A**. Three key voltage coordinates have been selected as from the classical gate/drain-lag characterization, namely: *GL*, corresponding to the minimum gate voltage ($V_{GQ} = -5$ V for device **A**) and $V_{DQ} = 0$ V; *DL*, corresponding to $V_{GQ} = 0$ V and to the maximum drain voltage ($V_{DQ} = 36$ V as per limitation of the drain driver); *ZZ*, corresponding to (V_{GQ},V_{DQ}) = (0,0) V. All these points feature zero power dissipation. The measurement of the drain current transient just after the step-like transitions among one these points and another one on the IV plane will allow us to quantify the typical gate/drain-lag performance, as well as observe trap dynamics. Indeed, this evaluation has been shown to be important in order asses the expected amount of current reduction due to trapping in a given technology [37], although it might lead to an overestimation of the performance reduction that can be encountered in RF applications [38], depending on the exact values of the applied voltages and the capture/release equilibrium established at RF.

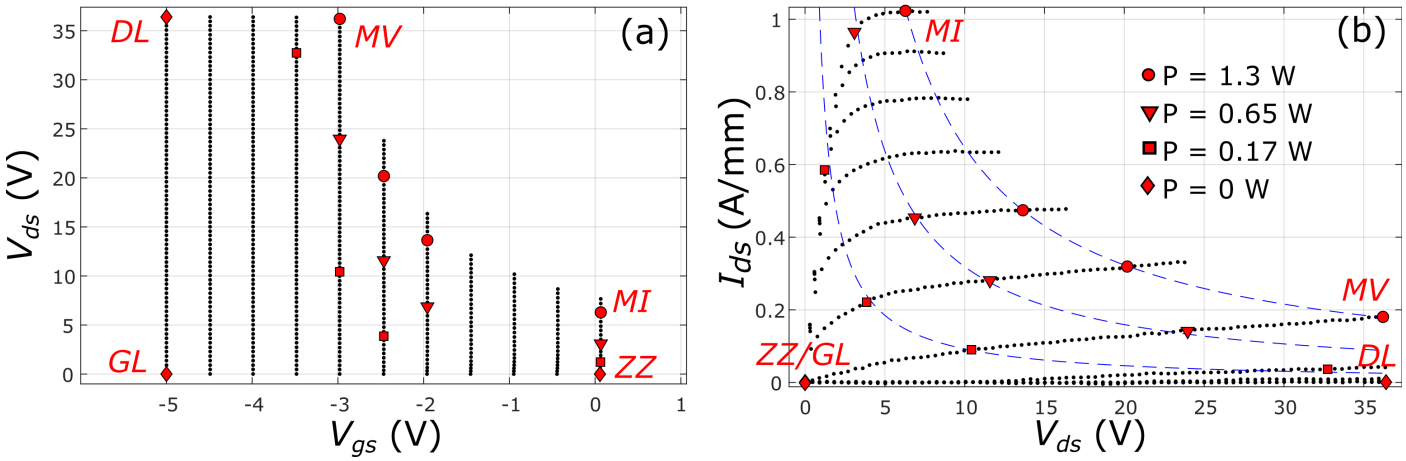

Figure 5. Selection of a meaningful subset of quiescent points from the static-IV characteristic of the device. The three key quiescent points for gate/drain-lag characterization *GL*, *DL*, and *ZZ* are at zero dissipated power. The other selected quiescent points are found on three iso-thermal IV-characteristics at dissipated powers 1.3 W, 0.65 W, and 0.17 W. (**a**) $V_{GS} - V_{DS}$ plane. (**b**) Static-IV characteristic for device **A** at T_C = 40 °C.

Other quiescent points to be included in the transient characterization dataset have been automatically chosen on the dc current characteristic of the HEMT (Figure 5b), which is preliminarily measured. On this characteristic, a limited number of iso-thermal profiles are selected, including the iso-thermal profile with the maximum dissipated power compatible with the maximum baseplate temperature considered for test (here, maximum $T_C = 80$ °C). As an example, for the device **A** in Figure 5b, the maximum-temperature iso-thermal profile has been measured at 1.3 W. Then, the maximum-current (*MI*) and maximum-voltage (*MV*) points of such iso-thermal profile are included in the subset of quiescent points for transient characterization. Additional quiescent points are finally selected on the other iso-thermal curves by maximizing the voltage swings and the exploration of the V_{GS}-V_{DS} plane. Similarly to Reference [39], this strategy allows us to measure current transients subject to the same thermal conditions yet with different applied voltages, permitting the separation between thermal and trapping dynamic effects. Eventually, the typical dataset collected for each measurement campaign on a given device involved a total of $N = 15$ quiescent voltages, resulting in 120 step-like transitions.

Considering the behavior of traps in GaN and their fast capture mechanisms for increasing V_{DS} and decresing V_{GS} [24], each transition $(V_{GQ,1}, V_{DQ,1}) \rightarrow (V_{GQ,2}, V_{DQ,2})$ and the complementary one $(V_{GQ,2}, V_{DQ,2}) \rightarrow (V_{GQ,1}, V_{DQ,1})$ must be designed to avoid triggering any spurious fast trap capture during the rise/fall step times. Indeed, this unwanted charge capture and its effect on the drain current would contribute to excite a different trapping dynamics that is not unambiguously determined by the user-programmed quiescent voltage pairs, but possibly also by the voltage states rapidly traversed during the transition.

The problematic situations are graphically depicted in Figure 6, shown in grey the regions not to be crossed during the transition. In case (I), the pulse is applied between the α and β voltage points. If the instantaneous voltage, either during to $\alpha \rightarrow \beta$ or the $\beta \rightarrow \alpha$ transition crosses the grey region, the trapped charge might be higher in one of the traversed states than in either α or β. As charge capture is typically orders of magnitude faster than charge release, even a fast transition in the forbidden area would be enough to set a new trapping state [29]. Then, the observed transient would be dominated by the slow de-trapping from this intermediate spurious state, obscuring the actual $\alpha \leftrightarrow \beta$ transients of interest. Conversely, by following the drawn trajectory in Figure 6, any unwanted side effect is avoided. In case (I), considering that the user-selected β point is the one with the highest current of the whole trajectory, there is no concern that the device will dynamically exit the SOA.

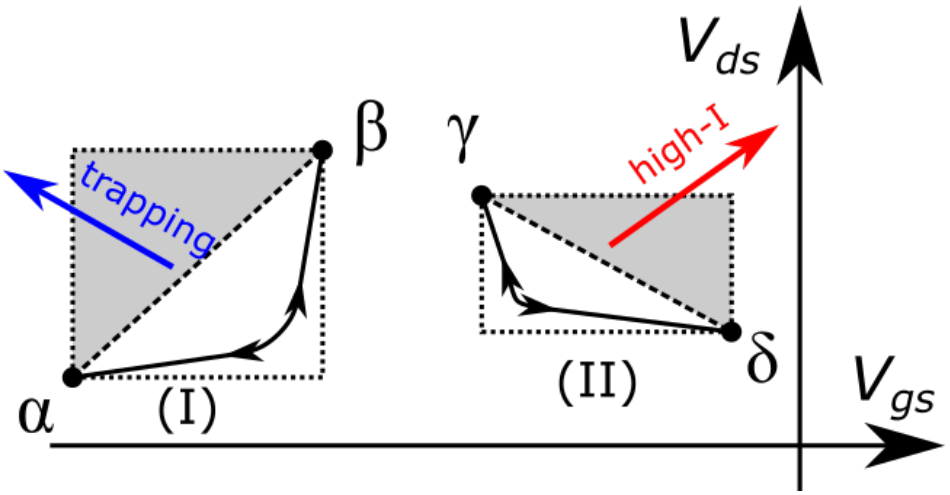

Figure 6. Graphical representation of two main cases (I) and (II) for the transitions between two quiescent voltage points. The showed trajectories allow to avoid exciting spurious fast charge capture and non-reversible high-current effects.

In case (II), γ is expected to be the point with the highest amount of trapped charge, whereas δ is the one with the lowest amount, irrespective of the chosen trajectory. Therefore, there is no concern of spurious intermediate trap captures impacting the transient response. On the other hand, a trajectory crossing the grey area would possibly display increased stress conditions with respect to either δ and γ, thereby exiting the SOA of the device. Even if this crossing happens during the fast transition between the voltage points, the intermediate points might feature higher instantaneous currents and junction temperatures, possibly causing damage to the device or altering the observed transient response. In all cases, the required trajectory can be enforced by accurate timing of the pulsed waveforms, with a carefully controlled overlapping of the 100-ns-long pulse edges.

4. Experimental Characterization of Trapping Dynamics

4.1. Gate/Drain-Lag

In order to compare the dynamical effects of the different device technologies introduced in Section 2, a significant subset of the overall set in Figure 5 has been selected. The set contains the *GL*, *DL*, *ZZ*, *MV*, and *MI* points in order to provide a global characterization of the thermal and trapping phenomena. The actual voltage and dissipation values used on the iso-thermal line for *MI* and *MV* are described in Table 2.

Table 2. Voltage values (V_{GQ}, V_{DQ}) and power dissipation points selected for the devices **A**–**D**.

Label	A	B	C	D
Gate Lag Point-*GL* (V)	(−5, 0)	(−3.5, 0)	(−5, 0)	(−3, 0)
Drain Lag Point-*DL* (V)	(−5, 36)	(−3.5, 36)	(−5, 36)	(−3, 20)
Max Voltage Point-*MV* (V)	(−3, 36)	(−1.4, 29)	(−2, 17.5)	(−1.2, 18.5)
Max Current Point-*MI* (V)	(0, 6.3)	(0, 6.8)	(0, 4.6)	(0, 3.9)
Power Dissipation (W)	1.3	0.8	0.8	0.7

Figure 7a,b detail all the possible transitions among these five points displaying a non-zero current, as its value is used to probe the trapping state of the device.

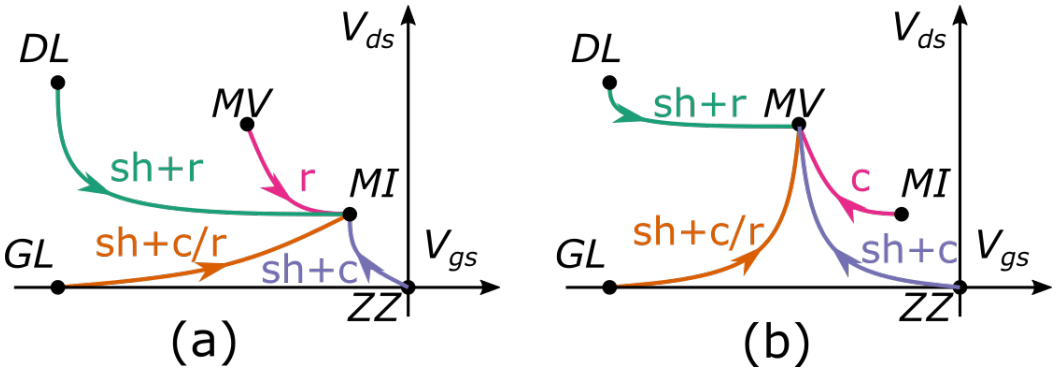

Figure 7. Graphical representation depicting all the relevant trapping/de-trapping transitions on the $V_{GS} - V_{DS}$ plane from the *ZZ*, *GL*, *DL* points to the *MI* (**a**) and *MV* points (**b**). The involved processes are highlighted on the transitions: self-heating (*sh*), charge capture (*c*), and release (*r*).

Each transition displays a different combination of capture/release and thermal transients, which is often overlooked in typical gate/drain-lag characterizations. For example, the charge release and self-heating transient from *DL* in Figure 8 displays a regular increase of the current due to de-trapping, but also a clearly identifiable current decrease at the ∼1 ms mark, likely linked to self-heating.

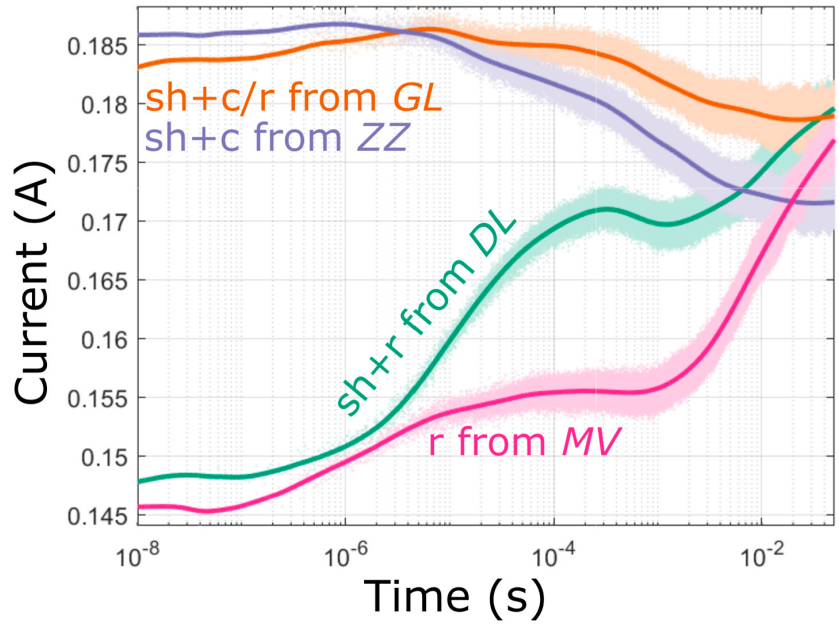

Figure 8. Time-domain current transients from *ZZ*, *GL*, *DL* to *MI* points for device **D** at T_c = 40 °C. Lighter shades of color identify acquired points, while solid lines are smoothed versions of the current transient.

The additional *MV*-*MI* transitions (across static points sharing the same static power dissipation) can be used to separate self-heating effects and charge trapping ones even when they are not visually separable. Indeed, the thermal signature is absent in the charge release iso-thermal transient from *MV*, despite the very similar voltage pulsing conditions. This difference in behavior can therefore likely be attributed to the existence of a dynamic self-heating phenomenon, and its analysis is critical when the assumption of an instantaneous self-heating, suggested in Reference [40], is not applicable.

Alternatively, current drops can also be interpreted as pointing to the spurious charge capture processes, which have indeed been shown to be present in some GaN technologies [32], but the use of iso-thermal transients seems to exclude this hypothesis in the DUT. Anyway, the use of a complete dataset can be employed in order to partially untangle

the reciprocal relationship between thermal and trapping phenomena, avoiding spurious identifications of each dynamical effect.

As an example of the proposed global characterization, time-domain transients for device **A** at $T_c = 40$ °C are reported in Figure 9. In all the cases, the current displays almost complete recovery to equilibrium, identified by the common endpoint of all the transients. By first examining the transients towards the *MI* point (Figure 9a), it is possible to notice that the measurement from *ZZ* shows a minor trapping and self-heating current decrease transient. Similar behavior is observed when pulsing from the *GL* point, highlighting the relative absence of strong gate-lag effects in the device. On the other hand, relevant increasing current transients are excited when pulsing from either *MV* or *DL*, pointing to the existence of significant slow de-trapping dynamics triggered by lower drain voltage. While the initial current drop with respect to the equilibrium dc value is similar in both cases, the transient displays a significantly different emission time. The difference can be likely attributed to the different initial thermal state between the two cases, as the *MV* point is iso-thermal with *MI*, while *DL* is not. The difference in V_{GS} between these two cases is instead likely to have a minor impact on the difference in transients, as shown by the limited gate-lag transient.

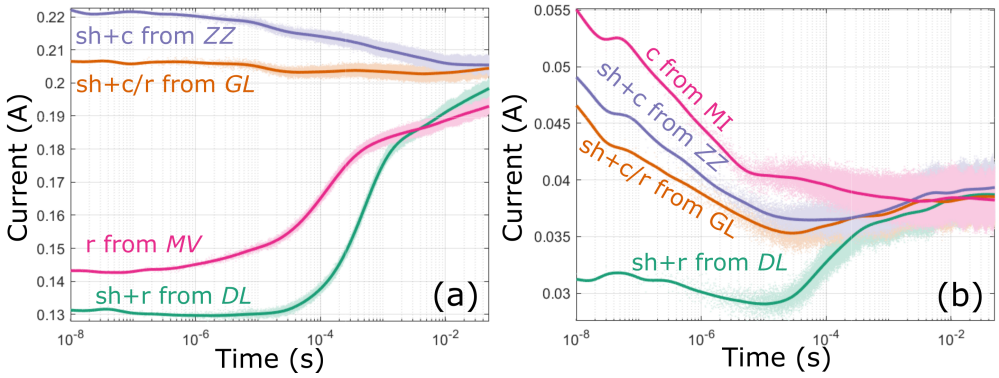

Figure 9. Time-domain current transients from *ZZ*, *GL*, *DL* to (**a**) *MI* and (**b**) *MV* points for device **A** at T_c = 40 °C. Lighter shades of color identify acquired points, while solid lines are smoothed versions of the current transient.

The observation of the transients towards the *MV* point (Figure 9b) highlights the existence of fast capture processes ($\leq$100 ns) when observing the currents from the iso-thermal *MI* point. The absence of evident peaks in the derivative for trapping transients points to the fact that trapping might indeed be faster than the 10 ns sampling rate used. Similar behavior is observed also in the pulses from the *ZZ* and *GL* point, highlighting that the measured transient is mostly due to the trapping state in the high drain voltage *MV* point, with minor influence of self heating. On the other hand, the drain-lag case displays an observable de-trapping transient, marked by the overall increase of the current towards equilibrium. The transient also embeds a dynamical self heating effect, identified by the temporary decrease of the measured current in the 1–10 µs range. The co-existence of both phenomena, as highlighted in the previous section, has to be taken into account for the formulation of behavioral models, as well as for the investigation of specific physical mechanisms. Similar considerations can be drawn for devices **B**, **C**, and **D** (not shown).

The collected dataset can be also used in order to extract gate-lag and drain-lag metrics of each device, allowing for a detailed technology comparison. By examining the start of each transient (in this case, the first 100 ns), one deduces the current that would be measured within the short pulse in a classical PIV setup. Figure 10 compares the percentage current drop measured at the *MI* point by pulsing from *DL*, *GL* and *MV* points with respect to the value obtained from the *ZZ*. Despite the different technologies, all the devices display a reduced gate lag effect. Gate lag has been linked mostly to surface states, in which effects have been shown to be greatly reduced by surface passivation and the use of field plates [37,41].

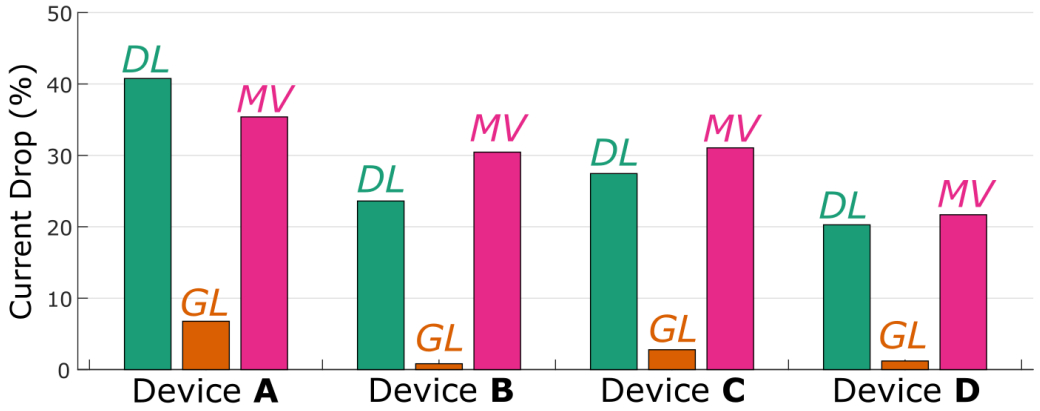

Figure 10. Percentage current drop measured at the *MI* point by pulsing from *GL*, *DL*, and *MV* points with respect to the value obtained from the *ZZ* point for devices **A**–**D** at T_c = 40 °C.

On the other hand, drain lag effects are still quite relevant in all the cases, with current drops in the order of 20–40% to be mainly attributed to the charge capture mechanisms activated statically. The drop observed for the iso-thermal *MV* point (which features different voltage values for the four DUTs; see Table 2) closely mimics the one seen for the similar *DL* point, yet it is unexpectedly larger for **B**, **C**, **D** devices. In fact, both *ZZ* and *DL* are zero-dissipation points, whereas *MV* involves a non-zero and different dissipation for the four DUTs. A higher operating temperature due to self-heating imposes a different starting state, causing various effects on the drain current transient and reducing the electron mobility but also modifying the threshold voltage, as well as trap release times. This result highlights that the complex dynamic behavior can still be significantly different than expected, and that a characterization just based on the classical gate/drain-lag experiment is not comprehensive enough for an accurate behavioral description.

4.2. I-DLTS and Arrhenius Analysis

The large number of current transients acquired can also be used in order to identify dynamical trapping signatures in the DUTs. Following the procedure in Reference [31], time-constants specific to each trapping process can be found as peaks in the I-DLTS trace, which can be obtained as the log-time derivative of the observed current transient. The amplitude of the peak, instead, is related to the amplitude of the current swing occurring during the transient.

An Arrhenius-type analysis is normally used to identify trap energy levels by observing the variation of de-trapping time constants (i.e., peaks in I-DLTS) with temperature. The working hypothesis is that the de-trapping process is mainly thermal in nature, becoming faster at higher operating temperatures [15]. The actual current levels and trap signatures strongly depend on the process technology and applied voltages, and can give valuable clues on the actual transport nature and locations of the trap centers, such as distinguishing between defects at interfaces between materials, surface states, and (un)intentional doping in the buffer. Nevertheless, similar signatures and energy levels can still be linked to several different physical causes [32,42], and a detailed knowledge of the technological process and specific measurement techniques are required in order to further discriminate between the effects [15]. However, this type of investigation lies beyond the scope empirical characterization proposed in this work.

In order to compare the dynamic behavior of the different technological solutions adopted in devices **A**–**D**, de-trapping current transients were examined after the $DL \rightarrow MI$ transition at different baseplate temperatures in the range T_c = 40–80 °C. In this way, it is possible to activate buffer-related traps at high drain voltages, which is the worst-case scenario in terms of trapping, provided that gate-related effects have been observed to be quite limited for all the examined devices. As the different devices display different current

densities, the I-DLTS in this case is normalized by the dc current at MI, so to assess the impact of the trapping transient relative to the respective quiescent value.

Both the current transients and the I-DLTS traces are reported for all devices in Figure 11a–d. Figure 12, instead, collects the resulting Arrhenius plots, together with the apparent activation energy for the traps in each device.

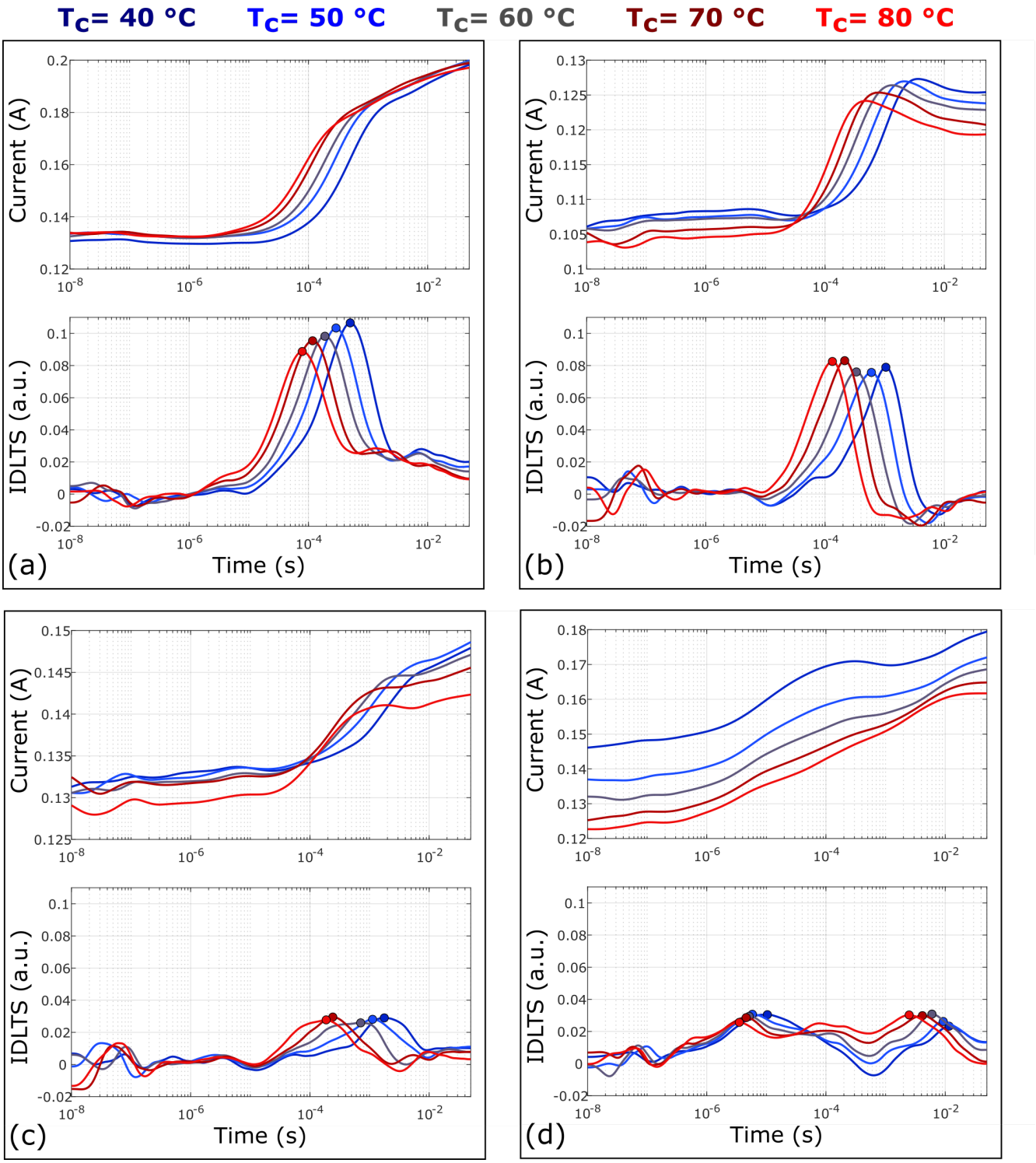

Figure 11. Comparison of the current transients (top plots) and the corresponding time-derivative traces (bottom plots) among the four studied technologies for a baseplate temperature range T_c = 40–80 °C. The time-derivative traces are referred to as I-DLTS as from Reference [31]. Devices **A**–**D** are reported in (**a**–**d**), respectively. The transients correspond to the $DL \rightarrow MI$ transition, with values as from Table 2.

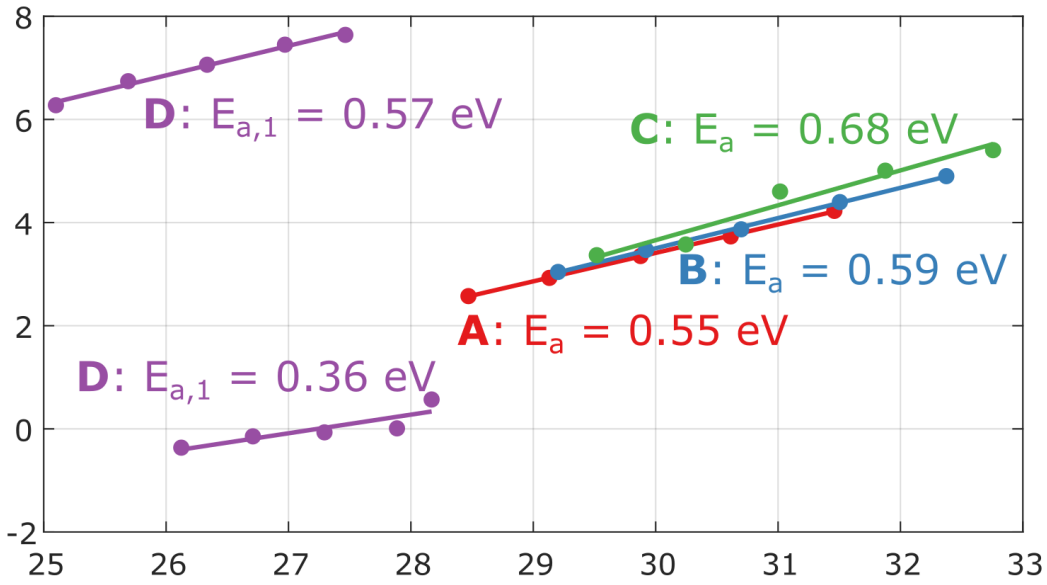

Figure 12. Comparison of the Arrhenius plots among the four technologies considered. Silicon Carbide (SiC)-based devices (**A** to **C**) share a similar trapping signature and apparent activation energy, whereas the Si-based device (**D**) reveals a different behavior involving two trapping signatures.

As it can be observed, all devices under test display some degree of trapping, albeit with different severity and characteristics. Devices **A** and **B** display a single pronounced peak in the 10^{-4} s range, with an activation energy of 0.55 eV and 0.59 eV, respectively. Although the presence of a back-barrier to improve electron confinement might not be ruled out, the measured energy levels and the clear single-peaked signature strongly correlate with Fe-doping in the GaN buffer layer [32]. As often reported in literature, the intentional introduction of acceptors (such as C or Fe) is used to enhance the performance of the buffer by increasing the substrate resistivity and the breakdown voltage while, at the same time, improving electron confinement and reducing short-channel effects. Moreover, the slightly larger thermal resistance for **B** is just marginal, whereas the presence of a back-barrier is known to display greater increases in thermal effects [43].

Devices **C** and **D**, instead, present strong non-exponential behavior, with significantly broadened spectral peaks in the I-DLTS traces and a less pronounced current transient. In both cases, the trapping mechanisms still show a significant thermal activation of the de-trapping process, ruling out temperature-independent transport phenomena [32]. The linear fit predicted by the Arrhenius model is also less accurate in both the examined cases. These peculiar signatures are likely to rule out acceptor buffer doping, but can be traced back to a large variety of defects introduced by the fabrication process [32], whose exact identification lies beyond the scope of the present paper.

In particular, the GaN-on-Si device (**D**) presents two different trapping locations (one at ∼10 µs and the other at ∼10 ms) with significantly different activation energies. The extraction of the I-DTLS profiles for this device is performed at a higher temperature than others, due lower thermal resistance and higher self-heating in the structure. The presence of an AlGaN back barrier in device **D** for improving electron confinement realistically rules out the presence of intentional buffer doping. However, the exact cause is unclear and might be related to higher amount of defects that are usually observed in double-heterostructure and GaN-on-Si devices [11,15]. In fact, the I-DLTS characterization is not conclusive in determining the physical effects behind the trapping processes for devices **C** and **D**.

In all the examined cases, due to the conditions chosen for the I-DLTS characterization, the transient is not iso-thermal and is indeed subject to thermal dynamics. This effect can be noticed, for example, in Figure 11b,d, where the increase of current due to de-trapping is followed by a decrease due to self-heating. The comparison with the iso-thermal transients

discussed in Section 4.1 allows us to reasonably exclude the existence of specific charge capture processes in the examined situations.

5. Conclusions

The present work proposes a novel time-domain charge trapping characterization technique for GaN HEMTs. The proposed method generalizes several well-known trap signature characterization techniques, such as gate/drain-lag and I-DLTS, and expands their capabilities by providing a complete exploration of the transient behavior across the SOA of the DUT. The acquired dataset is used in order to compare four different state-of-the-art sub-0.15 μm GaN devices for mm-wave applications, both on SiC and Si substrates.

All the different technologies display different degrees of charge trapping, with extracted de-trapping time constants on the order of 10 μs–10 ms, which can critically interfere on the performance of typical telecommunication applications with modulation frequencies in that range, e.g., 5G. While gate-lag phenomena related to surface traps seem modest with respect to previous technological generations, drain lag is still significant for all the examined devices, with the greatest effect displayed by technologies employing buffer acceptor doping for charge confinement.

The large variety of charge capture and release behavior observed between different processes, and their coupling with self-heating phenomena, highlights the need for general-purpose, compact behavioral models of traps for microwave circuit design.

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