Input current and voltage ripple analysis in ldn cells for h-bridge multilevel inverters

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2019.2896119, IEEE Transactions on Industrial Electronics

Input Current and Voltage Ripple Analysis in Level Doubling Network (LDN) Cells for H-Bridge Multilevel Inverters

M. Hammami, *Member, IEEE*, and G. Grandi, *Senior Member, IEEE*

***Abstract*— This paper deals with the analysis of the input dc-link voltage ripple in multilevel inverter based on H-bridge and level doubling network (LDN). The LDN is basically a half-bridge fed by a floating capacitor, with voltage self-balancing capability, recalling the concept of a flying capacitor configuration. The amplitude of the LDN voltage ripple is analytically determined considering both the low-order and the switching harmonic components. In particular, peak-to-peak distributions of voltage ripples over the fundamental period are analytically determined, making possible the design of dc-link capacitor relying only on the dc-voltage ripple requirements. The case study makes reference to negligible switching ripple in the output current. It well represents either grid connection or passive load having almost sinusoidal currents. Numerical simulations carried out by Matlab/Simulink and a complete set of experimental verifications are given to confirm the theoretical developments.**

***Index Terms*— DC-link voltage ripple, multilevel inverter, level doubling network, dc-link capacitor design.**

I. Introduction

In recent years, multilevel inverters have become more attractive for single-phase systems, due to their known advantages over conventional H-bridge pulse width-modulated (PWM) inverters. They offer improved output waveforms [1], [2], [3], smaller filter size, lower total harmonic distortion (THD), and higher output voltages [4], [5], [6].

The most common multilevel converter topologies presented in literature are the neutral-point-clamped (NPC), flying capacitor (FC), and cascaded H-Bridge (CHB) converters [7], [8]. In both NPC and FC configurations, the number of additional components (diodes or capacitors) proportionally increases with the number of levels, leading to lower reliability, higher complexity, volume, and cost. The cascaded H-bridge configuration is a flexible solution to increase the number of output voltage levels. This solution doesn't require additional components in comparison with aforementioned NPC and FC counterparts, but it needs an isolated dc power source for each H-bridge unit.

Manuscript received May 24, 2018; revised July 25, November 1, and December 26, 2018; accepted January 12, 2019.

M. Hammami and G. Grandi are with the Department of Electrical, Electronic, and Information Engineering, University of Bologna, Bologna, 40136. Italy. (e-mail: manel.hammami2@unibo.it; gabriele.grandi@unibo.it).

In order to improve the ratio between the number of output voltage levels and the number of components, several hybrid and asymmetric topologies of multilevel inverters have been proposed in the literature [9]-[13].

In [12], a novel PWM modulation strategy has been proposed for the FC asymmetric H-bridge (FCaHB) where only six power switches and one capacitor are needed. A design of the flying capacitor has been presented taking into account only the dc-link voltage ripple at the switching frequency.

An NPC asymmetric H-bridge (NPCaHB) topology has been proposed in [9], but this solution needs two dc-link capacitors and two supplementary diodes in comparison to the FCaHB topology.

Another asymmetric multilevel inverter that can be adopted in a wide variety of applications is the cascaded asymmetric H-bridge (CaHB). Its structure is based on a full H-bridge cascaded with a half-bridge module (two switches) in order to double the output voltage levels (also called level doubling network, LDN). This solution is quite similar to the FCaHB, just with a different disposition of the half-bridge, as shown in Fig. 1 (a) and (b). The CaHB topology is becoming popular, due to its simple, modular, and reliable structure. The LDN can also be considered as a retrofit to existing H-bridge configurations with the purpose to double the output voltage levels [5], [11].

Despite the LDN topology has been already presented in [5] and [11], only nearest voltage level control (staircase modulation) was exploited to support the LDN operations. Any PWM modulation strategies for LDN converters have not been reported yet. The analysis of the dc-link capacitor current and voltage ripple in single-phase H-bridge inverters have been presented in [14]-[15]. Dc-link current and voltage ripples

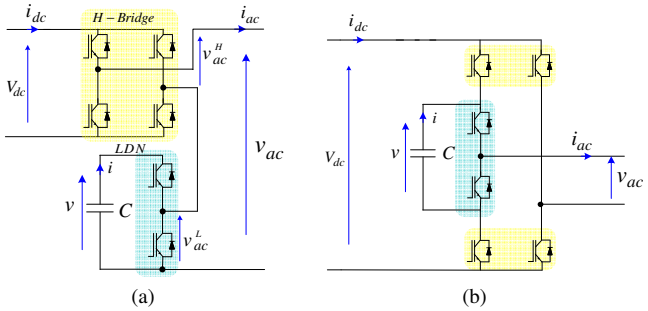

Fig. 1. Basic circuit scheme of considered single-phase multilevel inverters (a) CaHB (H-bridge and LDN), and (b) FCaHB (asymmetric H-bridge legs).

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have been investigated for other asymmetric single-phase multilevel inverter configurations, specifically for NPCaHB in [9] and for FCaHB in [12].

A multilevel PWM strategy for cascaded asymmetric H-bridge inverters (H-bridge plus LDN) is introduced in this paper. Furthermore, comparing to [5], the concept of self balancing capability for the LDN capacitor has been analytically proved. A detailed analysis of the dc-link current and voltage ripple for the LDN cell is developed, as an extension of [15] to multilevel inverters. In particular, the peak-to-peak dc-link current and voltage ripple amplitudes are analytically calculated over the fundamental period as a function of the modulation index. Both the low-frequency and the switching ripple components have been separately considered. Reference is made to sinusoidal output current, considering the output power phase angle as a degree of freedom.

Maximum peak-to-peak values of both low-frequency and switching frequency voltage ripple components can be effectively adopted to design the capacitor of the LDN cell basing on the desired dc-link voltage ripple requirements.

The paper is organized as follows. In Section II the system configuration and the modulation principle are introduced. Section III presents the analysis of low-frequency and switching frequency current components of the LDN cell, whereas in Section IV the analysis of the dc-link voltage ripple is introduced. Section V defines the guidelines for designing the LDN capacitor. In Section VI simulation and experimental verifications have been reported, and the conclusions are presented in Section VII. Specific analytical developments are given in the Appendix A and the concept of self-balancing of LDN voltage is analytically proved in Appendix B.

II. System Configuration and Modulation Principle

A. System configuration

The considered converter circuit is represented in Fig. 1 (a). It consists of a multilevel inverter supplying a sinusoidal ac output current (i_{ac}) representing either the grid or a passive load. The multilevel inverter is realized by a full H-bridge (supplied by a constant dc source voltage V_{dc}) connected in series with a half-bridge (LDN, supplied by a floating capacitor).

A proper PWM pattern has been adopted, as described in the next sub-section, providing for a self-balancing mechanism. In particular, the steady-state LDN average dc-link voltage is spontaneously kept around the half of the dc-link voltage of the H-bridge, i.e. $v \approx V_{dc}/2$, as proved in Appendix B in the case of symmetric LDN operations.

The instantaneous output voltage v_{ac}, normalized by V_{dc} and averaged over the switching period (overline), is determined within the linear modulation range as:

$$\overline{u}_{ac} \cong u_{ac} = m \sin\vartheta, \tag{1}$$

being u_{ac} the normalized reference output voltage, $\vartheta = \omega t$ the phase angle, $\omega = 2\pi/T$ the fundamental angular frequency, T the fundamental period, and m the inverter modulation index.

B. Modulation Principle

In order to obtain a proper multilevel output voltage waveform with self-balancing capability (normalized LDN voltage equal to 1/2), a modulating signal for the LDN is proposed in the following original compact form:

$$u_{ac}^{L} = \begin{cases} |u_{ac}|, & |u_{ac}| \le 0.5 \\ 1-|u_{ac}|, & |u_{ac}| \ge 0.5. \end{cases} \tag{2}$$

For the H-bridge, the modulating signal can be obtained as

$$u_{ac}^{H} = u_{ac} - u_{ac}^{L}, \tag{3}$$

leading to the following original compact form:

$$u_{ac}^{H} = \begin{cases} u_{ac} - |u_{ac}|, & |u_{ac}| \le 0.5 \\ u_{ac} - 1 + |u_{ac}|, & |u_{ac}| \ge 0.5. \end{cases} \tag{4}$$

Modulating signals (1)-(4) and normalized instantaneous output voltages are depicted in the examples of Figs. 2 and 3 for m = 0.5 and 1, respectively.

III. Analysis of LDN Input Current

The current through the LDN capacitor i is composed by its averaged value over the switching period $\bar{i}$ and the instantaneous switching ripple Δi. The averaged value over the switching period consists of the dc component I (I=0 in the case of steady-state balanced operation) and the low-frequency component $\tilde{i}$, i.e., the set of current harmonics with a frequency much lower than the switching frequency:

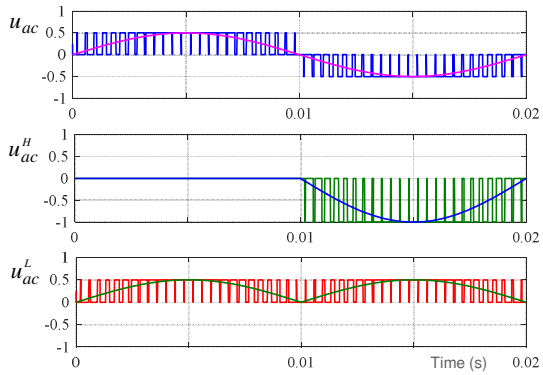

Fig. 2. Modulating signals and instantaneous output voltage normalized by V_{dc} in case of m = 0.5: total (u_{ac}), H-bridge (u_{ac}^{H}), LDN (u_{ac}^{L}).

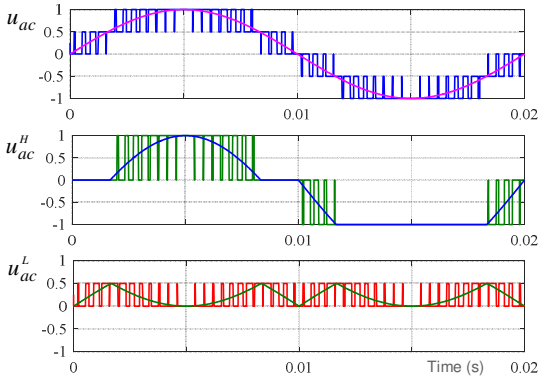

Fig. 3. Modulating signals and instantaneous output voltage normalized by V_{dc} in case of m = 1: total (u_{ac}), H-bridge (u_{ac}^{H}), LDN (u_{ac}^{L}).

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$$i = \bar{i} + \Delta i = I + \tilde{i} + \Delta i \,. \tag{5}$$

The analysis of the LDN input current is developed on the basis of the input-output power balance of the LDN cell, considering the averaged quantities over the switching period (T_{sw}=1/f_{sw}). Supposing that the normalized LDN input voltage is almost constant and equal to 1/2, the power balance of the LDN cell can be written as:

$$\tfrac{1}{2}\,\bar{i} = \bar{u}_{ac}^{L}\,\bar{i}_{ac} \,. \tag{6}$$

A. Low-frequency (averaged) current component

The output current is supposed to be almost sinusoidal:

$$i_{ac} = I_{ac}\,\sin(\vartheta - \varphi) \approx \bar{i}_{ac} \,, \tag{7}$$

where I_{ac} is the current amplitude and φ is the phase angle. The corresponding output voltage is given by (1). Replacing (1), (2), and (7) in (6), the input LDN current can be analytically calculated as

$$\bar{i} = \tilde{i} = \begin{cases} 2\,m\,I_{ac}\,\sin(\vartheta-\varphi)\,|\sin\vartheta|\,, & m\,|\sin\vartheta| \le 0.5 \\ 2\,I_{ac}\,\sin(\vartheta-\varphi)\,(1-m\,|\sin\vartheta|)\,, & m\,|\sin\vartheta| \ge 0.5. \end{cases} \tag{8}$$

It should be noted that (8) represents the low-frequency component, being null the dc component (I = 0) due to the waveform symmetry in the balanced case $v \cong V_{dc}/2$. Similar results have been analytically obtained in [9] for the neutral point capacitor current in case of NPCaHB converter, and numerically in [12] in case of FCaHB, having different circuit topology, and only considering the case of unity power factor.

The input LDN current (8) contains just odd harmonics, and its harmonic spectrum is given by (Appendix A):

$$\tilde{i} = -I_{ac}\left\{U_2\sin(\vartheta+\varphi) - 2U_0\sin(\vartheta-\varphi) + \right. \\ \left. + \sum_{n=3}^{\infty}\left[U_{n+1}\sin(n\vartheta+\varphi) - U_{n-1}\sin(n\vartheta-\varphi)\right]\right\}, \tag{9}$$

where $n \ge 3$ is an odd number.

B. Switching frequency current component

Once the low-frequency component is determined by (8), the LDN switching current component Δi can be calculated basing on (5). In particular, during the "on-time" and the "off-time" of the upper LDN power switch, it becomes:

$$\begin{cases} \Delta i_{on} = I_{ac}\sin(\vartheta-\varphi) - \tilde{i} \\ \Delta i_{off} = -\tilde{i} \,. \end{cases} \tag{10}$$

Introducing (8) in (10), and considering the "on-time", the switching ripple component of the LDN input current can be expressed as:

$$\Delta i_{on} = \begin{cases} I_{ac}\sin(\vartheta-\varphi)\,(1-2\,m\,|\sin\vartheta|)\,, & m\,|\sin\vartheta| \le 0.5 \\ I_{ac}\sin(\vartheta-\varphi)\,(-1+2\,m\,|\sin\vartheta|)\,, & m\,|\sin\vartheta| \ge 0.5 \end{cases} \tag{11}$$

As an example, Figs. 4 and 5 show the instantaneous LDN input current and the low-frequency component (8) in case of two different modulation indexes (m = 0.5 and m = 1) and for two cases of load phase angles (φ = 0° and φ = 30°) considering unity output current (I_{ac} = 1A).

Similar calculations have been developed in [19] in order to calculate the input current components of the main H-bridge cell.

IV. Analysis of LDN Input Voltage

Basing on the LDN input current, the analysis can be developed also for the LDN input voltage. In particular, to ensure a proper design of the dc-link capacitor, the peak-to-peak values of the voltage ripple components are analytically determined. As for the LDN input current, the instantaneous dc-link voltage of the LDN can be written as

$$v = V + \tilde{v} + \Delta v \,, \tag{12}$$

being V the dc component, proved in Appendix B to be V_{dc}/2, $\tilde{v}$ the low-frequency component (corresponding to the averaged component over the switching period, apart the dc component), and Δv the switching frequency component.

A. Low-frequency (averaged) voltage component

The low-frequency dc-link voltage component can be analytically calculated by integrating the corresponding input current (8) as:

$$\tilde{v} = \frac{1}{\omega C}\int \tilde{i}\,d\vartheta + K \,, \tag{13}$$

where K is an integration constant. Introducing (8) in (13) and solving the integral, the input LDN voltage becomes:

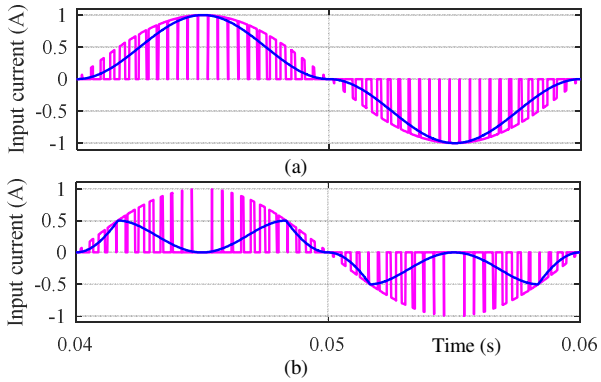

Fig. 4. Input LDN current and its averaged counterpart $\tilde{i}$ for (a) m = 0.5 and (b) m = 1, in case of load phase angle φ = 0° and I_{ac} = 1A.

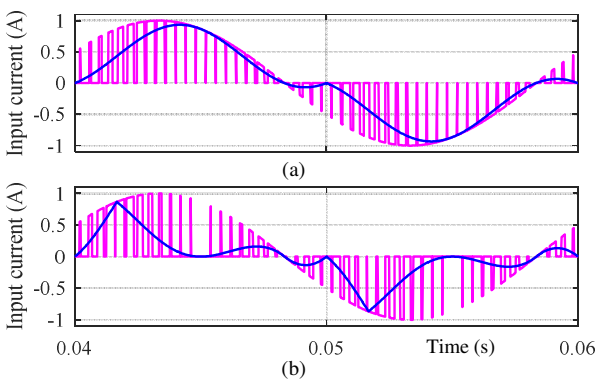

Fig. 5. Input LDN current and its averaged counterpart $\tilde{i}$ for (a) m = 0.5 and (b) m = 1, in case of load phase angle φ = 30° and I_{ac} = 1A.

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$$\tilde{v} = \frac{I_{ac}}{2fC}\tilde{u}\,, \tag{14}$$

being $\tilde{u}$ the normalized low-frequency component of the input LDN voltage given by

$$\tilde{u} = \begin{cases} \dfrac{m}{\pi}\left(\vartheta\cos\varphi - \dfrac{1}{2}\sin(2\vartheta-\varphi)\right) + K_1\,, & m\left|\sin\vartheta\right| \le 0.5 \\ -\dfrac{2}{\pi}\cos(\vartheta-\varphi) - \dfrac{m}{\pi}\left(\vartheta\cos\varphi - \dfrac{1}{2}\sin(2\vartheta-\varphi)\right) + K_2\,, & m\left|\sin\vartheta\right| \ge 0.5 \end{cases} \tag{15}$$

K_1 and K_2 are determined by exploiting the continuity of $\tilde{u}$ passing from the first to the second range, i.e., setting the same value of the two expressions of $\tilde{u}$ for $m|\sin\vartheta|=0.5$. The waveform of $\tilde{u}$ for different modulation indexes in case of $\varphi = 0°$ and $\varphi = 30°$ is depicted in Fig. 6 (a) and (b), respectively. It can be noticed that the maximum value is obtained in the case of unity power factor ($\varphi = 0°$) and it always falls in the middle of the fundamental period. As a consequence, the maximum peak-to-peak of the LDN low-frequency voltage ripple can be readily calculated by setting $\vartheta = \pi$ and $\varphi = 0°$ in (15), giving:

$$\tilde{u}_{pp} = \begin{cases} m\,, & m \le 0.5 \\ \dfrac{4}{\pi}m\arcsin\left(\frac{1}{2m}\right) - m + \dfrac{1}{m\pi}\sqrt{4m^2-1}\,, & m \ge 0.5 \end{cases} \tag{16}$$

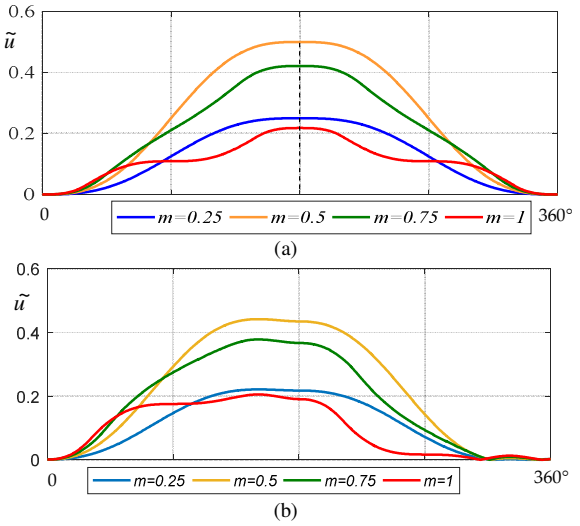

Fig. 6. Normalized low-frequency input LDN voltage in the fundamental period [0, 360°] for different m. Output phase angle (a) $\varphi = 0°$ and (b) $\varphi = 30°$.

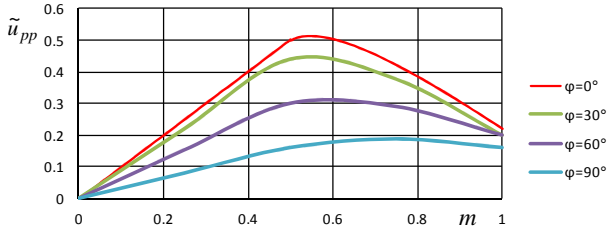

Fig. 7. Peak-to-peak value of the normalized low-frequency input LDN voltage vs. modulation index m and output phase angle $\varphi = 0°, 30°, 60°, 90°$.

Fig. 7 shows the maximum of the normalized peak-to-peak ripple amplitude for $\varphi = 0°$, 30°, 60°, and 90°. In case of $\varphi = 0°$, $\tilde{u}_{pp}$ was analytically determined by (16) (red trace), while for the other three cases it was done numerically.

The maximum amplitude of normalized peak-to-peak low-frequency voltage ripple is observed around $m \approx 0.55$ ($\varphi = 0°$), and it can be analytically calculated by (16) as:

$$\tilde{u}_{pp}^{\max} = 0.514\,. \tag{17}$$

Finally, combining (14) and (17), the maximum amplitude of the low-frequency peak-to-peak voltage ripple can be written as a simple function of output current amplitude and LDN capacitance as:

$$\tilde{v}_{pp}^{\max} = 0.514\frac{I_{ac}}{2fC}\,. \tag{18}$$

B. Switching frequency voltage component

Considering sinusoidal PWM, the "on-time" interval Δt_{on} for the LDN cell is calculated on the basis of (1) and (2) as

$$\Delta t_{on} = \begin{cases} 2m\left|\sin\vartheta\right|T_{sw}\,, & m\left|\sin\vartheta\right| \le 0.5 \\ 2\left(1-m\left|\sin\vartheta\right|\right)T_{sw}\,, & m\left|\sin\vartheta\right| \ge 0.5. \end{cases} \tag{19}$$

The corresponding peak-to-peak dc voltage variation over the sub-period $[0, \Delta t_{on}]$ can be expressed as

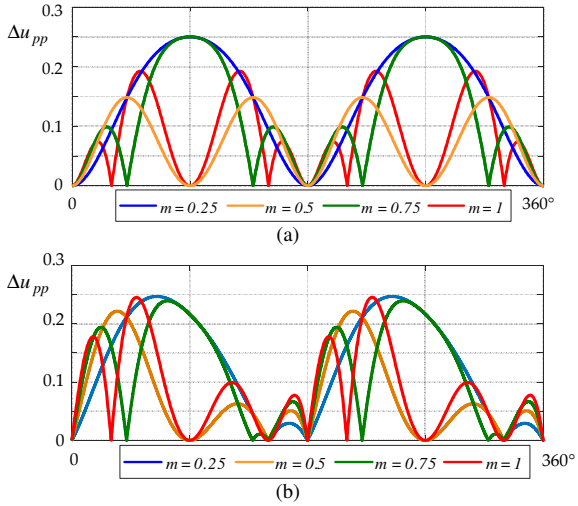

Fig. 8. Normalized peak-to-peak switching ripple amplitude of input LDN voltage in fundamental period [0, 360°] for different m. Output phase angle (a) $\varphi = 0°$ and (b) $\varphi = 30°$.

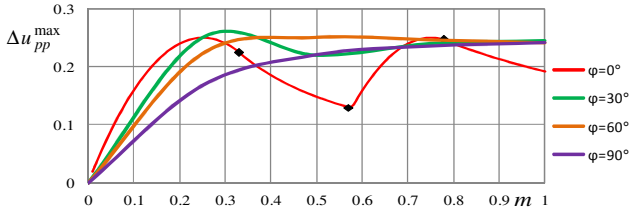

Fig. 9. Max. of normalized peak-to-peak switching ripple of input LDN voltage (obtained by joining the four ranges) vs. modulation index m and output phase angle $\varphi = 0°, 30°, 60°$ and 90°.

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$$\Delta v_{pp} = \frac{1}{C}\int_0^{\Delta t_{on}} \Delta i_{on}\, dt \approx \frac{1}{C}\Delta i_{on}\,\Delta t_{on}. \tag{20}$$

By introducing in (20) the on-time interval Δt_{on} given by (19) and the corresponding current Δi_{on} given by (11), the peak-to-peak switching ripple amplitude of the LDN input voltage becomes:

$$\Delta v_{pp} = \frac{I_{ac}}{f_{sw} C}\,\Delta u_{pp}, \tag{21}$$

being Δu_{pp} its normalized value given by

$$\begin{cases} \Delta u_{pp} = 2m\left|\sin(\vartheta-\varphi)\right|\left|\sin\vartheta\right|\left(1-2m\left|\sin\vartheta\right|\right), & m\left|\sin\vartheta\right| \le 0.5 \\ \Delta u_{pp} = 2\left|\sin(\vartheta-\varphi)\right|\left(2m\left|\sin\vartheta\right|-1\right)\left(1-m\left|\sin\vartheta\right|\right), & m\left|\sin\vartheta\right| \ge 0.5 \end{cases} \tag{22}$$

Fig. 8 shows the distribution of the normalized peak-to-peak ripple amplitude given by (22) over the fundamental period. Four cases of modulation index m = 0.25, 0.5, 0.75, and 1, and two cases of output phase angle $\varphi = 0°$ (Fig. 8 (a)) and $\varphi = 30°$ (Fig. 8 (b)), have been considered.

In order to estimate the maximum voltage switching ripple amplitude in the fundamental period, the following expressions are analytically calculated from (22) in the case of zero phase angle ($\varphi = 0°$):

$$\Delta u_{pp}^{\max} = \begin{cases} 2m(1-2m), & 0 \le m \le \dfrac{1}{3} \\ \dfrac{2}{27m}, & \dfrac{1}{3} \le m \le 0.575 \\ 2(2m-1)(1-m), & 0.575 \le m \le \dfrac{3+\sqrt{3}}{6} \\ \dfrac{\sqrt{3}}{9m}, & \dfrac{3+\sqrt{3}}{6} \le m \le 1. \end{cases} \tag{23}$$

The maximum of normalized peak-to-peak voltage ripple as a function of m is depicted in Fig. 9. It can be noted that the range is between 0 (m = 0) and 1/4 (m = 1/4 and 3/4). Replacing $\Delta u_{pp}^{\max} = 1/4$ in (21), the absolute maximum becomes:

$$\Delta v_{pp}^{\max} = 0.25\frac{I_{ac}}{f_{sw} C}. \tag{24}$$

The analysis has been numerically extended to other phase angles (φ = 30°, 60°, and 90°) as shown in Fig. 9, obtaining a slightly higher value for global maximum of the normalized peak-to-peak voltage ripple, i.e., 0.261 instead of 0.25.

It is important to mention that all the previous calculations developed for the LDN cell can be similarly extended to the analysis of the input voltage ripple of the H-Bridge cell in case of non-negligible dc source impedance [19], considering the "ad hoc" modified modulating signal defined in (4).

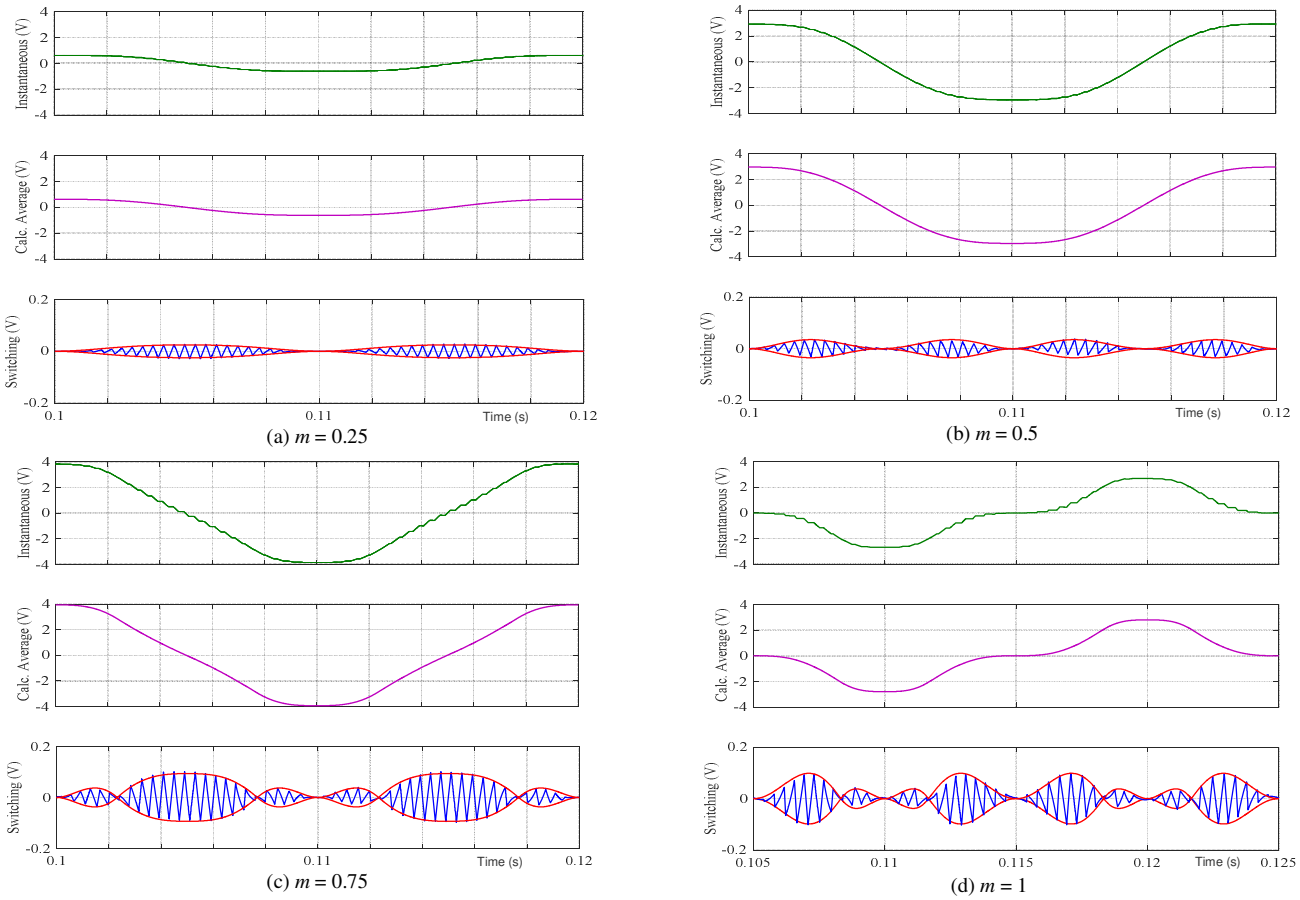

Fig. 10. Simulation results: Alternating LDN input voltage (green, top diagrams), theoretical (calculated) low-frequency (violet, middle diagrams), and switching ripple components with theoretical envelopes (blue and red traces, respectively, bottom diagrams) for different modulation indexes and $\varphi = 0°$.

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V. GUIDELINES FOR DESIGNING THE LDN CAPACITOR

The results obtained for calculating both the switching frequency and the low-frequency input voltage ripples can be readily adopted for designing the LDN capacitor.

In particular, is supposed a restriction in the maximum voltage switching ripple amplitude, $\Delta v_{pp}^{\max} = \Delta v_{pp}^{*}$, such as for reducing switching noise, conducted EMI, measurements inaccuracy, etc. The resulting minimum value of dc-link capacitance C can be calculated according to (24) and Fig. 9 as:

$$C \geq 0.261 \frac{I_{ac}}{f_{sw} \Delta v_{pp}^{*}} . \quad (25)$$

Note that a relation similar to (25) has been obtained in [12] in the case of flying capacitor asymmetric H-bridge.

Instead, if the target is to limit the low-frequency voltage oscillation amplitudes (low-order harmonics), $\tilde{v}_{pp}^{*}$, the dc-link capacitance can be calculated according to (18), leading to:

$$C \geq 0.257 \frac{I_{ac}}{f \tilde{v}_{pp}^{*}} . \quad (26)$$

Note that (25) and (26) have almost the same coefficients considering low and switching frequency ripple components.

VI. SIMULATION AND EXPERIMENTAL RESULTS

To verify the analytical developments proposed in previous sections, simulations and corresponding experimental tests are carried out for single-phase multilevel H-bridge inverter based on level doubling network, according to Fig. 1 (a).

A. Simulation Results

Circuit simulations of the considered multilevel inverter are performed by Matlab/Simulink. Simulation parameters are: dc (ideal) H-bridge supply: V_{dc} = 100V, LDN capacitance: C = 1.1 mF, switching frequency: f_{sw} = 2.5 kHz.

In order to verify the precise matching with the proposed analytical developments, the inverter output is connected to a RLC circuit with unity power factor, according to the parameters given in Table I (same as for the experimental setup).

Fig. 10 presents the alternating LDN input voltage (top diagram), the theoretical low-frequency component $\tilde{v}$ calculated by (14) and (15), corresponding to its value averaged over the switching period (middle diagram), and the switching ripple component together with its theoretical envelopes $\pm\Delta v_{pp}/2$ evaluated by (21) and (22) (bottom diagram). Different modulation indexes have been considered to cover the whole modulation range, i.e. m = 0.25, 0.5, 0.75, and 1. A perfect matching is observed for all the presented cases.

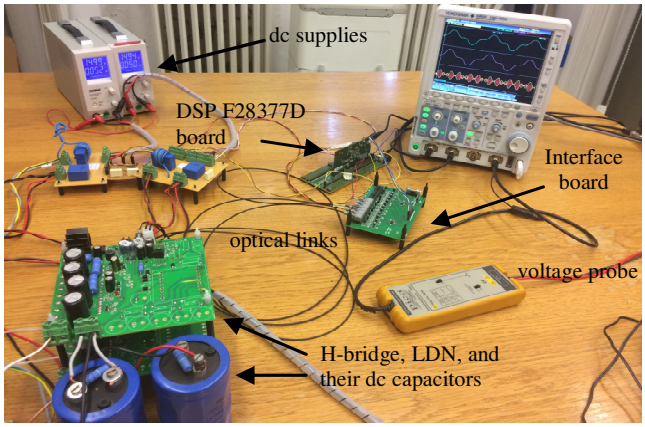
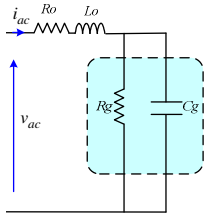


Fig. 11. View of the experimental setup.

TABLE I
SIMULATION AND EXPERIMENTAL SETUP PARAMETERS

V_{dc}	H-bridge dc source voltage (C_{dc}=1.1 mF)	100 V
C	LDN capacitor	1.1 mF
f, f_{sw}	Fundamental and switching frequencies	50 Hz, 2.5 kHz
R_o, L_o	Output series impedance	6.5 Ω, 34 mH
R_g, C_g	Equivalent grid (parallel impedance)	30 Ω, 44 µF



B. Experimental Results

Theoretical and simulation results have been experimentally verified by the setup shown in Fig. 11. It includes a DSP board (TMS320F28377D) programmed by Code Composer Studio (CCS), also employed to change online all the modulation parameters. The single-phase H-bridge inverter with level doubling network of Fig. 1 (a) has been implemented by two power IGBT modules IPM PS22A76 (1200 V, 25 A), driven by the DSP board via intermediate optical links. A TDK-Lambda GEN100-15 dc source has been used to supply the H-bridge, with an additional parallel dc-link capacitance of 1.1

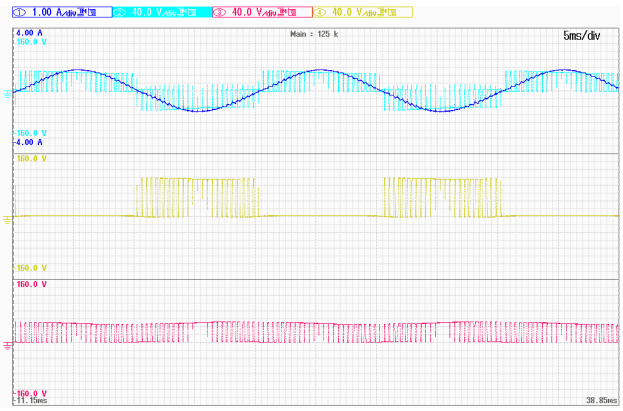


Fig. 12. Inverter output variables for m = 0.5. Top trace: total voltage and current. Middle trace: H-bridge voltage. Bottom: LDN voltage.

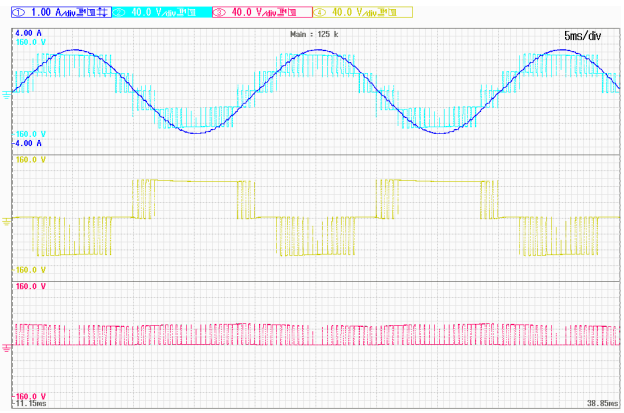


Fig. 13. Inverter output variables for m = 1. Top trace: total voltage and current. Middle trace: H-bridge voltage. Bottom: LDN voltage.

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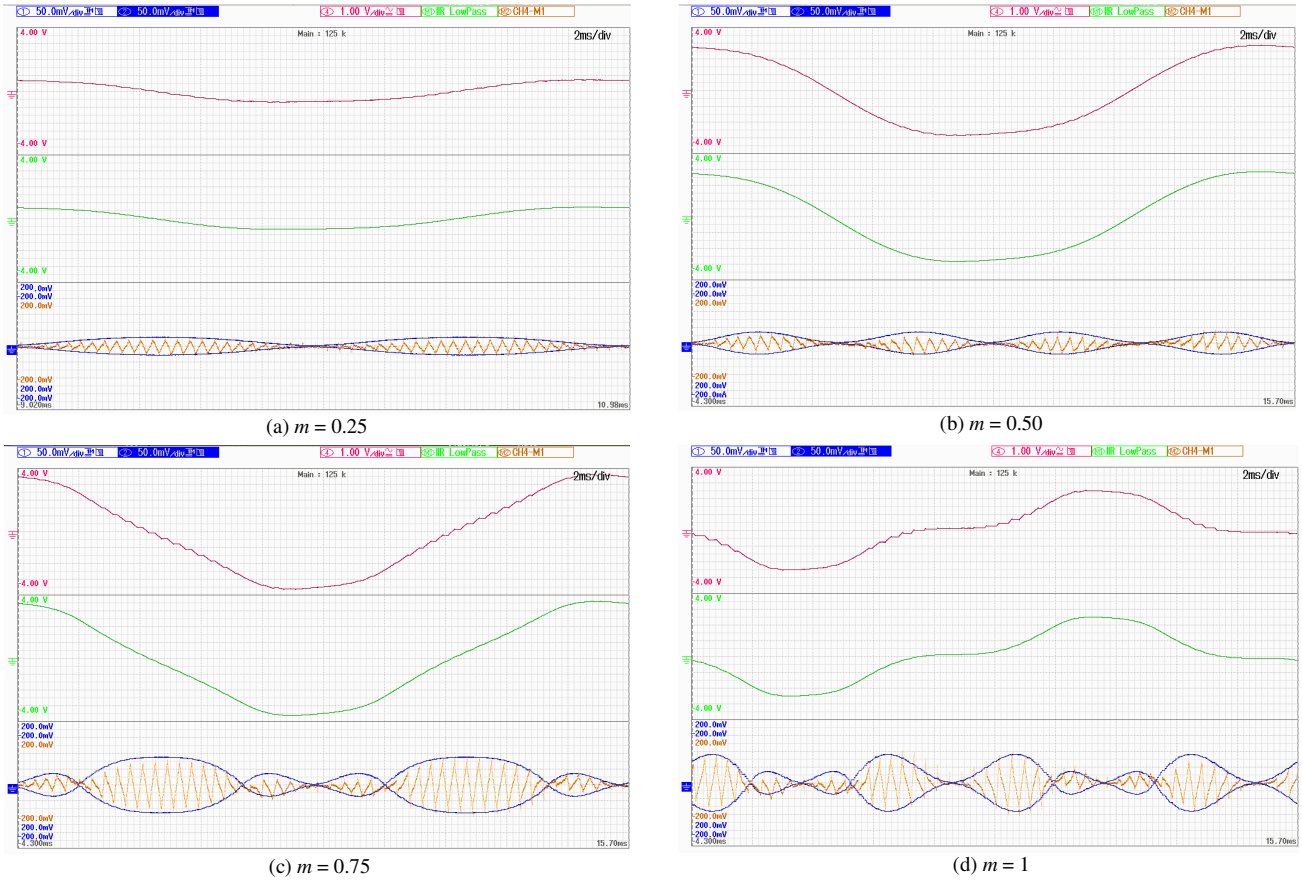

(a) $m = 0.25$ (b) $m = 0.50$

(c) $m = 0.75$ (d) $m = 1$

Fig. 14. Experimental results for different modulation indexes. Top traces: alternating LDN input voltage. Middle traces: low-frequency component (filtered by oscilloscope functions). Bottom traces: switching frequency component and corresponding theoretical envelopes. Reference is made to Fig. 10.

mF (the same size used for the LDN cell). The inverter output is connected to an RLC circuit with unity power factor, emulating the grid connection trough an ac-link inductor. The main setup parameters are given in Table I (as in simulations).

Experimental results are shown by oscilloscope screenshots, elaborating and emphasizing the signals of interests.

Figs. 12 and 13 show the output variables in case of $m = 0.5$ and $m = 1$, corresponding to Figs. 2 and 3, respectively. In particular, the top traces represent the total output voltage and current (almost sinusoidal current with unity power factor can be noted), the middle trace represents the individual output voltage of the H-bridge cell, and the bottom trace represents the individual output voltage of the LDN cell.

The input LDN voltage with its components are shown in Fig. 14 over one fundamental period ($T = 20$ ms) for different modulation indexes ($m = 0.25$, 0.5, 0.75, and 1), corresponding to the simulation results given in Fig. 10.

In particular, for each screenshot, the top trace represents the alternating LDN voltage, and the middle trace represents the low-frequency component obtained by the built-in low-pass filter function of the oscilloscope. The bottom traces represent the switching ripple component together with the peak-to-peak envelopes $\pm\Delta v_{pp}/2$ calculated by (21) and (22) on the DSP board and sent to an output DAC channel with a proper voltage scaling.

TABLE II
MAX PEAK-TO-PEAK DC-LINK VOLTAGE RIPPLE OF THE LDN CELL

m	Switching frequency component			Low-frequency component		
	Th. [V]	*Sim.* [V]	*Exp.* [V]	*Th.* [V]	*Sim.* [V]	*Exp.* [V]
0.25	0.05	0.06	0.06	1.22	1.2	1.2
0.50	0.07	0.08	0.08	5.77	5.7	5.6
0.75	0.18	0.20	0.20	7.63	7.6	7.4
1.00	0.19	0.20	0.20	5.25	5.2	5.0

C. Discussion

The alternating LDN input voltage in both simulation and experimental results has been calculated by filtering from the instantaneous voltage its dc component, i.e. $V_{dc}/2 \approx 50$V. In the case of experimental results, the "ac coupling" built-in function of the oscilloscope has been used for a fast and effective dc offset compensation, introducing a slight and acceptable distortion in the order of a few percent.

Simulation and experimental results have a good matching for all the considered cases, as proved by the comparison of Fig. 10 and Fig. 14. Note that the same scale is adopted in corresponding simulations and experimental diagrams in order to facilitate the comparison.

The results in terms of peak-to-peak LDN input voltage ripple are summarized in Table II for the four considered modulation indexes in case of theory (*Th.*), simulations (*Sim.*), and experiments (*Exp.*). For all the considered cases the matching is within the expected resolution of a few percent.

VII. Conclusion

The modulation principle and analysis of input current and voltage ripple in multilevel inverters made by cascading H-bridge and LDN cells are presented in this paper. In particular, a carrier-based modulation principle has been defined for single-phase configuration, guaranteeing proper multilevel waveforms (switch synchronization) and self-balancing capability.

Both the low-frequency and the switching frequency input current and voltage ripple components have been analytically determined for the LDN cell, with a procedure easy extendable to the H-bridge cell. In particular, the peak-to-peak voltage ripple amplitudes have been calculated as a function of the modulation index. Simple and effective guidelines to design the dc-link capacitor of the LDN cell have been also proposed.

Developments have been carried out in case of unity power factor, representing most of the grid-connected applications, and extended to a general output phase angle. Both simulation and experimental results have been presented, proving the feasibility of the proposed modulation and the effectiveness of the analytical developments.

Appendix A
Output Voltage and Current Harmonics

The normalized LDN output voltage averaged over the switching period, i.e. the LDN modulating signal (2) corresponding to the low-frequency components, can be written in terms of harmonics as:

$$\bar{u}_{ac}^{L} = U_0 + \sum_{k=2}^{\infty} \bar{u}_k^{L} = U_0 + \sum_{k=2}^{\infty} U_k \cos(k\vartheta), \qquad (27)$$

where U_0 is the average component and U_k is the amplitude of the k^{th} harmonic component, being k an even number (due to the symmetry). The amplitude (including the sign) of these components can be calculated on the basis of (2), leading to:

$$U_0 = \begin{cases} \dfrac{2}{\pi} m & \text{for } m \le 0.5 \\ \dfrac{2}{\pi}\left[m + \dfrac{\pi}{2} - \alpha_m - \sqrt{4m^2 - 1} \right] & \text{for } m \ge 0.5 \end{cases}, \qquad (28)$$

$$U_k = \begin{cases} -\dfrac{4}{\pi} \dfrac{m}{(k^2 - 1)} & \text{for } m \le 0.5 \\ \dfrac{4}{\pi}\left[A_k + B_k \right] & \text{for } m \ge 0.5 \end{cases}, \quad k \text{ even}. \qquad (29)$$

The coefficients A_k and B_k in (29) are calculated as:

$$A_k = \int_0^{\alpha_m} m \sin\vartheta \cos(k\vartheta)\, d\vartheta, \quad B_k = \int_{\alpha_m}^{\pi/2} (1 - m\sin\vartheta)\cos(k\vartheta)\, d\vartheta \qquad (30)$$

$$A_k = \frac{1}{2k^2 - 2}\left[k\sin(k\alpha_m) + \sqrt{4m^2 - 1}\cos(k\alpha_m) - 2m \right] \qquad (31)$$

$$B_k = -\frac{1}{k}\sin(k\alpha_m) + \frac{1}{2k^2 - 2}\left[k\sin(k\alpha_m) + \sqrt{4m^2 - 1}\cos(k\alpha_m) \right], \qquad (32)$$

being $\alpha_m = \arcsin(1/2m)$.

Regarding the input LDN current, it can be expressed by the input-output power balance (6), introducing the output voltage (27) and the output current (7), leading to:

$$\tilde{i} = -I_{ac}\{U_2 \sin(\vartheta + \varphi) - 2U_0 \sin(\vartheta - \varphi) + \sum_{n=3}^{\infty}\left[U_{n+1}\sin(n\vartheta + \varphi) - U_{n-1}\sin(n\vartheta - \varphi) \right]\} \qquad (33)$$

From (33) the amplitudes of the low-frequency input LDN current harmonic components in case of general power angle φ are:

$$\begin{cases} I_0 = I_2 = 0, & n \ge 3 \text{ odd integer} \\ I_1 = I_{ac}\sqrt{(\cos\varphi)^2 (U_2 - 2U_0)^2 + (\sin\varphi)^2 (U_2 + 2U_0)^2} \\ I_n = I_{ac}\sqrt{(\cos\varphi)^2 (U_{n+1} - U_{n-1})^2 + (\sin\varphi)^2 (U_{n+1} + U_{n-1})^2} \end{cases} \qquad (34)$$

In particular, the low-frequency input LDN current harmonic components in case of unity power factor (φ = 0°) are:

$$\begin{cases} I_0 = I_2 = 0 \\ I_1 = I_{ac}\left[U_2 - 2U_0 \right] \\ I_n = I_{ac}\left[U_{n+1} - U_{n-1} \right] \end{cases} \quad n \ge 3 \text{ odd integer}. \qquad (35)$$

Appendix B
Self-Balancing Principle of LDN Cell

According to the modulation principle introduced in Section II, in case of sinusoidal output current, the steady-state LDN voltage is $V = V_{dc}/2$, that is also called "balanced voltage". The self-balancing principle for LDN has been briefly introduced in [5], and it is analytically proved here on the basis of the proposed LDN modulation principle.

With reference to a generic LDN input voltage V, the LDN output voltage can be expressed by considering (1) and (2) as:

$$\bar{v}_{ac}^{L} = \begin{cases} 2Vm|\sin\vartheta|, & m|\sin\vartheta| \le 0.5 \\ 2V(1 - m|\sin\vartheta|), & m|\sin\vartheta| \ge 0.5 \end{cases} \qquad (36)$$

The self-balancing principle is based on unmodified H-bridge modulating signal, even in presence of LDN voltage unbalance. The H-bridge output voltage is expressed by (4) on the basis of the H-bridge input voltage V_{dc} as:

$$\bar{v}_{ac}^{H} = \begin{cases} V_{dc}(m\sin\vartheta - m|\sin\vartheta|), & m|\sin\vartheta| \le 0.5 \\ V_{dc}(m\sin\vartheta - 1 + m|\sin\vartheta|), & m|\sin\vartheta| \ge 0.5 \end{cases} \qquad (37)$$

As a result of (36) and (37), the total output voltage becomes:

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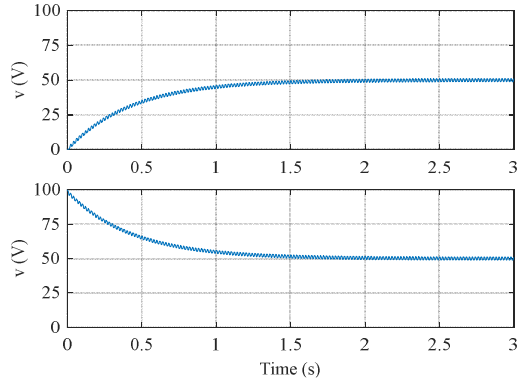

Fig. 15. Example of LDN dc-link capacitor voltage balancing transient with different initial conditions (0 and V_{dc} = 100V) for m = 1 and φ = 30°.

$$\bar{v}_{ac} = \bar{v}_{ac}^{H} + \bar{v}_{ac}^{L} = V_{dc}\, m \sin\vartheta + \left(2V - V_{dc}\right)\bar{u}_{ac}^{L}. \tag{38}$$

Equation (38) shows that, in case of LDN voltage unbalance, i.e. $V \neq V_{dc}/2$, an offset (average) voltage that is a fraction of the LDN output voltage is added to the reference (sinusoidal) output voltage, with a sign and an amplitude depending on the voltage unbalance itself. The average output voltage $V_{ac,0}$ is calculated by (38) and (28) as:

$$V_{ac,0} = \left(2V - V_{dc}\right)U_0. \tag{39}$$

The average output voltage (39) produces a corresponding average output current, in addition to the sinusoidal component, generating a corresponding average of the input LDN current, with a sign balancing the LDN voltage unbalance.

Examples of LDN dc-link voltage balancing transients considering the initial voltages 0 and V_{dc} are shown in Fig. 15. It can be noted that in both cases the dc-link voltage v spontaneously goes to the half of the dc voltage source ($v \approx V_{dc}/2$) from both initial conditions, proving the self-balancing capability of the considered LDN modulation.

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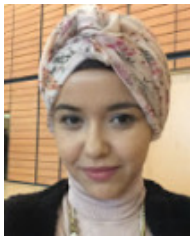

Dr. Manel Hammami is currently a Postdoctoral Fellow at the Dept. of Electrical, Electronic and Information Engineering, "Guglielmo Marconi" – DEI, University of Bologna, Italy. She received the Bachelor (2010) and Master degree (2012), both in Electrical Engineering, from University of Tunis, Tunisia. She received the PhD degree in Electronics, Telecommunications and Information Technologies Engineering from University of Bologna in 2018.

Dr. Hammami authored a several number of papers published in high-ranking Journals or presented at IEEE conferences; she is an appreciated reviewer for three reputed international journals (IEEE Trans. on Industrial Electronics, IET Power Electronics, MDPI Energies and MDPI Electronics).

Her research interests include photovoltaic generation systems, multilevel converters and charging systems for electric vehicles.

Gabriele Grandi (M'00–SM'13) received the M.Sc. (cum laude) and Ph.D. degrees in electrical engineering from the University of Bologna, Bologna, Italy, in 1990 and 1994, respectively.

He has been with the Department of Electrical, Electronic, and Information Engineering, University of Bologna, as Research Associate (since 1995), Associate Professor (since 2005), and actually as Full professor (since 2016), in electrical engineering.

He is the Head of the SolarTronic-Lab at University of Bologna. He has authored or co-authored more than 160 papers in conference proceedings and international journals, mainly with the IEEE. His main research interests include power electronic circuits, multiphase and multilevel converters, photovoltaics, and circuit modeling. Dr. Grandi actually serves as Editor-at-Large for IET Power Electronics, Academic Editor for MDPI Energies, MDPI Electronics, and Associate Editor for IEEE Trans. on Industrial Electronics.