

## Article

# Modeling Stray Capacitances of High-Voltage Capacitive Dividers for Conventional Measurement Setups

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**Abstract:** Stray capacitances (SCs) are a serious issue in high-voltage (HV) applications. Their presence can alter the circuit or the operation of a device, resulting in wrong or even disastrous consequences. To this purpose, in this work, we describe the modeling of SCs in HV capacitive dividers. Such modeling does not rely on finite element analysis or complicated geometries; instead, it starts from an equivalent circuit of a conventional measurement setup described by the standard IEC 61869-11. Once the equivalent model including the SCs is found, closed expressions of the SCs are derived starting from the ratio error definition. Afterwards, they are validated in a simulation environment by implementing various circuit configurations. The results demonstrate the expressions applicability and effectiveness; hence, thanks to their simplicity, they can be implemented by system operators, researchers, and manufacturers avoiding the use of complicated methods and technologies.

**Keywords:** stray capacitance; high voltage; capacitive divider; modeling; voltage divider; capacitor; expressions



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## 1. Introduction

The power network has undergone a significant revolution in the last few decades, due to the spread of distributed energy resources (DER) (e.g., almost 35% of the total amount of production in Italy [1]) by intelligent electronic devices (IED), such as energy meters, phasor measurement units (PMUs), etc., and most recently, the introduction of electric vehicles (EVs), with their sales increasing daily. These changes have forced utilities and distribution system operators (DSOs) to rethink ways to manage and control the grid, for all the considered voltage levels, i.e., low, medium, and high (LV, MV, and HV, respectively), to avoid serious complications due to the presence of such new actors within the grid.

In this scenario, instrument transformers (ITs) play a significant role [2–4]. In fact, despite the aforementioned changes and modifications of the grid, they must continue, in a reliable way, to operate, scaling voltages (voltage transformers, VTs) and currents (current transformers, CTs) in order to be suitable for the typical acquisition systems, and then to be evaluated by the operators.

ITs rely upon a solid backbone of standards, the IEC 61869 series, comprised of fifteen documents which cover all kind of transformers and their different features and capabilities. For example, Standards IEC 61869-1 and -6 deal with general requirements [5,6] that apply to conventional ITs and low-power ITs (LPITs), respectively; Standards IEC 61869-2 to -5 describe inductive instrument transformers; regarding the new generation of electronic devices, they are standardized in Standards IEC 61869-7 to -15 (including direct current (DC) devices and merging units) [7,8].

In addition to the standards for ITs, there is also extensive related literature with available documents that try to address most of the issues that may affect their correct operation. For example, in [9–13], the effects of temperature on ITs are described; in [14–20],

several modeling methods and procedures are presented, for both CTs and VTs (in both time and frequency domain); finally, [21–26] discuss specifically the ITs uncertainty under rated or off-nominal conditions of the grid.

From the literature, emerges the fact that electrical and environmental quantities can affect ITs and their accuracy (of course, within the grid, not only are ITs affected by those quantities, but also other assets, such as electric motors [27–29] and accessories [30–34]).

Therefore, accuracy must be treated as a fundamental aspect to deal with whenever applications of ITs are considered; and therefore, in this paper, we focus on an evaluation of how the accuracy of ITs is influenced by some stray parameters. Specifically, in this paper, HV capacitive dividers (CDs) are considered; in particular, stray capacitances between points at different voltages are analyzed and modeled.

It is well-known that measuring high voltage is always a critical task as compared with MV and LV, due to the issues associated the high voltage. Among all the potential ways of measuring HV, CDs are frequently adopted to reduce HV, and therefore are one of the most studied [35–39] (see further details below).

As previously mentioned, stray capacitances are a critical issue related to working with HV and CDs. In fact, they originate and increase as the voltage difference between two points of the circuit increases, introducing new paths for the current, and then modifying the expected operation of the equipment.

Stray capacitances (SCs) have been previously studied in several works. For example, formulae for the capacitances based on the geometries studied are described in [40]. In [41–44], stray capacitances were modeled for resistive, capacitive–resistive, and capacitive dividers, respectively. In those works, considering the complexity of the capacitance computation, even for simple geometries, the authors treated the stray capacitance identification with finite element methods, or assumed simple geometries as known. However, those approaches are not always possible or available.

In contrast, we aim at simplifying this assessment process, differentiating its content from what can be found in the literature, by avoiding the use of complicated techniques and the need for preliminary knowledge of the equipment and location geometries to deal with. In fact, for this work, we start from a conventional in-field configuration of capacitive dividers, the three-phase configuration of devices, to identify an equivalent circuit of the capacitive dividers which includes the stray capacitances. Afterwards, SCs are estimated starting from accuracy measurements performed on actual CDs and by manipulating the test conditions to extrapolate more information.

The result of our research is a set of closed expressions to find the stray capacitances of the considered circuit, starting from the knowledge of the rated capacitance (visible on the nameplate of the device) of the divider and from the ratio error information (obtained from real in-field or in-laboratory measurements). Then, the obtained expressions could be adopted by manufacturers or researchers to improve the design of CDs for better fulfilling the accuracy test requirements fixed by the standards. In particular, users of CDs may build their own equivalent circuit which includes the SCs that are influencing a CD's behavior.

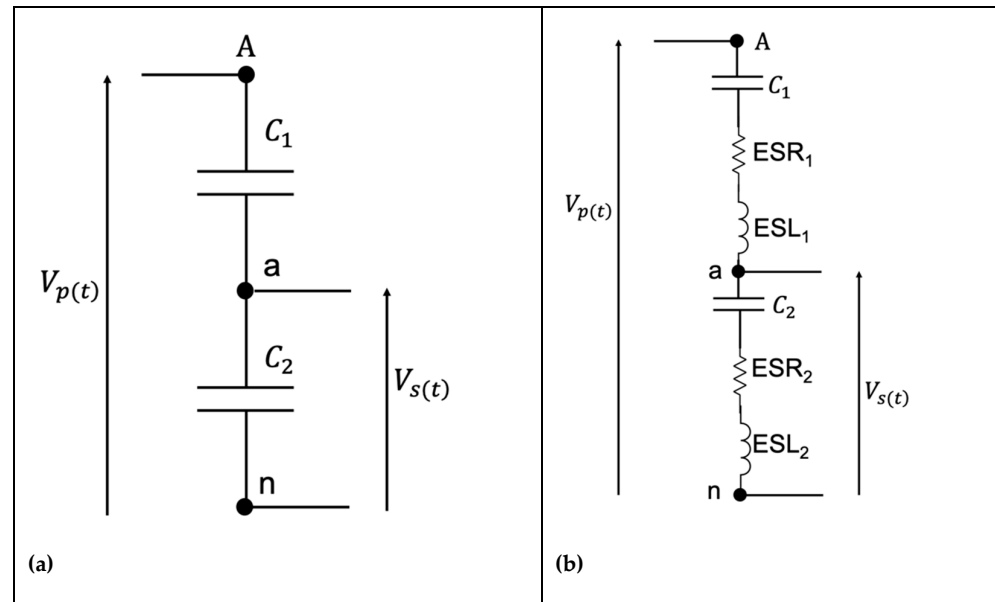
The paper is structured as follows: In Section 2, we provide an overview of the basic principles of a capacitive divider; in Section 3, we describe the modeling of the stray capacitances, in which the considered circuit is presented along with all the steps that lead to the final expressions; in Section 4, we validate and discuss the obtained results by means of a simulation environment; and in Section 5, we provide conclusions and some comments are summarized.

## 2. Capacitive Dividers

### 2.1. Basic Principles

A CD is a device that uses capacitors (instead of resistors, for example) to reduce a high voltage according to the selected number and values of the capacitors. In detail, the greater amount of voltage drops on the smallest capacitor of the divider (opposite working principle than resistors).

The ideal equivalent circuit is depicted in Figure 1a, where the primary and secondary capacitors can be distinguished ( $C_1$  and  $C_2$ , respectively). Furthermore, the diagram also shows the primary high-voltage terminal “A” (hence the HV to be reduced), the secondary low voltage terminal “a” (the reduced voltage), and “n” the common ground or reference terminal.



**Figure 1.** (a) The ideal equivalent circuit of a capacitive divider; (b) The real equivalent circuit of a capacitive divider.

From Figure 1a it is also possible to write the input/output relation of the ideal divider as follows:

$$V_{s(t)} = V_{p(t)} \frac{C_1}{C_1 + C_2}, \quad (1)$$

where  $V_{s(t)}$  is the time-dependent output voltage and  $V_{p(t)}$  is the time-dependent primary voltage, to be reduced by the divider. The interesting fact from Equation (1) is that even if the capacitor is a frequency dependent component the frequency does not appear. This is due to the fact that the capacitive divider components are all equally affected by frequency, hence, the frequency dependence of the output voltage disappears.

From Equation (1), it is possible to compute the transformation ratio of the divider  $k$  (hence the ideal, or expected) as follows:

$$k = \frac{C_1 + C_2}{C_1}. \quad (2)$$

Therefore, from Equation (2), it is clear that the higher the secondary capacitor the higher the  $k$  of the overall divider.

Turning to the real CD, note that its equivalent circuit is shown in Figure 1b. Of course, one can complicate the real circuit as much as desired, but the depicted one has been selected due to its typical usage when the real description of the CD is considered. What differs from the ideal circuit is the presence of the equivalent series resistor ESR and the equivalent series inductor ESL for both primary and secondary sides ( $ESR_1$  and  $ESL_1$  for the primary and  $ESR_2$  and  $ESL_2$  for the secondary, respectively).

The presence of the ESR describes the non-ideality of the capacitor that also consists of conductors or metallic parts that dissipate heat. The presence of the ESL, instead, describes the non-ideality of the capacitor that leads to an autoresonance between the capacitance value of the capacitor and ESL. This resonance value must be selected far from the operating frequency of the considered application.

In light of the non-idealities, Equation (1) becomes the following:

$$V_{s(t)} = V_{p(t)} \frac{Z_2}{Z_1 + Z_2}, \quad (3)$$

where  $Z_1$  and  $Z_2$  are the complex impedances of the primary and secondary side of the circuit, respectively, which include the contributions of the ESR and ESL.

## 2.2. Pros and Cons

The CD technology is commonly implemented from the LV to the HV due to its advantages with respect to other technologies. Compared to the resistive divider, for example, the CD does not dissipate as much heat, hence, the current circulating through a CD is not a limiting factor. Of course, if the real circuit of the CD is considered, an equivalent resistor is to be considered; however, its contribution to the heat dissipation is negligible as compared with a resistive divider.

Furthermore, CDs can be classified in terms of their loss tangent (or  $\tan\delta$ ), which is the ratio between the resistive and the reactive part of a capacitor, which quantifies the “goodness” or the efficiency of the capacitor itself.

Another advantage of a CD is its linearity vs. frequency. In fact, as introduced above, even if the reactance  $X_c = 1/2\pi fC$  is dependent on the frequency  $f$ , the ratio of the divider, hence the output of a CD, is not frequency dependent.

On the contrary, among the disadvantages, CDs cannot be implemented into DC applications due to the capacitor nature of blocking DC components. Finally, it should be emphasized that CDs match the above description and advantages as much as they show an ideal behavior; hence, not influenced from the parasitic parameters.

## 3. Modeling Stray Capacitances

After the brief description of the CDs presented in Section 2, this section contains the core of the work. In detail, after introducing stray capacitances in Section 3.1, in Section 3.2, we describe the considered equivalent circuit. Then, in Section 3.3, we perform a simple circuit analysis to obtain useful information that is used, as described in Section 3.4, to derive the SCs expressions.

### 3.1. Stray Capacitances

A stray capacitance is an issue that manifests between two points subjected to different potentials, due to the fact that the electric field lines, starting from one point, close themselves to the surrounding points with different potentials. As a matter of fact, this issue is more significant in HV applications such as HV AC measurements (but, of course, SCs affect a wide variety of fields, from telecommunications to microelectronics, etc., even if they are not HV applications).

However, the identification of SCs is a very difficult task for several reasons including the following: (i) SCs are very small capacitances which, due to noise signals and other disturbances, are very difficult to measure and even detect; (ii) even if the approach is numerical, the geometries of the application is not always known, hence, the estimation of a SC is often not 100% correct.

The results of such difficulties impact on the knowledge of the equivalent circuit. In the specific case of a HV divider, it influences the value of the transformation ratio, hence, all the accuracy indexes computed starting from the ratio of the device. In fact, the actual transformation ratio is affected by temperature, humidity, non-idealities, etc., and also the SCs, which modify the equivalent circuit to be considered. In other HV applications, including motors and transformers [45], SCs play a fundamental role in the frequency behavior estimation of such machines.

Therefore, it is important to find simple and sufficiently accurate ways of estimating SCs to fully understand the behavior of electric assets when operating at rated or faulty

conditions and, in the case of HV capacitive dividers, how well they measure, hence what is their associated uncertainty.

In [46], for example, the authors evaluated the uncertainty with methods A and B (from the guide of the expression of uncertainty [47]) of a CD but without including stray capacitances.

### 3.2. Considered Model

In this work, the SC modeling is based on a measurement setup defined in the IEC standard [8] to evaluate the immunity of CDs. Such a setup is schematized in Figure 2 and it consists of the following: (i) a grounded wall indicated with “W”; (ii) the HV divider under test indicated with “DUT” and another identical HV divider used as a dummy divider for the tests, indicated as “DD”.

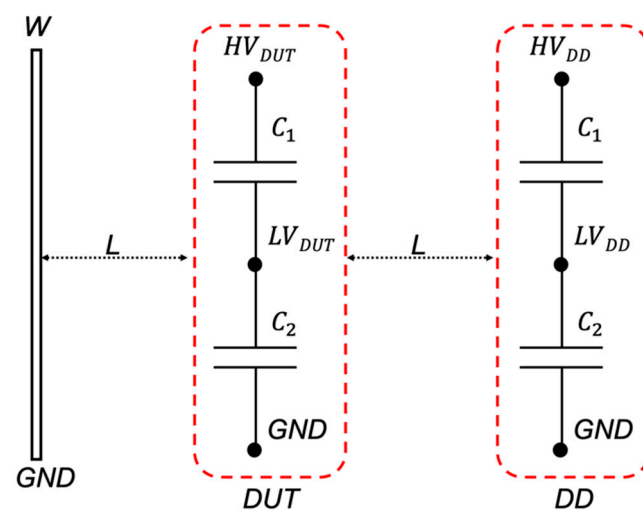


Figure 2. The measurement setup defined in Standard IEC 61869-11 [8].

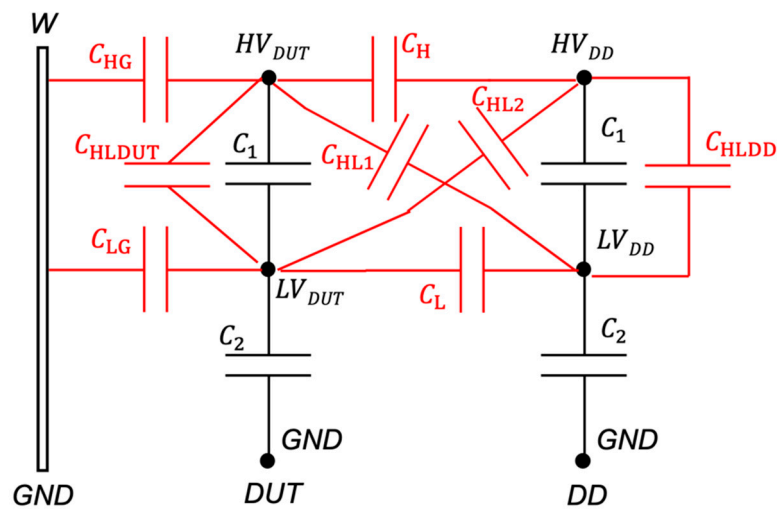
In Figure 2, the following can be observed: (i) the fixed distance “L” between the wall and the dividers; (ii) the points where the HV is applied  $HV_{DUT}$  and  $HV_{DD}$  for the device under test and the dummy one, respectively; and (iii) the LV secondary outputs  $LV_{DUT}$  and  $LV_{DD}$ . It is important to emphasize that the distance L has been defined by the standard as the distance between two devices operating at the highest rms value of phase-to-phase voltage for which the equipment is designed in respect of its insulation [8].

At this point, the equivalent circuit of Figure 2 has been complicated and completed with the SCs that raise from that circuit. The final schematic is presented in Figure 3.

The SCs, as shown in Figure 3, are listed and described in Table 1 for the sake of clarity. Regarding  $C_H$  and  $C_L$ , the “\*” is to highlight that when the HV is shared between the dividers, as in one of tests described by [8], they do not exist. However, for a complete scenario that includes tests in which the two HVs may be different or with different phases, they have been included in the equivalent circuit.

At a glance, without preliminary studies but from their position, it is possible to predict the SCs that may affect the operation of the dividers, i.e.,  $C_{HLDUT}$  and  $C_{LG}$ . The following sections confirm or confute the hypothesis. It should be noted that, considering the model of Figure 3, more configurations that include SCs can be obtained from the circuit. Therefore, the model is not limited to the presented configuration.

Next, three test conditions are studied and used to obtain the SC expressions. They are listed in Table 2 and they represent a potential operating condition of the setup depicted in Figure 2. In detail, Section 3.3 exploits tests T1 to T3 to derive the CD input/output relation of each circuit. Finally, the results of Section 3.3 are used in Section 3.4 to obtain the SCs expressions.



**Figure 3.** The equivalent circuit of the setup in Figure 2 including the stray capacitances (SCs).

**Table 1.** List of SCs and their meaning.

Symbol	Details	Symbol	Details
$C_{HG}$	Capacitance between HV and ground	$C_H$	* Capacitance between the two HV
$C_{HLDUT}$	Capacitance between HV and LV of the DUT	$C_{HL1}$	Capacitance between HV of DUT and LV of the DD
$C_{LG}$	Capacitance between LV and ground	$C_{HL2}$	Capacitance between HV of DD and LV of the DUT
$C_L$	Capacitance between the two LV	$C_{HLDD}$	Capacitance between HV and LV of the DD

**Table 2.** Description of the test conditions considered in Section 3.2.

Test #	Description
T1	The dummy divider is grounded, hence, $HV_{DD}$ potential is ground
T2	The dummy divider is fed with the same voltage of the DUT
T3	Like T1 but without wall W

### 3.3. Circuitual Analysis with T1, T2, and T3

The main idea of the analysis is to obtain an equivalent circuit which obeys the conditions of the tests in Table 2. Afterwards, for each equivalent circuit, the associated input/output ratio  $k_i$  is calculated as follows:

$$k_i = \frac{V_p}{V_s}, \quad (4)$$

where  $V_p$  and  $V_s$  are the rms values of the primary and secondary voltage, respectively (see Figure 1).

For the sake of clarity, the  $V_s(t)$  defined to describe Figure 1 corresponds to the voltage between  $LV_{DUT}$  and ground; hence, the secondary voltage of the divider under test.

Starting from test T1, the equivalent circuit is depicted in Figure 4. Note, from the circuit, it can be appreciated which capacitors concur to the computation of the secondary voltage.

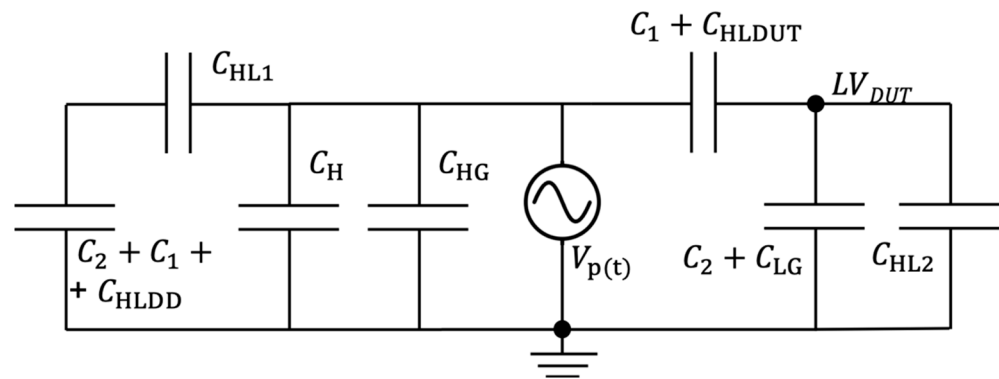


Figure 4. Equivalent circuit of the test condition T1.

Such capacitors are  $C_{HLDUT}$ ,  $C_1$ ,  $C_2$ ,  $C_{LG}$ , and  $C_{HL2}$ . Therefore, the secondary voltage of the circuit  $V_{sT1}(t)$  can be written as:

$$V_{sT1}(t) = V_p(t) \frac{C_1 + C_{HLDUT}}{C_1 + C_{HLDUT} + C_2 + C_{LG} + C_{HL2}}. \quad (5)$$

After some manipulation, and moving to a rms representation of the quantities, the ratio defined in Equation (4) can be obtained as:

$$k_{T1} = \frac{C_1 + C_{HLDUT} + C_2 + C_{LG} + C_{HL2}}{C_1 + C_{HLDUT}}. \quad (6)$$

The calculations to Equation (6) are replicated for T2. The main difference is the presence of two voltage sources which requires the use of the well-known superposition principle. Therefore, the two circuits to be analyzed are shown in Figure 5. Figure 5a represents the condition when the source in  $HV_{DUT}$  is considered, while Figure 5b represents the condition when the source in  $HV_{DD}$  is used.

Once the superposition principle has been applied to the circuits of Figure 5, the overall secondary voltage becomes:

$$V_{sT2}(t) = V_p(t) \frac{C_1 + C_{HLDUT} + C_{HL2}}{C_1 + C_{HLDUT} + C_2 + C_{LG} + C_{HL2}}, \quad (7)$$

And the ratio is easily found to be:

$$k_{T2} = \frac{C_1 + C_{HLDUT} + C_2 + C_{LG} + C_{HL2}}{C_1 + C_{HLDUT} + C_{HL2}}. \quad (8)$$

The last analysis considers the configuration T3 which does not involve the presence of the grounded wall W. Therefore, as previously done, the equivalent circuit without wall is the one presented in Figure 6, where all the symbols have been previously defined.

From the circuit, the secondary voltage can be written as follows:

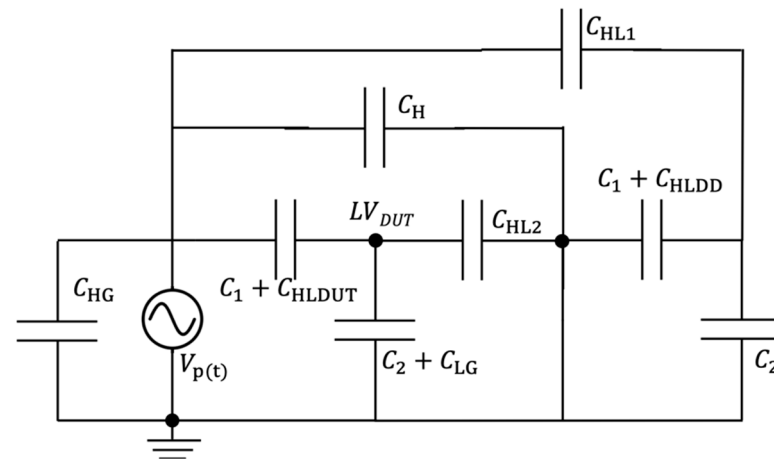
$$V_{sT3}(t) = V_p(t) \frac{C_1 + C_{HLDUT}}{C_1 + C_{HLDUT} + C_2 + C_{HL2}}, \quad (9)$$

and the ratio can be obtained as:

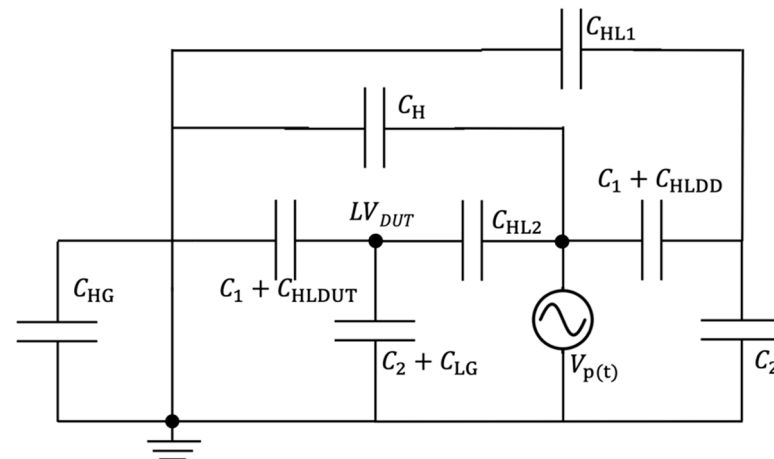
$$k_{T3} = \frac{C_1 + C_{HLDUT} + C_2 + C_{HL2}}{C_1 + C_{HLDUT}}. \quad (10)$$

It is important to highlight that, if in the above expressions of  $k_i$  all the SCs are neglected, the rated transformation ratio is easily obtained as in Equation (2).

Equations (2), (6), (8), and (10) are used in Section 3.4 to find the SCs expressions.

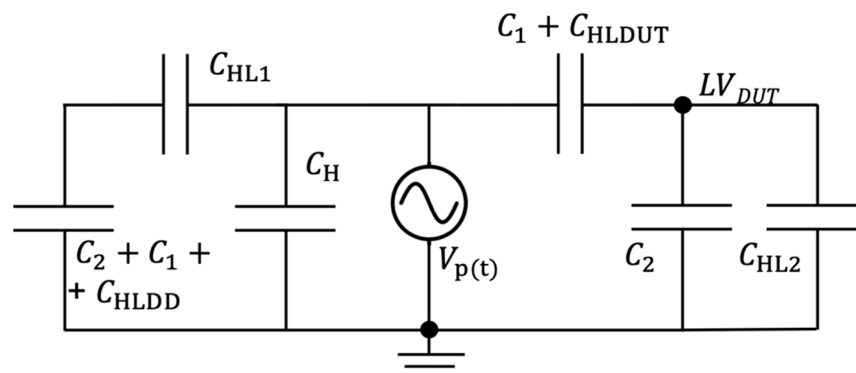


(a)



(b)

**Figure 5.** Equivalent circuit of the test condition T2. (a) When the source  $HV_{DUT}$  is considered; (b) When source  $HV_{DD}$  is considered.



**Figure 6.** Equivalent circuit of the test condition T3.

### 3.4. SCs Expressions

In Section 3.3, the actual ratio of the CD has been written in terms of the SCs to highlight their contribution to the ratio. In fact, the actual ratio directly affects the ratio error of the CDs. Therefore, the SC expressions are found by considering the ratio error of the measurements performed on configurations T1 to T3. In other words, let us assume



$\varepsilon_1$ ,  $\varepsilon_2$ , and  $\varepsilon_3$  to be the ratio error (as defined in the standard [6]) of measurements on configurations T1, T2, and T3, respectively. Then, the defined ratio errors can be written in terms of the  $k_i$ , previously found, as follows:

$$\varepsilon_1 = \frac{k_1 - k_{id}}{k_{id}}, \quad (11)$$

$$\varepsilon_2 = \frac{k_2 - k_{id}}{k_{id}}, \quad (12)$$

$$\varepsilon_3 = \frac{k_3 - k_{id}}{k_{id}}. \quad (13)$$

By substituting the expressions of the  $k_i$  inside Equations (11)–(13), one obtains:

$$\varepsilon_1 = \frac{C_1 C_{LG} + C_1 C_{HL2} - C_2 C_{HLDUT}}{(C_1 + C_2)(C_1 + C_{HLDUT})}, \quad (14)$$

$$\varepsilon_2 = \frac{C_1 C_{LG} - C_2 C_{HLDUT} - C_2 C_{HL2}}{(C_1 + C_2)(C_1 + C_{HLDUT} + C_{HL2})}, \quad (15)$$

$$\varepsilon_3 = \frac{C_1 C_{HL2} - C_2 C_{HLDUT}}{(C_1 + C_2)(C_1 + C_{HLDUT})}. \quad (16)$$

Inside the three expressions, the unknowns are exclusively the three SCs. Therefore, solving the linear system of three equations with three unknowns leads to the following:

$$C_{HL2} = \frac{C_1 C_2 (\varepsilon_1 - \varepsilon_2)}{C_1 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 - \varepsilon_1] + C_2 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 + 1]}, \quad (17)$$

$$C_{LG} = \frac{C_2^2 [-\varepsilon_2 \varepsilon_3 - \varepsilon_3 + \varepsilon_1 (\varepsilon_2 + 1)] + C_1 C_2 [-\varepsilon_2 \varepsilon_3 - \varepsilon_3 + \varepsilon_1 (\varepsilon_2 + 1)]}{C_1 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 - \varepsilon_1] + C_2 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 + 1]}, \quad (18)$$

$$C_{HLDUT} = -\frac{C_1^2 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 - \varepsilon_1] + C_1 C_2 (\varepsilon_2 \varepsilon_3 + \varepsilon_3)}{C_1 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 - \varepsilon_1] + C_2 [\varepsilon_2 (\varepsilon_3 + 1) + \varepsilon_3 + 1]}. \quad (19)$$

Despite the complicated appearance, the closed Expressions (17)–(19) can be used to find the SCs of the considered HV circuit, by knowing the ratio error measured for the three configurations T1 to T3 and the primary and secondary capacitance of the adopted divider. It is worthwhile to note that the expressions have been found without knowing the detailed geometry of the equipment and the location. Furthermore, no complicated finite element analysis has been performed.

Another interesting observation is that, if  $\varepsilon_3 = \varepsilon_2 = \varepsilon_1 = 0$ , hence an ideal condition of no SCs in the circuit, Expressions (17)–(19) provides  $C_{HL2} = C_{LG} = C_{HLDUT} = 0$  as expected. Therefore, at this point, the theoretical correctness of the closed expression is confirmed.

#### 4. Implementation and Validation

In this section, first of all, measurement results of laboratory experimental activities are used to quantify the SCs. Afterwards, the obtained SCs are used to simulate the complete equivalent circuit of Figure 3 (in light of what has been described above) to be used as a verification tool for the obtained expressions.

##### 4.1. SC Computation from Experimental Results

To implement Expressions (17)–(19), measurement results obtained from tests in a HV laboratory, performed on real CDs, are used. In particular, for each configuration of Table 2, one ratio error measurement has been performed. The results are listed in Table 3.

**Table 3.** Ratio error measurements results for each test.

Test #	Ratio Error (%)
T1	0.484
T2	0.195
T3	0.356

By considering the rated values of capacitance of the device under test,  $C_1 = 225$  pF and  $C_2 = 450$  nF, the application of Expressions (17)–(19) provides the following:

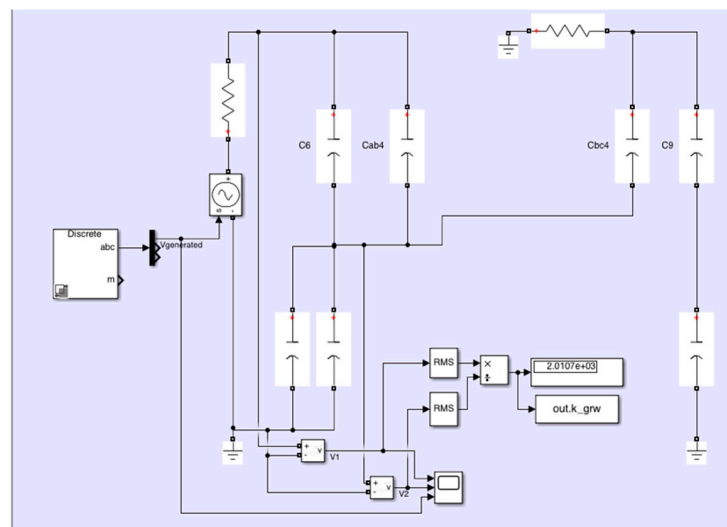
$$C_{HL2} = 0.646 \text{ pF} \quad C_{LG} = 0.574 \text{ nF} \quad C_{HLDUT} = -0.798 \text{ pF}, \quad (20)$$

where the minus of  $C_{HLDUT}$  takes into account the voltage drop sign variation, among configurations T1 to T3. From (20) it can be concluded that the obtained values for the SCs are significantly smaller than  $C_1$  and  $C_2$ , hence, aligned with the definition of SC. However, despite the almost negligible amplitude, they produce significant variations to the ratio error, as confirmed by Table 3.

#### 4.2. Validation from Simulation

In this section, by means of simulations in the MatLab Simulink environment, some test configurations are run, which are describe below.

A screenshot of the developed Simulink model is shown in Figure 7. The entire model has been omitted for the sake of brevity.

**Figure 7.** Screenshot of the equivalent circuit model developed with the Simulink environment.

In addition to configurations T1–T3, which are simulated to numerically confirm the results of the circuit analysis, further configurations are implemented in the Simulink environment. Such configurations replicate experimental ones that were not used to derive the SC values but for which the ratio errors were measured. Hence, they are used as benchmarks to assess if the obtained SCs can be used to predict the ratio errors in those situations. These new configurations are referred to as T4, T5, and T6. Configuration T4 is identical to T2 but without the grounded wall W; configuration T5 instead is identical to T2 but the DD is fed with a voltage of the same amplitude but with  $180^\circ$  phase shift as compared with the voltage applied to the DUT. Finally, configuration T6 is identical to T5 but without the presence of the grounded wall. Furthermore, all configurations T1–T6 have been tested and simulated by applying 100%, as well as 80% of the rated voltage  $V_n$ , as defined in [8]. This further test has been done to verify that the amplitude of the applied

voltage does not affect the model of Figure 8 and the accuracy of a CD. Hence, this test confirms that the SC expressions are not influenced by the voltage amplitude, which, at the same way, does not influence the real in-lab test accuracy measurements.

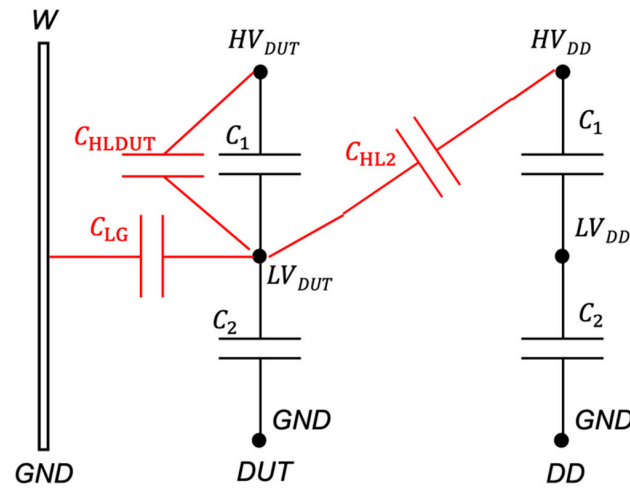


Figure 8. The final equivalent circuit of the setup in Figure 2 including the significant SCs.

As it is clear, T4 to T6 have not been used in the computation of the SC expressions; hence, as written above, they are used for assessing their validity.

Inserting the SCs of (20) inside the model and running the simulations for T1 to T6 provides the estimated ratio errors  $\varepsilon_e$ , shown in Table 4, where the corresponding in-field measured ratio error  $\varepsilon_m$  are also reported for the sake of comparison.

Table 4. Comparison between the measured and the estimated ratio errors.

Test #	$\varepsilon_m$ [%]		$\varepsilon_e$ [%]	
	$0.8V_n$	$V_n$	$0.8V_n$	$V_n$
T1	0.480	0.484	0.484	0.484
T2	0.194	0.195	0.195	0.195
T3	0.352	0.356	0.356	0.356
T4	0.050	0.054	0.067	0.067
T5	0.765	0.772	0.774	0.774
T6	0.650	0.652	0.646	0.646

#### 4.3. Discussion

Several points can be highlighted from both the circuital analysis in Section 3 and the results in Table 4. The first point concerns the usefulness of the considered SCs. In fact, some SCs do not contribute to the ratio error of the CD, hence, they do not influence its accuracy. Therefore, starting from the model of Figure 3, a new and simpler model can be drawn. The model is depicted in Figure 8, and it contains, as unique contributors to the ratio error,  $C_{HL2}$ ,  $C_{HLDUT}$ , and  $C_{LG}$ .

A second point concerns the obtained Expressions (17)–(19). Notably, by simply knowing the capacitance values of the CDs (provided on the nameplate) and the ratio errors of some test configurations, it is possible to obtain the set of SCs that identify the non-idealities of the considered circuit.

A third point concerns the simulations performed to validate the applicability of the presented expressions. As shown in Table 4, for all configuration T1–T6 and both voltage levels tested, the simulations containing the SCs obtained with Expressions (17)–(19) provide excellent results. Furthermore, what emerges from the results is that the proposed model and

the obtained expressions are sufficiently accurate to describe the stray capacitance behavior in various conditions. For example, they can be used to distinguish whether or not there is a grounded wall, or if the DD is fed with an in-phase or an opposite-phase voltage. This result demonstrates the sensitivity and the effectiveness of the proposed approach.

A final point concerns the ease of applicability and usefulness of the SC expressions. In fact, the limited information required to implement the expressions and their simplicity make them an interesting and effective tool for system operators, researchers, and manufacturers. In detail, manufacturers could use the presented expressions to preliminarily test their products in order to understand whether and in which configuration they are compliant with the accuracy limits defined by the standards (see [5,6,8]) and, in the light that the considered configurations rely on that defined in [8], for assessing the immunity of CDs to external electric fields.

## 5. Conclusions

Stray capacitances are an undesired side effect that affect several fields and applications. They are typically treated with complex and long finite element analysis, or for very simple geometries with known equations that are not practical and flexible. Therefore, this work differs from the existing literature because it treats stray capacitance with a numerical approach that starts from a simple equivalent circuit obtained from the standards. The device, in which the stray capacitances are evaluated, is a high-voltage capacitive divider. In the work, closed expressions of the main stray capacitances are found starting from the knowledge of the ratio error of the device, measured in several configurations. The obtained expressions are evaluated with real ratio error measurements and inside a simulation environment to reproduce the real setup. All results confirm the validity and the applicability of the found expressions; furthermore, their ease of use and implementation may facilitate system operators and researchers in the study of stray capacitances of typical measurement setups. In other words, whoever is going to work with high-voltage dividers may use the proposed expressions to model its own equivalent circuit, quantifying the contribution of stray capacitances to the device accuracy.

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