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A Clockless Temperature-Compensated Nanowatt Analog Front-End for Wake-Up Radios Based on a Band-Pass Envelope Detector

This is the final peer-reviewed author's accepted manuscript (postprint) of the following publication:

Published Version:
Elgani A.M., Renzini F., Perilli L., Franchi Scarselli E., Gnudi A., Canegallo R., et al. (2020). A Clockless Temperature-Compensated Nanowatt Analog Front-End for Wake-Up Radios Based on a Band-Pass Envelope Detector. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. I, REGULAR PAPERS, 67(8), 2612-2624 [10.1109/TCSI.2020.2987850].

Availability:
This version is available at: https://hdl.handle.net/11585/792922 since: 2021-01-29

Published:
DOI: http://doi.org/10.1109/TCSI.2020.2987850

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(Article begins on next page)

12 October 2024

This is the post peer-review accepted manuscript of:

A. M. Elgani, F. Renzini, L. Perilli, E. Franchi Scarselli, A. Gnudi, R. Canegallo and G. Ricotti

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IEEE Transactions on Circuits and Systems I: Regular Papers, date of Publication: 28 April 2020

The published version is available online at: https://doi.org/10.1109/TCSI.2020.2987850

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A Clockless Temperature-Compensated Nanowatt Analog Front-End for Wake-Up Radios Based on a Band-Pass Envelope Detector

Alessia M. Elgani, Francesco Renzini, Luca Perilli, Eleonora Franchi Scarselli, *Member, IEEE*, Antonio Gnudi, *Member, IEEE*, Roberto Canegallo, and Giulio Ricotti

***Abstract*—This paper presents an Analog Front-End for integrated Wake-Up Radios. The proposed Analog Front-End is composed of an envelope detector, a Schmitt trigger and a biasing block and has three distinctive features: i) clockless solution, which does not require an always-on oscillator; ii) an envelope detector with band-pass response which leads to smaller capacitance, thus easier integration, and low-frequency noise suppression; iii) temperature compensated biasing scheme. An active scheme for the detector is used based on MOSFETs operated in the subthreshold region with a self-biased topology. Advantages and drawbacks of the proposed architecture are analyzed. A prototype was fabricated in the STMicroelectronics 90-nm BCD technology. The overall power consumption, excluding the biasing block, is 36 nW at 1.2 V. A 10^{-3} Bit Error Rate is measured with a 771-MHz, 2-kbit/s OOK modulated input signal with -46 dBm power at room temperature and at -20 °C, and with almost -43 dBm power at 60 °C.**

***Index Terms*—Wake-Up Radio (WUR), OOK modulation, envelope detector, ultra-low-power, subthreshold operation.**

I. Introduction

LOW-power Wireless Sensor Networks (WSNs) have been key since the rise of the Internet of Things (IoT). Nodes are usually battery-powered, which sets strict constraints on their consumption. Several hardware-software solutions, as well as new protocols, have been proposed in order to improve battery lifetime. Since most of the node power consumption is due to the wireless transceiver, a popular solution is the reduction of communication activity. However, the well-known drawback of this approach is the introduction of latency.

The Wake-Up Radio (WUR) is a valid alternative, as it represents an emerging technology that enables asynchronous communication schemes while reducing overall power consumption. WURs are always-on devices with the main task of continuously monitoring the channel and waking up the microcontroller (MCU) or the main radio only when a wake-up signal is received. Several WUR hardware designs have recently been presented employing both discrete components and integrated solutions [1]-[13]. On-Off Keying (OOK) is the most common modulation method due to the simplicity of its demodulator circuit. Moreover, the 868-MHz ISM band is often used.

As shown in Fig. 1.a, WURs are usually composed of an Analog Front-End (AFE), which turns the input RF signal into a bitstream, and a baseband logic, which is generally implemented through digital correlators and carries out the addressing, along with an internal oscillator for data synchronization. The Wake-Up signal is generated only if the incoming bitstream corresponds to the address of the specific node. Therefore, the WUR usually receives only short bit sequences, ranging from 11 bits [10] to 40 bits [11].

Fig. 2.a shows the typical AFE of an integrated WUR. An external high-Q matching network is typically employed to match the antenna impedance and provide voltage amplification. It is followed by a detector to extract the envelope, a baseband amplifier for the envelope signal and a comparator to digitize it. Envelope extraction is either performed through passive rectification [4][5][8][10]-[12], where an actual baseband amplifier follows, or leveraging the second order non-linearities of a MOSFET in the subthreshold region [3][6][7][9], within an envelope detector (ED) which also performs baseband amplification.

Sensitivity/power-consumption is the most important trade-off when studying WUR AFEs. Nanowatt WURs usually target medium-range (at most 100m) applications and are useful for indoor applications [1], where sensor nodes are tens of meters away. Moreover, low throughput applications are usually targeted, as low bitrates allow the minimization of integrated noise and the maximization of sensitivity [4][5][7]-

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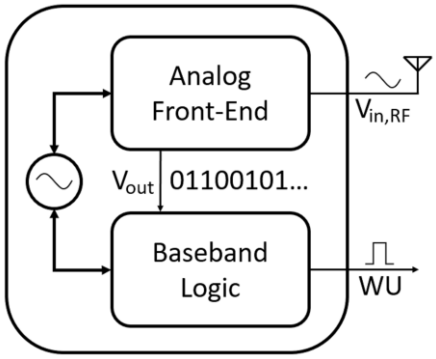

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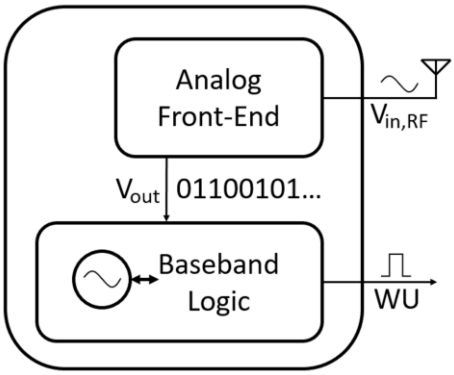


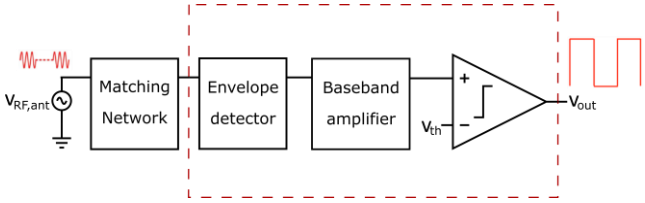
b.

Fig. 1.: a. High level block diagram of a generic clocked WUR.
b. High level block diagram of a generic clockless WUR.

[10]. Also, low supply voltages enable the minimization of power consumption [5]-[12].

The main goal of this paper is to assess the performances of an innovative kind of WUR AFE, underlining its advantages and drawbacks. Distinctive features of the hereby proposed circuit are: i) clockless solution, which does not require an always-on oscillator; ii) band-pass response for easier integration and low-frequency noise suppression; iii) temperature compensated biasing scheme. Only the AFE is considered in this paper, therefore addressing capabilities are not included. A preliminary analysis was presented in [14]. A specific design targeting nanowatt power consumption with a Manchester coded 0.5-kbit/s OOK modulated input signal and a carrier frequency in the ISM band is discussed. The measurement results of a prototype circuit manufactured in a smartpower STMicroelectronics 90-nm BCD technology are also presented. This choice is intended to make integration of the WUR possible in end-nodes of the IoT world, which have actuating capabilities as well as sensing, communication and elaboration ones, such as the one in [15].

The paper is organized as follows: in Section II the main architectural choices and specifications are discussed, whereas in Section III the circuit is described. In Section IV, simulated results are shown. In Section V, the prototype is presented along with measurement results. Section VI shows a comparison between the proposed WUR and the state-of-the-art, while conclusions are drawn in Section VII.



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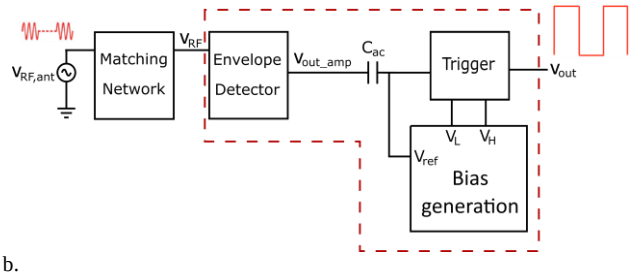

b.

Fig. 2.: a. High level block diagram of a generic integrated WUR AFE.
b. High level block diagram of the proposed integrated circuit.

II. Architectural Choices and Specifications

A. *Clocked vs. clockless AFE*

Most integrated architectures known from literature [2][4]-[10][12] include an oscillator which is constantly on, as shown in Fig. 1.a. The clock is essential in the baseband logic for data extraction, but it is also beneficial for the AFE, where it allows the use of latched comparators, which would not be feasible otherwise. Indeed, latched comparators are typically faster than conventional ones at parity of current thanks to positive feedback and also allow the implementation of offset cancellation techniques [16]. However, the clock consumes power, even if calibrated low-power RC oscillator designs are adopted.

Conversely, in this paper a clockless approach for the AFE was chosen, as shown in Fig. 1.b, where the oscillator is turned on only upon reception of the first bit of an incoming message and turned off once the whole message has been received, as recently proposed also in [11]. The circuit operates in two phases. During the first phase, the AFE is the only active section. When recognition of the first bit of the message takes place, which occurs at the first transition of the AFE output signal, the second phase starts: the oscillator and the baseband logic are turned on and the incoming bitstream is compared with the stored address. If the transition causing the second phase to start is spurious (solely due to noise), the oscillator and baseband logic turn back off after a predefined time interval, pushing the circuit back into the first phase [17]. If P_1, t_1, P_2, t_2 are the power and the ON time of the two phases, the average power consumption can be calculated as [11]

$$P_{avg} = \frac{P_1 t_1 + P_2 t_2}{t_1 + t_2}. \quad (1)$$

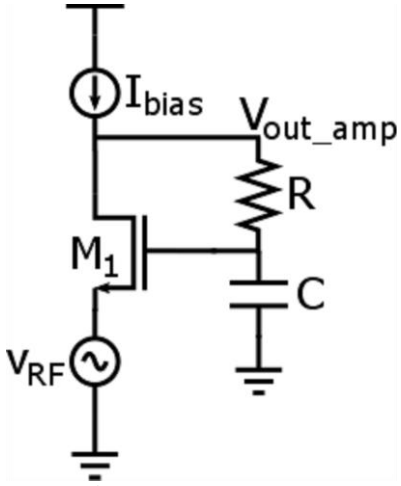

Fig. 3. Basic topology of an active envelope detector [9].

This implies that if the specific application is characterized by long idle periods, i.e. $t_2/t_1 \ll 1$, in a clockless AFE architecture $P_{avg} \sim P_1$, which means the logic and the oscillator do not count in terms of power, but their functionalities are available nonetheless. In the actual implementation, the time required for the oscillator to start must be taken into account as well (the baseband logic does not pose the same problem since it is a digital circuit). Although this aspect is not addressed in this paper, details can be found in [17], where a relaxation oscillator is employed for Clock and Data Recovery. In [17] it is shown that the oscillator start time is within 2 bit-times and this implies that a very short preamble is sufficient to prevent errors after the first transition of the AFE output signal.

B. Envelope detector

Envelope detectors can be either active, typically a common-source or common-gate topology [3][6][7][9][14], or passive, typically diode detectors [4][5][8][10]-[12], such as the Dickson one. Passive detectors have no power consumption but are proven to be less effective than active ones in terms of noise-equivalent power when higher bitrates, thus higher bias currents, are involved [8]. Actually, the use of passive detectors normally requires the cascade of several tens of stages in order to provide a high enough output voltage. In turn, this seems to reduce the bandwidth of such detectors, making their use effective only with bitrates below 1 kbit/s. In [12] a 10-stage passive detector is used with a high bitrate, 400 kbit/s, but subsequent baseband circuits need hundreds of nA and are also required to perform filtering. Therefore, in this paper it was chosen to employ an active ED in order to achieve bitrate scalability, as will be clear in Section II.D.

Our ED is an elaboration of the topology proposed in [9], which is reported in Fig. 3 for convenience. The main advantage of that circuit is its simplicity and low current, as it is composed of only one branch. Transistor M_1 operates in the subthreshold region and works as a common gate amplifier, provided capacitor C is large enough to effectively ground the gate for all frequencies within the signal band, as well as a rectifier, exploiting the exponential I-V_{GS} subthreshold characteristic. Resistance R provides the bias to the gate of

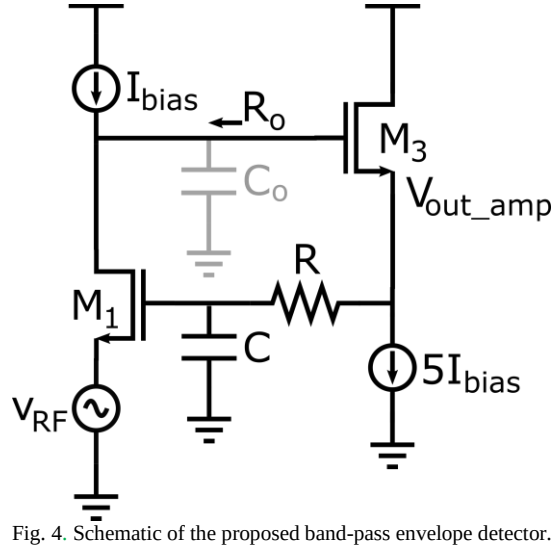

Fig. 4. Schematic of the proposed band-pass envelope detector. C_o accounts for all parasitic capacitances at the drain of M_1.

M_1, which is therefore self-biased. However, a drawback is the need for R to be prohibitively large in order to provide enough voltage gain, given the small transconductance value in subthreshold. In [9] this problem was circumvented by replacing R with MOSFETs in the OFF state. In turn, this required 8 bits for calibration against process variations.

Conversely, as shown in Fig. 4, we chose to add a follower, M_3, to be able to implement R with an actual resistor without compromising the baseband gain and thus eliminating, or at least reducing, the need for calibration against process variations. This of course comes at the expense of an additional current branch. Both M_1 and M_3 operate in subthreshold. If

$$v_{RF}(t) = V_{OOK}(t)\cos\omega t \tag{2}$$

is the input RF voltage, where $V_{OOK}(t)$ is the OOK envelope signal, assuming the gate of M_1 to be grounded by capacitance C at the carrier angular frequency ω, the drain current of M_1 can be written as

$$I_{D1} = I_{bias}e^{-\frac{v_{RF}}{nV_T}} \approx I_{bias}\left[1 - \frac{v_{RF}}{nV_T} + \frac{1}{2}\left(\frac{v_{RF}}{nV_T}\right)^2\right], \tag{3}$$

where n is the subthreshold ideality factor and V_T the thermal voltage. Substituting (2) into (3) and assuming the high-frequency components in (3) to be grounded by parasitic capacitances at the drain of M_1, the low-frequency components of the drain current, which are the only ones contributing to the ED gain, can be written as

$$I_{D1,LF} = I_{bias}\left[1 + \frac{V_{OOK}^2(t)}{4n^2V_T^2}\right] \equiv I_{bias} + \Delta I(t). \tag{4}$$

The envelope-dependent part $\Delta I(t)$ can be equivalently attributed to an effective low-frequency input voltage source $v_{IN}(t)$ replacing $v_{RF}(t)$

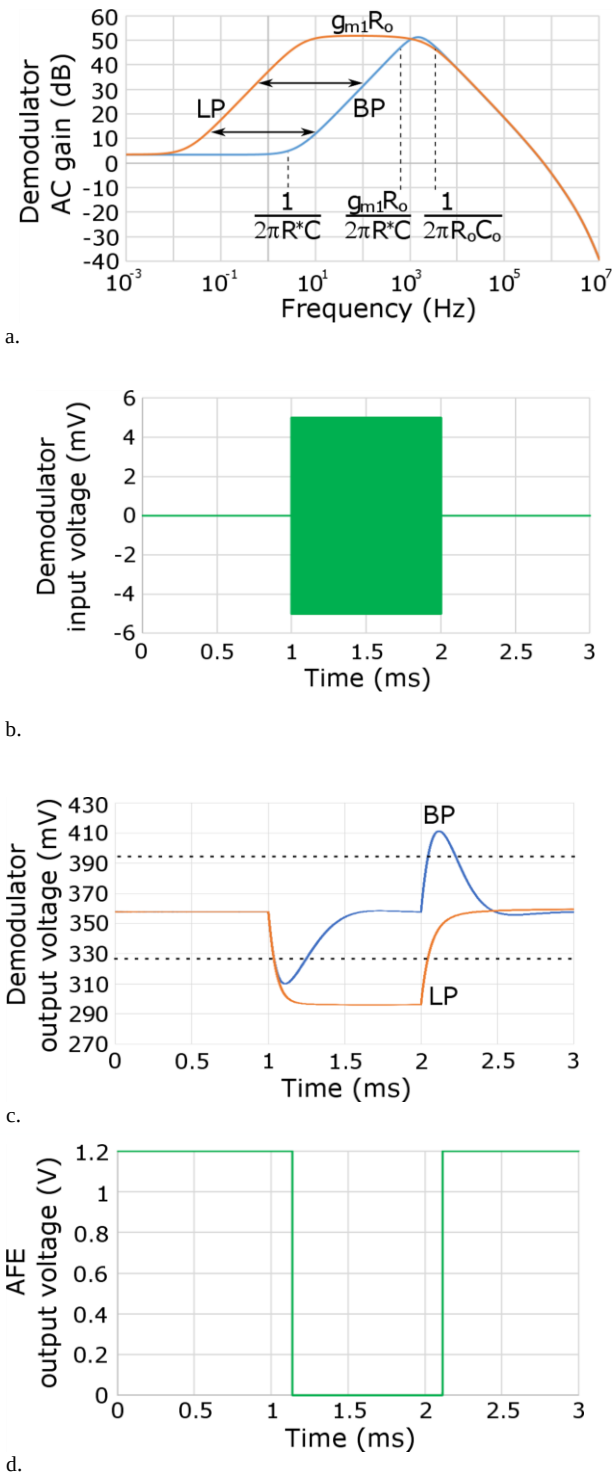

Fig. 5. a.: simulated frequency response of the envelope detector: v_{out_amp}/v_{IN} for C = 100 nF (orange) and for C = 500 pF (light blue).
b.: input RF signal.
c.: simulated time-domain response of the envelope detector: v_{out_amp} for C = 100 nF (orange) and for C = 500 pF (light blue). The thresholds are also visible in dotted line.
d.: simulated time-domain response in both cases.

$$v_{IN}(t) \equiv \frac{\Delta I(t)}{g_{m1}} = \frac{V_{OOK}^2(t)}{4nV_T} \quad , \tag{5}$$

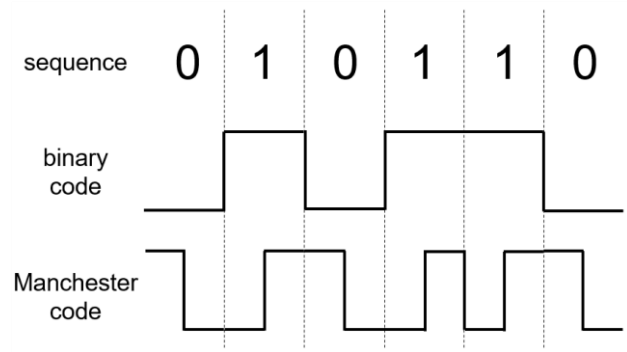

Fig. 6. Binary vs. Manchester coded sequence.

where the expression of the transconductance of M_1 in subthreshold $g_{m1} = I_{BIAS}/nV_T$ has been used.

By circuit inspection and assuming unity gain for the follower for simplicity, the expression of the approximated small-signal amplifier response to $v_{IN}(t)$ can be derived to be

$$\frac{v_{out_amp}}{v_{IN}}(s) = -\frac{1 + sR^*C}{(1 + s\frac{R^*C}{g_{m1}R_o})(1 + sR_oC_o)}, \tag{6}$$

where $R^* = R + R_{OUTFOLL}$, with $R_{OUTFOLL}$ the output resistance of the follower stage, $R_o = r_{out1}$ is the output resistance at the drain of M_1, where $r_{out1} = 1/\lambda I_{BIAS}$, and C_o is the total capacitance seen between the drain of M_1 and ground, due to the current generator, M_3 and parasitics. Equation (6) shows that the low-frequency gain is close to one as a result of the negative feedback. For angular frequencies above $1/R^*C$, capacitance C progressively shorts the gate of M_1 to ground and the gain increases up to its peak value, equal to $g_{m1}R_o$ for the case of well separated poles, when M_1 behaves as a common gate stage. The second pole is due to the capacitance and the resistance at the drain of M_1.

The main noise contributors are M_1 and current generator I_{bias} and the output noise shaping function can be proved to be similar to (6).

C. Band-pass vs. low-pass envelope detection

Most EDs presented in literature have a response that can be classified (somewhat improperly) as low-pass (LP). It can be obtained from (6) by fixing the R^*C time constant to a large enough value so as to place the first pole $(g_{m1}R_0/R^*C)$ at a frequency lower than the inverse of the total transmission time, in order to have an effective LP time response across all received bits. This type of frequency response is shown in Fig. 5.a (orange line), while the corresponding time-domain response is reported in Fig. 5.c, assuming the input RF signal portrayed in Fig. 5.b. The second pole $(1/R_0C_0)$ must be placed at a frequency close to the maximum bitrate that the system is supposed to handle. In general, higher bitrates require larger drain currents through M_1, given the dependence of R_o on the bias current. In such LP solutions, a limitation is represented by the low-frequency flicker noise. For example, for a 1-kbit/s bitrate and a 30-bit transmission the first

TABLE I. PERFORMANCE COMPARISON BETWEEN BAND-PASS AND LOW-PASS ENVELOPE DETECTORS

Response shape	Capacitance	Power (P*dc*) [nW]	Bitrate (BW) [kbit/s]	Estimated sensitivity (P_{SEN}) [dBm]	Estimated normalized sensitivity ($P_{SEN,norm}$) [dB]
BP	500 pF	7.2	0.5	-34.9	-48.4
LP	100 nF	7.2	1	-34.2	-49.2

TABLE II. PERFORMANCE COMPARISON BETWEEN LOW AND HIGH THROUGHPUT BAND-PASS ENVELOPE DETECTOR

Response shape	Capacitance	Power (P*dc*) [nW]	Bitrate (BW) [kbit/s]	Estimated sensitivity (P_{SEN}) [dBm]	FoM_1 [dB]	FoM_2 [dB]
Low thr.	500 pF	7.2	0.5	-34.9	89.5	99.8
High thr.	5 pF	720	50	-34.9	89.5	89.8

frequency must be around a few Hz, and flicker noise reduction requires to increase the area of M_1 and M_3. This in turn leads to a larger capacitance C_o and hence a larger I_{bias} to guarantee the required second pole frequency.

An alternative solution, which is investigated in this paper, is to adopt a truly band-pass (BP) response for the ED. This is obtained by placing the first pole close to the second pole, as shown in Fig. 5.a (blue line). The BP time response (Fig. 5.c, blue line) is characterized by a positive/negative output pulse corresponding to each falling/rising edge transition in the input envelope, which means that envelope transitions are recognized (edge detector) rather than the envelope itself. For the correct operation of the BP edge detector, the first pole must be high enough to guarantee the relaxation of the output signal to its quiescent value within one bit-time, so as to avoid inter-bit interference. This of course also improves flicker noise suppression and in addition leads to a smaller value of capacitance *C*, also amenable for integration. On the other hand, too small of an R^*C constant would kill the amplitude of the output pulse. Assuming the use of an ideal OOK modulation, the pulse peak amplitude V_{OUTM}, as obtained from (5) and (6), is

$$V_{OUTM} \propto \frac{g_{m1}R_o}{4nV_T}V_{OOKM}^2, \qquad (7)$$

where V_{OOKM} is the amplitude of the input envelope.

In order to recover an envelope signal with full digital level from the output pulses of the edge detector, a comparator with hysteresis, i.e. a trigger with two thresholds, is well suited. Its behavior is illustrated by the waveforms in Fig. 5.c and 5.d. The two thresholds can be adjusted for best rejection of input noise and interferences, depending on the signal amplitude. The positive feedback inherent in the trigger operation allows fast switching even with very small currents.

A possible drawback of the trigger is that, in case of sequences of identical transmitted bits, the occurrence of a detection error due to noise at the beginning of the sequence causes the misdetection of the entire sequence. This problem can be minimized by using codes with frequent transitions. As an extreme choice, a Manchester coding scheme can be adopted, where a logic 0 is represented by a high-to-low transition in the bit-time while a logic 1 by a low-to-high transition (see Fig. 6). On the other hand, for the same bitrate, this requires to double the detector bandwidth, with a penalty in terms of current.

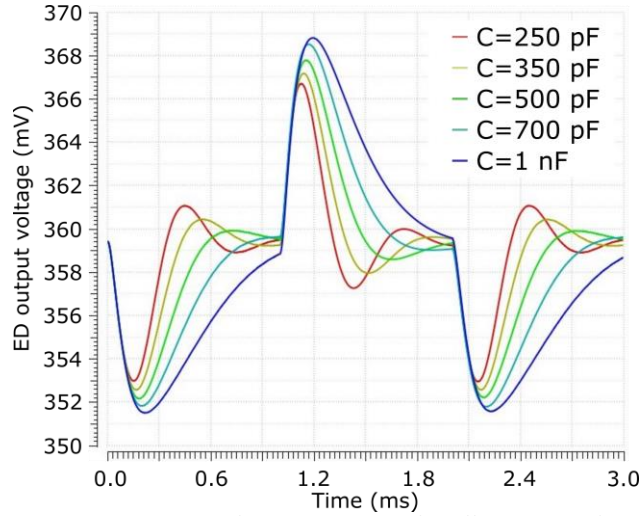

Fig. 7. ED output signal of the circuit in Fig. 4 for different values of *C* with a 5-mV RF input.

A BP and a LP version of the ED in Fig. 4 were designed for comparison, assuming the same bias current for the two designs. Sensitivity (P_{SEN}) and bitrate (BW) are taken into account to calculate the normalized sensitivity ($P_{SEN,norm}$) [11], which we hereby use to assess the performances of the EDs only,

$$P_{SEN,norm}(dB) = -P_{SEN}(dBm) + 5\log BW \qquad (8)$$

where P_{SEN} is defined as the value of the voltage V_{OOKM} (measured in dBm on a reference 50-Ω resistance) corresponding to 11-dB SNR at the ED output [18]. Results are based on simulations. Since both designs have the same total current (6 nA, of which I_{bias} = 1 nA and 5 nA in the follower, with V_{DD} = 1.2 V), the second pole is at the same frequency, which has been fixed at roughly 1 kHz, that is the bitrate of the LP ED, while the BP detector uses a Manchester coded signal with 0.5 kbit/s rate. In both designs *R* = 75 MΩ. The choice of *C* = 500 pF for the BP version was driven by the results in Fig. 7, which shows the ED output signal of the circuit in Fig. 4 for different values of *C* with a 5-mV RF input. As stated in Section II.B, (6) was derived modeling the follower as a unity gain block. Actually, it is apparent from Fig. 7 that this is not true, since a ringing response appears when the pole due to *C* is too close to the second one, which occurs when *C* is too small. The analysis of the ratio between the output peak amplitude and the total RMS output noise voltage indicates it is advantageous to maximize *C*, in the range between 250 pF and 1 nF, for maximum SNR. Yet, too large values for *C* must be avoided to allow the output voltage to relax to its quiescent value within one bit-time, preventing the risk of inter-bit interference. On the other hand, in the LP case *C* = 100 nF. It is clear that a 500-pF capacitance could be integrated (with the chosen technology), as an integrated capacitor of this value has an estimated area of 190 µm · 190 µm (1.2-V poly-on-pplus capacitor), while a 100-nF *C* would certainly have to be off-chip.

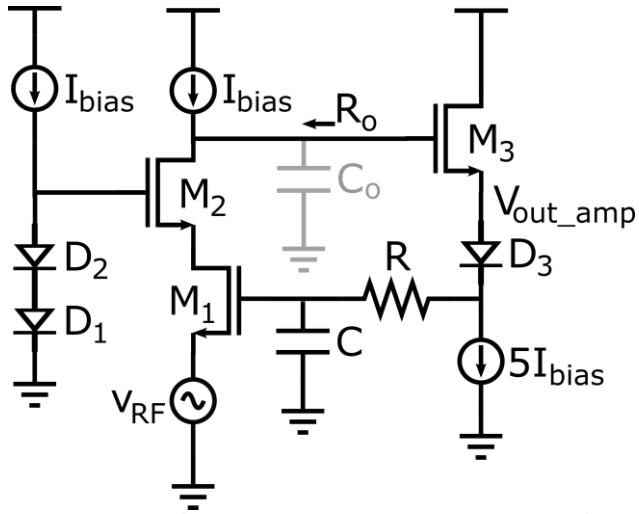

Fig. 8. Schematic of the proposed envelope detector. C_o accounts for all parasitic capacitances at the drain of M_2. I_{bias} is copied from M_1 in Fig. 11. Diodes are implemented through diode-connected MOSFETs.

The results, shown in Table I, indicate that there is no significant difference between the two cases in terms of estimated normalized sensitivity, the halving of the bitrate in the BP solution being on average compensated by its better sensitivity, mainly due to a more efficient suppression of flicker noise. The rest of the paper will focus on an exploratory design of an ED stage with BP response.

D. Design scalability of the BP ED

The generic BP topology in Fig. 4 can also be easily customized according to the throughput required for the chosen application. For instance, the frequency of the second pole is multiplied by a factor k whenever I_{bias} is multiplied by k, whereas the frequencies of the zero and the first pole are multiplied by the same factor k when capacitance C is divided by k. So this topology can be implemented for both low and high throughput applications, where the high throughput requires a higher current and a smaller capacitance than the low throughput one, making the integration of C even more practical. The sensitivity, closely linked to the integrated noise, stays roughly the same in the two cases (in accordance with the fact that, with a higher throughput, a lower power spectral density is integrated over a wider bandwidth).

The performances of the circuit in Fig. 4 for low and high throughput were compared and results are shown in Table II. A new Figure of Merit (FoM), FoM_1, was defined, as thoroughly described in the Appendix.

$$FoM_1(dB) = -P_{SEN}(dBm) + 5\log BW - 5\log I_{bias} \quad (9)$$

Nevertheless, the FoM as defined in [9] was also used:

$$FoM_2(dB) = -P_{SEN}(dBm) + 5\log BW + -10\log\frac{P_{dc}}{1\,mW}. \quad (10)$$

FoM_2 takes into account the supply voltage, which enters the DC power consumption P_{dc}. Moreover, dependence on current consumption is different in the two figures. On the other hand, as explained in the Appendix and confirmed by the results shown in Table II, FoM_1 proves to be an invariant for a given architecture and, therefore, a suitable figure to compare the performances of different architectures.

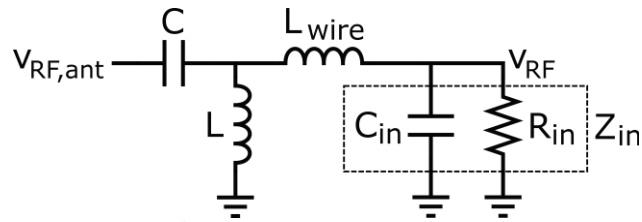

Fig. 9. Schematic of the proposed matching network. Z_{in} indicates the input impedance of the ED.

As for the actual current consumption in the low and the high throughput cases, the low throughput ED consumes 6 nA, whereas the high throughput ED consumes 600 nA, as shown in Table II.

E. AC coupling between BP ED and trigger

Due to the BP response of the ED, it is natural to employ an AC-coupling between the ED itself and the trigger, as shown in Fig. 2.b, as it involves no loss of information. This leaves the possibility of biasing the trigger independently of the output DC voltage of the ED. In the next Section, a circuit is proposed for the generation of the two threshold voltages as well as the input DC voltage for the trigger independently of the detector output and robustly against process and temperature variations, without the need for additional circuits for calibration. Thresholds only need to be trimmed according to the signal amplitude at the ED input, which in turn depends on the distance between nodes and the application.

F. Circuit specifications

It was chosen to address applications requiring transmission in the kbit/s range. More precisely, the design targets nanowatt power consumption and a Manchester coded 0.5 kbit/s OOK modulated bitstream with a carrier frequency in the ISM band.

While supply voltage reduction helps decrease the power consumption of the system, it requires the addition of voltage regulators, which consume power themselves, occupy area and increase the complexity of the system. Therefore, in this paper we chose to employ the nominal supply voltage of the STMicroelectronics 90-nm BCD technology, 1.2 V.

III. Circuit Description

The block diagram of the proposed circuit is shown in Fig. 2.b. It reflects the choices presented in Section II: the BP ED is AC-coupled to a Schmitt trigger through capacitance C_{ac} and a specific biasing block provides reference voltage V_{ref} and threshold voltages V_H and V_L for the trigger. As mentioned in the Introduction, the baseband logic is not included in this design, which therefore has no addressing capabilities.

A. Envelope detector

The scheme of the implemented ED is shown in Fig. 8. It differs from the one already discussed in Fig. 4 essentially for

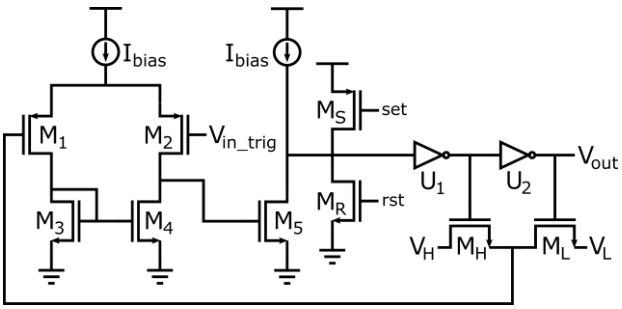

Fig. 10. Schematic of the trigger including the two-stage differential amplifier and the switches for the threshold voltage feedback. I_{bias} is copied from M_1 in Fig. 11.

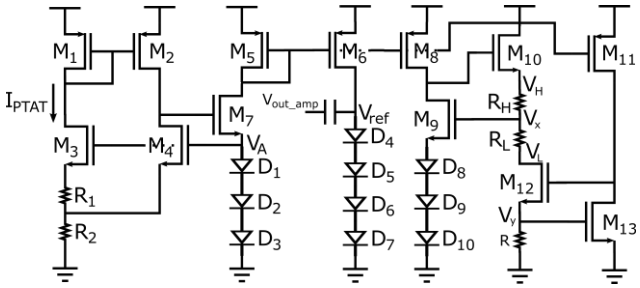

Fig. 11. Schematic of the temperature independent bias generation circuit. All mirrors are 1:1. Diodes are implemented through diode-connected MOSFETs. M_9 and M_{13} have the same dimensions as D_1-D_{10}.

the addition of cascode transistor M_2 to achieve higher gain. Consistently, diode D_3, implemented though a diode connected MOSFET, was also added in the feedback branch to properly bias M_1 and M_2. The frequency response is still given by (6), provided the resistance of D_3 is added in series to the output resistance of the follower $R_{OUTFOLL}$ and $R_o = r_{out1} g_{m2} r_{out2}$, where g_{m2} and r_{out2} are the transconductance and the output resistance of M_2, respectively. To properly bias the gate of M_2, the chain of diodes D_1-D_2, implemented through diode connected MOSFETs, was employed.

It should be noticed that the addition of cascode transistor M_2 is made possible by the previously discussed choice of keeping the supply voltage at 1.2 V. For lower supply voltages the topology in Fig. 4 would probably be the preferred choice.

B. Matching network

In this exploratory design, the matching network has been implemented with a simple off-chip L-shaped *LC* stage, as shown in Fig. 9. Inductance *L* short-circuits to ground the source of transistor M_1 of Figure 8 in DC. The *L* and *C* component values have been chosen based on an estimate of the chip input capacitance, including pads, and inductance, mainly due to the bonding wire.

The matching network provides additional voltage gain, which in the ideal case (lossless network) would be equal to the square root of the ratio between the ED input impedance, Z_{IN}, and 50Ω. Since the ED input impedance is very high, the actual voltage gain is limited by the network Q, mainly determined by the inductor. For instance, assuming Q = 80, it is possible to achieve 18-dB gain.

C. Trigger

The complete transistor-level schematic of the trigger is shown in Fig. 10. It consists of a differential amplifier and two switches (M_H and M_L) driven by the amplifier output voltage V_{out}, which feed either a low (V_L) or a high (V_H) voltage level back to the amplifier input within a bistable loop with positive feedback. The V_H and V_L levels are programmable in order to tailor the noise and disturbance rejection according to the input signal amplitude. M_S and M_R allow to preset the trigger to the desired state at the end of each received message and prepare it for the reception of the following one, i.e. initialize the circuit.

The optimization of V_H and V_L does not require measuring either the input signal or the noise. Instead, a calibration routine, in the prototype implemented by hand, is intended to take place upon node deployment (that is, once the input power has been set by the transmitter output power and the distance between the transmitter and the WUR) and/or at scheduled times. In particular, the calibration criterion is the maximization of the BER or the Packet Error Rate. In [8], a similar threshold calibration loop is implemented: it sets a comparator offset to a level which provides a desired False-Positive Rate.

The main target of the trigger design was to keep its input offset and noise voltage at values that do not limit the overall receiver sensitivity, which is ultimately determined only by the noise of the first stage, i.e. the ED. This goal is not difficult to achieve due to the large gain obtained with the ED. The chosen bias current is I_{bias} = 1 nA. Positive feedback guarantees fast enough switching despite transistors in the first stage having a large area for low offset.

D. Biasing circuit

As mentioned in Section II, the aim of the biasing block is to provide the trigger DC input voltage and thresholds as robustly as possible against process and temperature variations. As shown hereafter, this block requires a non-negligible bias current. In an ultra-low power design, it may be reduced to a current generator with a programmable resistance ladder: while this would certainly reduce the number of branches, thus the consumed current, it would not provide any temperature compensation. If such an approach was chosen, the programmable resistance ladder would have to be recalibrated at every change in the operating temperature. Instead, the architectural choice here is to limit the need for calibration only to the start-up phase, as explained in Section II.E.

The biasing block schematic, reported in Fig. 11, aims at providing V_{ref}, V_H and V_L. All transistors are operated in the subthreshold regime, thus exhibiting an exponential characteristic. The reference voltage generator cell composed of M_1-M_4 and R_1-R_2 [19] is the core of the block, whose output is a fairly temperature-stable V_A. V_A is the gate voltage of M_3 and M_4 and is given by the sum of the PTAT voltage drop on resistance R_2 and of V_{GS4}, which has a negative temperature coefficient instead. V_A is then applied to a chain of diode-connected transistors and the resulting current is copied by M_5-M_6 into the chain of MOSFET diodes D_4-D_7, which have the same dimensions as D_1-D_3, thus the same V_{GS}. Therefore, $V_{ref} \propto V_A$. This allows the generation of a

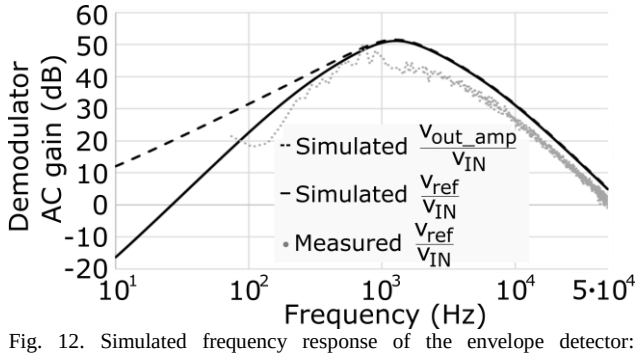

Fig. 12. Simulated frequency response of the envelope detector: v_{out_amp}/v_{IN} (dashed line) and v_{ref}/v_{IN} (solid line). Measured v_{ref}/v_{IN} with nominal envelope detector bias current (grey dots).

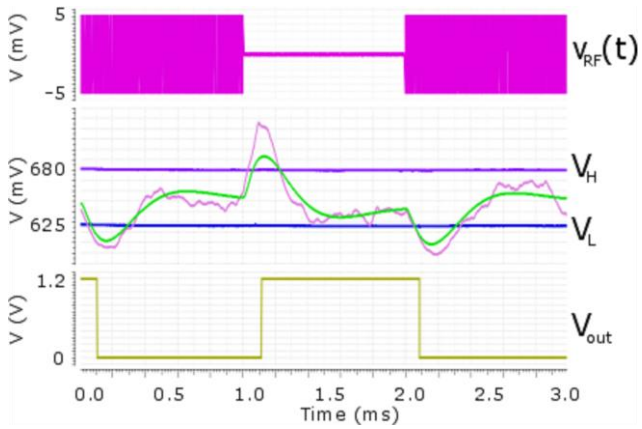

Fig. 13. Transient noise simulation showing a 1-0-1 RF input voltage with a 5 mV amplitude (top, purple trace), trigger thresholds V_H and V_L (middle, violet and blue traces), the amplifier output voltage after the coupling capacitor with and without noise (middle, pink and green traces) and the output voltage of the inverting trigger (bottom, yellow trace).

temperature-compensated input bias voltage V_{ref} for the trigger, which is AC-coupled to the ED output. The same current is also copied by M_8 into M_9 and D_8-D_{10}. Under the assumption that V_{GS9} is roughly equal to the voltage across D_1-D_{10}, voltage $V_x \cong V_{ref}$ is generated as well. This is the case since V_{DS9} is large enough to force M_9 to work in saturation, therefore resulting in the current of M_9 being a function of V_{GS9} only. This is proven right by simulations, as the simulated V_{GS} of the diodes is roughly 97 mV while the simulated V_{GS9} is roughly 95.5 mV at room temperature.

Finally, M_{11} forces into M_{13} the same current which flows in D_1-D_{10}, which, under the assumption that M_{13} is in saturation as well, sets $V_{GS13} = V_y \cong V_{ref}/4$, making it a temperature independent voltage. The local feedback between M_9 and M_{10} and between M_{12} and M_{13} further enforces this condition. V_y is then applied to resistance R, so as to obtain

$$V_H - V_{ref} \cong V_H - V_x = (R_H/R)\, V_y \quad (11)$$
$$V_{ref} - V_L \cong V_x - V_L = (R_L/R)\, V_y \quad (12)$$

Resistor values, in particular R_1=10 MΩ, R_2=17 MΩ, and transistor sizes, in particular $(W/L)_3$ = 104.2 and $(W/L)_4$ = 4.2 and $(W/L)_1$ = $(W/L)_2$, were chosen so as to minimize the dependence of V_A, thus V_{ref}, on temperature as well as to keep

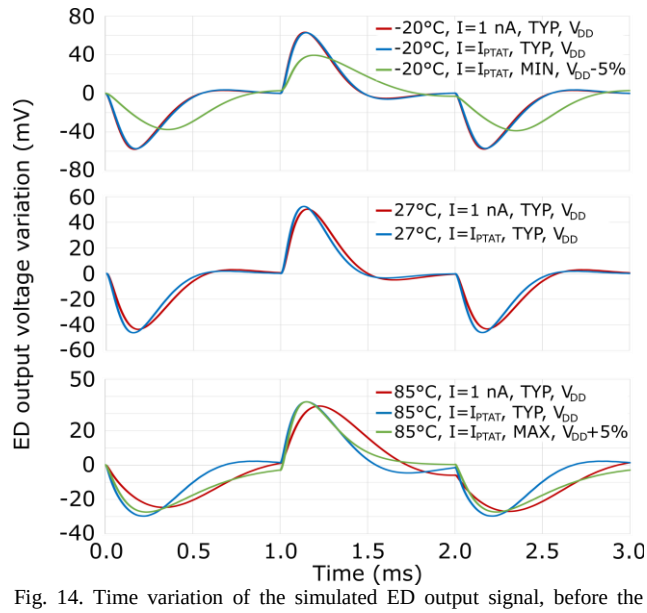

Fig. 14. Time variation of the simulated ED output signal, before the coupling capacitor, with respect to its quiescent value, at different temperatures and using either a constant 1-nA biasing current or a current copied from the PTAT block of the biasing circuit in Fig. 11. The two extreme corners, -20°C/MIN with low supply voltage and 85°C/MAX with high supply voltage, are also included. PTAT and constant biasing currents give almost the same results at room temperature and at -20°C. At 85°C the PTAT is preferable.

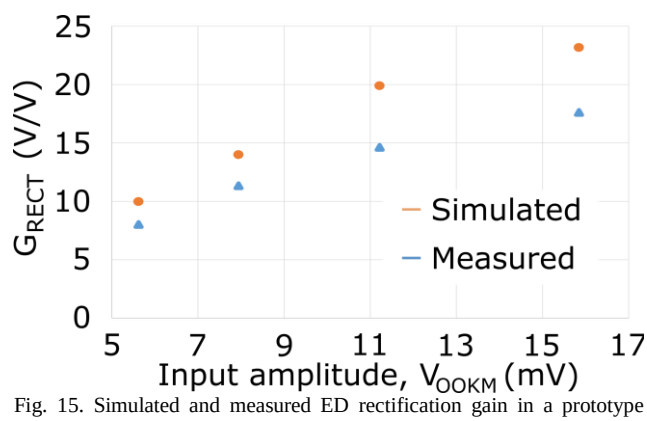

Fig. 15. Simulated and measured ED rectification gain in a prototype without matching network.

the current consumption of the block in the nA range at room temperature, while the number of diodes was selected for $V_{ref} \cong V_{DD}/2$.

This approach has two main drawbacks, i.e. rising consumption with temperature and large resistor area. Consumption increases with temperature because currents rise in most of the branches in the block, in particular currents through M_1 and M_2 rise linearly, through M_5, M_6, M_8, M_{11} rise exponentially and the current though M_{10} follows the dependence on temperature of resistors, i.e. is roughly constant. It should be noticed that the exponential increase of current with temperature is due to the application of a temperature-independent voltage to a chain of diode connected transistors. This problem could be avoided by replacing the diodes with integrated resistors, which however should be very large for nA-power consumption and would require the

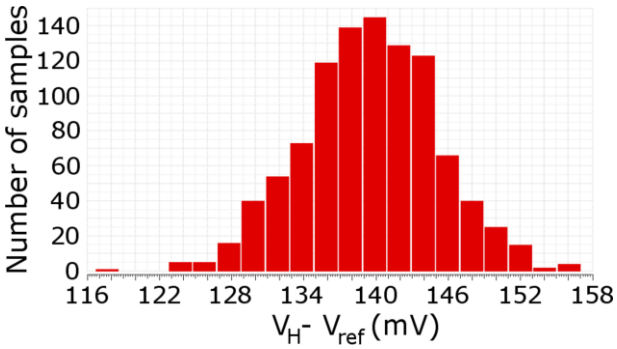

Fig. 16. V_H -V_{ref} in a 1000-run Monte Carlo simulation with the maximum values of R_H.

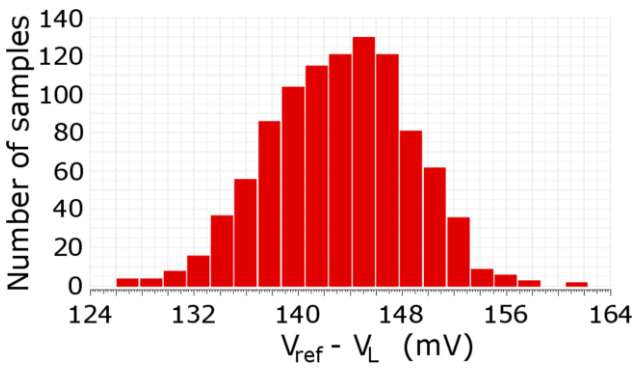

Fig. 17. V_{ref} -V_L in a 1000-run Monte Carlo simulation with the maximum values of R_L.

availability of large resistance-per-square layers, which is not the case in our technology. In our design, resistors with a resistance-per-square $R_{\square}$= 1.3 kΩ are available and resistors R_1 and R_2 alone occupy most of the area of the chip.

IV. Simulated Results

The circuit described in Section III was designed using an STMicroelectronics 90-nm BCD technology. As mentioned in Section II, the standard supply voltage V_{DD} = 1.2 V has been used for all blocks. The target is to detect the envelope edges of a signal with a carrier frequency of 868 MHz and a Manchester coded 0.5 kbit/s OOK modulated bitstream.

The post-layout simulated AC response of the amplifier is shown in Fig. 12, with the output taken both before (v_{out_amp}/v_{IN}, dashed line) and after (v_{ref}/v_{IN}, solid line) the AC coupling capacitance, where v_{out_amp} and v_{ref} are defined in Fig. 11. With a nominal value of I_{bias} = 1 nA and with the follower stage of the ED biased with 5 nA, the simulated integrated output noise power proves to be roughly 200 μV^2. With V_{OOKM} = 5 mV, an ED output pulse amplitude V_{OUTM} ≅ 50 mV is calculated. The corresponding simulated waveforms are reported in Fig. 13, which shows the input RF signal (top), the trigger input voltage (that is, the amplifier output signal after the coupling capacitor) with and without noise together with the set thresholds (center) and the trigger output (bottom). It is apparent that also in the presence of

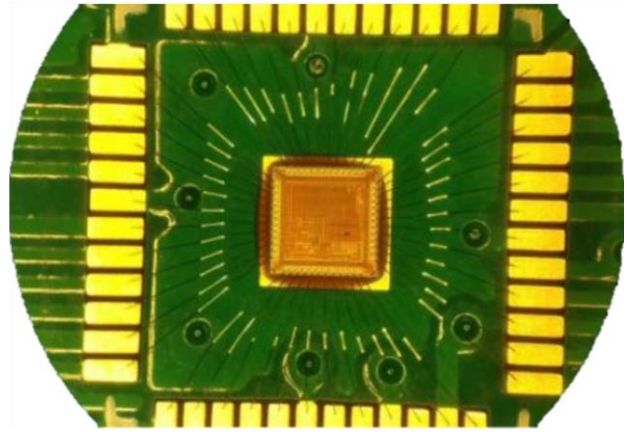

Fig. 18. Micrograph of the circuit prototype.

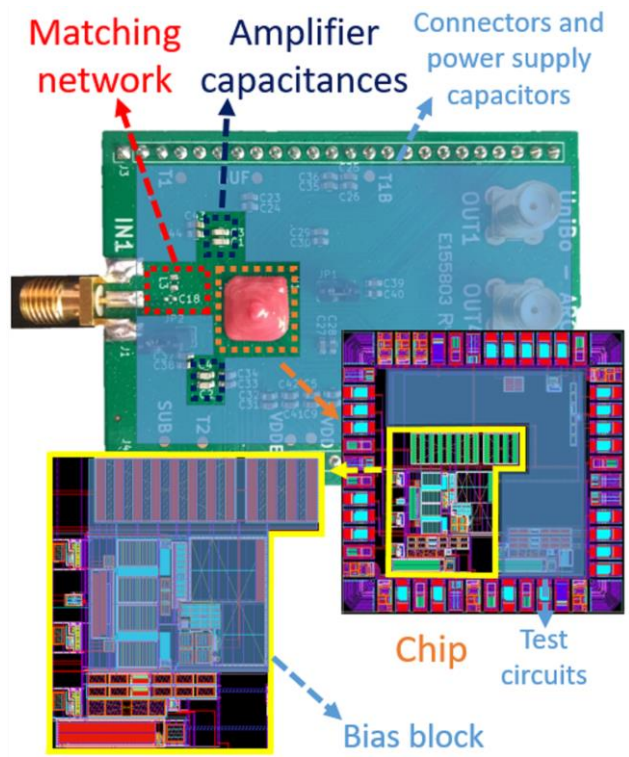

Fig. 19. Top: WUR testing board. Bottom: die layout.

noise the input signal is correctly detected, which gives an estimated sensitivity of 5 mV at the ED input, corresponding to -36 dBm. As an example of the functionality of the ED in process corners, the ED output before the coupling capacitor at -20°C in the MIN corner with low supply voltage and at 85°C in the MAX corner with high supply voltage is shown in Fig. 14. The simulated ED rectification gain, defined as

$$G_{RECT} \equiv \frac{V_{OUTM}}{V_{OOKM}} \propto V_{OOKM}, \qquad (13)$$

from (7), is plotted in Fig. 15. The expected linear dependence of G_{RECT} is verified but gain compression is apparent once the input amplitude is high enough.

Fig. 20. Measured waveforms corresponding to an input sequence of equal (all 0s or 1s) Manchester-coded bits at 0.5 kbit/s rate. From top to bottom:1) modulating input signal gating the RF generator; 2) output of the envelope detector; 3) output of the Schmitt trigger. The horizontal blue lines are the trigger thresholds V_H and V_L. RF signal: 771 MHz frequency, -44 dBm amplitude.

As for the matching network, simulations employing lumped-parameter models of commercial high-Q components at 868 MHz indicate that 18-dB gain can be reached, which leads to a total simulated sensitivity of -54 dBm. With reference to Fig. 9, the estimated values of C_{in}, including parasitics and pads, is roughly 1.6 pF, while the one of the bonding wire inductance is roughly 4 nH. This results in L = 8.7 nH and C = 400 fF.

In order to make the thresholds adaptable to the signal level, R_H and R_L in Fig. 11 are implemented through two resistor chains whose lengths are made programmable with a 5-bit control signal each. In this design, programming is carried out through a Serial-Input Parallel-Output Shift Register which accepts a 10-bit sequence and feeds the bits to the two decoders controlling R_H and R_L in a parallel fashion. This results in the use of only 3 pins, i.e. one for the clock signal, one for the input and one for the output for measurement sessions.

The reference and threshold voltages generated by the bias block are fairly process stable, thanks to proper transistor sizing: Fig. 16 and Fig. 17 show V_H - V_{ref} and V_{ref} - V_L, respectively, corresponding to the maximum values for R_H and R_L obtained with a Monte Carlo simulation with 1000 runs at room temperature. V_H - V_{ref} has a mean value of 139.6 mV and a standard deviation of 5.6 mV, while V_{ref} - V_L has a mean value of 143.2 mV and a standard deviation of 5.4 mV.

As far as power is concerned, bias generators I_{bias} in Fig. 8 and Fig. 10 are copied from the PTAT current flowing through M_1 in Fig. 11. The total currents for the ED, the trigger and the biasing block at room temperature are 8.7 nA, about 2.5 nA and 38 nA, respectively. Conversely, at 85°C the ED consumes 12 nA, the trigger 3.5 nA and the biasing block 360 nA.

V. Prototype and Measurement Results

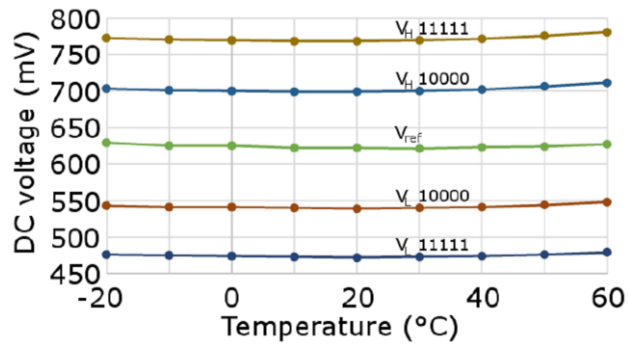

Fig. 21. Measured trigger threshold voltages V_H and V_L for two control bit configurations and input reference voltage V_{ref} vs. temperature generated by the bias circuit of Fig. 11.

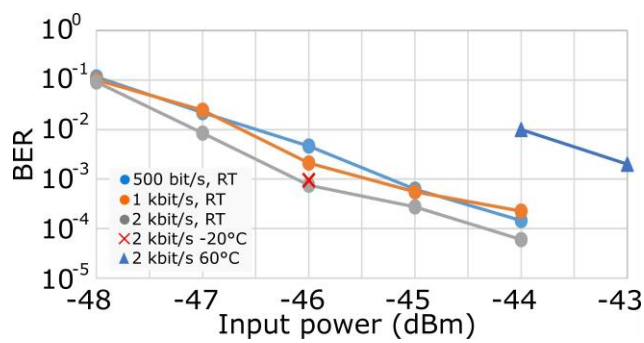

Fig. 22. BER measured for three sequences of randomly generated Manchester coded bits at 0.5, 1 and 2 kbit/s rate at room temperature (RT). Each sequence is composed of 2.5 x 10^5bits. The 2 kbit/s BER at -20°C and +60 °C is also plotted.

Fig. 18 shows the chip photograph, while Fig. 19 illustrates the components on the WUR testing board as well as the chip layout, on which the actual circuit is highlighted. Within the actual circuit, the biasing block is shown in blue. As mentioned in Section III, resistors make up a large amount of the overall circuit area: this is due to the lack of high resistivity components in the chosen technology. The circuit area, excluding the matching network and capacitance C in the ED, is 0.7 mm^2, ~60% of which is occupied by the biasing block. A direct chip-on-board bonding technique has been adopted to minimize parasitics at the RF input. Capacitance C was chosen to be off-chip solely for testing purposes.

As stated in Section III.B, the matching network was designed according to simulations rather than measurements, most likely resulting in inaccuracies in the estimation of the chip input impedance Z_{in} and parasitics. In turn, this caused the gain and center frequency of the LC network not to match the simulated ones, likely along with variability issues.

As far as the matching network is concerned, the actual frequency corresponding to the gain peak has proved to be around 771 MHz. The matching gain is calculated as

$$A_V = \frac{v_{RF,1}}{v_{RF,2}} \tag{14}$$

where $v_{RF,1}$ is the RF input amplitude with a 50-Ω resistance in the place of the matching network, while $v_{RF,2}$ is the RF

TABLE III. PERFORMANCE COMPARISON

	Proposed WUR (simulated)	***Proposed WUR (measured)***	***Roberts [3]***	***Wang [9]***
Temperature range	**-20 ÷ 85°C**	**-20 ÷ 60°C**	-	-
Carrier frequency	**868 MHz**	**771 MHz**	915 MHz	114 MHz
Matching gain	**18 dB**	**12 dB**	12 dB	25 dB
Bitrate	**0.5 kbit/s**	**2 kbit/s**	100 kbit/s	0.3 kbit/s
Sensitivity at 27ºC	**-54 dBm****	**-46 dBm***	-41 dBm*	-65 dBm*
Supply voltage	**1.2 V**	**1.2 V**	1.2 V	0.4 V
Power	**13.4 nW**	**36 nW**	98 nW	3.7 nW
Digital correlator	**no**	**no**	no	yes
Technological node	**90 nm**	**90 nm**	130 nm	180 nm
DTMOS	**no**	**no**	yes	yes
Die area	**0.7 mm^2**	**0.7 mm^2**	0.03 mm^2	1.75 mm^2 (estimated)
External components	**LC**	**LC**	LC	lumped LC + distributed coupling region
FoM_1, eq. (9)	**107.3 dB**	**100 dB**	101.4 dB	117.6 dB
FoM_1 without matching gain	**89.3 dB**	**88 dB**	89.4 dB	92.6 dB
FoM_2 as defined in [9], eq.(10)	**116.2 dB**	**106.9 dB**	106.1 dB	131.7 dB
FoM_2 as defined in [9] without matching gain	**98.2 dB**	**94.9 dB**	94.1 dB	106.7 dB

* Sensitivity defined through 10^{-3} Bit Error Rate (BER)
** Sensitivity estimated assuming 11-dB SNR at the ED output

input amplitude with the matching network between the antenna and the ED input, assuming the signal amplitude at the ED output V_{OUTM} to be equal in the two cases. With this process, a matching gain of 12 dB was found instead of 18 dB.

For easier testing, in the actual prototype the biasing currents for the ED and the trigger, i.e. I_{bias} in Fig. 8 and Fig. 10, are not copied from M_1 of the biasing circuit but provided to the chip through an external generator. Therefore, the testing process was carried out using constant ED and trigger biasing currents instead of the planned PTAT one. As shown in Fig. 14, this leads to results at high temperature slightly worse than expected from simulations.

Sample measured waveforms are reported in Fig. 20. They refer to a sequence of identical Manchester-coded bits at 0.5 kbit/s rate with a 771 MHz, –44 dBm RF signal at room temperature. The curves demonstrate that the input bit sequence is correctly recognized. The reported measurements have been carried out with bias currents in the ED about four times larger than the nominal value, resulting in a total ED current of 28 nA. This current increase has proved necessary to obtain transient responses similar to the ones found with post-layout simulations during the design phase. On the other hand, trigger operation was effective also with a current of 2 nA, therefore no current increase was required. Some discrepancies have also emerged between the expected frequency response and the one measured in nominal bias conditions. This is due to an early access to the 90-nm BCD technology node currently under development, which resulted in a threshold voltage overestimation in the subthreshold region and a capacitive effect underestimation. Fig. 12 shows the AC responses measured by applying an AC signal to the ED input, compared to the simulated ones. The measured ED gain is shown in Fig. 15 along with the simulated one, displaying the same behavior as simulations.

Fig. 21 shows the measured V_H, V_L and V_{ref} over the -20 °C / +60 °C temperature range for two configurations of the control bits. This shows that the threshold margins are well controlled over the entire range. Measurements over 60 °C were not possible due to lack of heat resistant cables.

The BER vs. input RF power measured for 0.5-, 1- and 2-kbit/s Manchester-coded bit streams, each of which is composed of 2.5 x 10^5 randomly generated bits, is plotted in Fig. 22. An ED bias current equal to roughly 4x the nominal value has been used. A 10^{-3} BER is achieved with a -46 dBm RF input power at room temperature and at -20 °C, almost -43 dBm at 60 °C.

VI. DISCUSSION AND COMPARISON WITH PREVIOUS DESIGNS

Table III shows a performance comparison between the proposed design and some previous ones. For the reasons explained in Section II.B, the comparison is limited to designs employing active EDs. In the Table both the simulated and the measured results for the proposed design are presented, due to the discrepancies discussed above concerning the uncertainty in parasitic estimation for the matching network and threshold voltage overestimation in the subthreshold region due to the use of a technology which is currently still under development. In Table III only the currents of the ED and the trigger are considered, thus excluding the biasing block, to make a fair comparison with the other architectures, whose functionality in terms of temperature is unknown. Overall, the proposed architecture achieves performances comparable to the considered prior art, according to simulation results. A deeper insight can be gained by the comparison with the architecture in [9], which is the most similar to the proposed one. The main differences are the presence in the circuit in [9] of a baseband logic, the fact that it is clocked and the ED is LP. It is clear that [9] reaches a better FoM_1 as defined in (9). This is mainly due to a lower carrier frequency, which facilitates a higher matching gain. Indeed, after subtracting the gain of the matching network, the advantage of [9] reduces to roughly 3 dB, as shown in the row entitled "FoM_1 without matching gain". This residual difference must be attributed to

intrinsic architectural differences, the main of which being the presence in our ED topology of the follower branch (M_3 in Fig. 8), which allows the enhancement of robustness and integration, also avoiding complex calibration sessions, but also adds a current consumption of 5 nA. In addition, in [9] Dynamic Threshold MOSFETs are used, which have a higher transconductance but are available only in non-standard technologies, such as Silicon-On-Insulator (SOI) ones.

Table III also shows performances in terms of FoM_2, which, as indicated in (10), also takes the supply voltage into account. While in [9] a 0.4-V supply was used, in the proposed architecture a standard supply voltage of 1.2 V was employed to avoid the need for additional internal or external circuitry to generate lower supply voltages.

In summary, the lack of need for calibration resulted in a 3-dB penalty, as per FoM_1, while the use of a 1.2-V supply corresponds to an additional 5-dB loss, as per FoM_2.

VII. Conclusions

An architecture for the AFE of a WUR was proposed. Provided wake-up events occur rarely enough, the choice of a clockless solution for the AFE simplifies the design of the oscillator, which is still necessary for the baseband logic but is not required to be ultra-low-power. A BP response for the ED allows the integration of the full ED itself, including the capacitance responsible for the first pole. The ED is realized with the aim of avoiding the need for calibration, at the expense of a second branch for correct biasing. An additional network is also proposed, which guarantees temperature independent biasing. A prototype was designed using a standard supply voltage to avoid the need for voltage regulators. The comparison between simulations and prior art using active EDs indicates that the cost for the choices explained above can be estimated in 3 or 6 dBs depending on whether FoM_1 or FoM_2 are considered.

Appendix: Definition of a new Figure of Merit

A Figure of Merit (FoM) was defined based on some assumptions:

- Rectification leverages an exponential characteristic, in particular second-order non-linearities, as shown in (7).
- $g_{m1} \propto I_{bias}$ and $R_o \propto 1/I_{bias}$, therefore $g_{m1}R_o \cong const$ with respect to I_{bias}.
- In-band noise is mostly thermal, i.e. $i_n^2(f) \propto g_{m1}$, therefore the RMS noise voltage at the ED output

$$v_n \propto \sqrt{g_{m1}R_o^2\, BW} = \alpha\sqrt{\frac{BW}{I_{bias}}}, \qquad (15)$$

  where α is a constant.
- The required signal-to-noise ratio SNR_{SEN} at the ED output determines sensitivity

$$V_{OUTM_SEN} = SNR_{SEN}v_n. \qquad (16)$$

Therefore, if V_{OOKM_SEN} is the input RF amplitude which yields V_{OUTM_SEN} at the ED output, we obtain using (7), and (15)

$$V_{OOKM_SEN}^2\, k\,\frac{g_{m1}R_o}{4nV_T} = \alpha SNR_{SEN}\sqrt{\frac{BW}{I_{bias}}}, \qquad (17)$$

where k is a proportionality constant. Eq. (17) shows that $V_{OOK_SEN}^2\sqrt{\frac{I_{bias}}{BW}}$ is an invariant for any ED architecture sharing the above assumptions, making it a suitable figure to compare the performances of different architectures. Obviously, it is desirable for this quantity to be as small as possible, so the FoM can be defined as its inverse:

$$FoM_1(dB) = -P_{SEN}(dBm) + 5\log BW - 5\log I_{bias} \qquad (9)$$

Acknowledgements

Authors would like to thank the ARCES-STMicroelectronics joint lab team in Bologna for their support.

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