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Evaluation of DC-link voltage ripple in five-phase PWM voltage source inverters

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Abstract: This paper presents the analysis of the DC-link voltage switching ripple in five-phase PWM voltage source inverters with balanced load. The analysis is particularly important for the design and selection of a DC-link capacitor making it possible to meet desired electrical performance of the inverter system. Simple and practical equation for designing the DC-link capacitor is proposed relating the value of capacitance to the maximum value (peak-to-peak) of the DC-link voltage ripple. The amplitude of the DC-link voltage switching ripple is analytically derived as a function of modulation index, and the amplitude of the output current and phase angle. In order to show peak-to-peak voltage ripple distribution, different diagrams are introduced. Reference is made to continuous symmetric centred PWM modulation (i.e., space vector modulation SVM). In order to verify proposed developments, simulations have been carried out by Matlab/Simulink considering full range of modulation index and output phase angle.

1 Introduction

In last decades, a large interest has been focused on multiphase variable-speed drives, due to many advantages obtained by joining multiphase motor and multiphase inverter. Compared to their traditional three-phase counterparts, main advantages are reduction of the stator current per phase without increasing the voltage per phase, reduction of the rotor harmonic currents, increased fault tolerance, and higher reliability. Also, multiphase motor drives offer the additional degrees of freedom which can be used for various purposes [1–3].

With the increase of interest in multiphase drives, many carrier-based (CB) and space vector (SV) PWM techniques have been developed for multiphase VSIs, enabling sinusoidal output voltage generation. The carrier-based PWM with common-mode injection, which leads to identical operation as SV PWM technique, is considered as the most practical and suitable control method. Recently, much effort has been directed towards development of SV PWM schemes in case of five-phase VSIs, since five-phase VSI is very common multiphase inverter configuration [4–8]. In general, due to the large number of space vectors, there is a lot of flexibility in choosing the proper combination of space vectors. By combining the utilisation of large and medium length neighbouring space vectors in an appropriate manner, sinusoidal output voltages are obtained without any low-order harmonics [9].

The analysis of the inverter characteristics at the input (DC-link) side is important for the selection of an appropriate DC-link capacitor. Critical performance specifications seem to be DC-link current ripple and voltage ripple since the DC-link capacitor is usually selected according to them. In general, voltage ripple can be significantly reduced by using the large capacitance. On the other side, the size of the DC-link capacitor should be kept as small as possible so high power density of the entire system can be achieved. It is shown in [10] that the input current ripple can be significantly reduced by increasing the phase number from three to five. However, the reduction is not significant when the phase number is more than nine.

In order to achieve an optimum minimisation of the DC-link capacitor, some studies are done and are mostly based on the Fourier analysis (harmonics) and RMS calculations of the input current and voltage characteristics. With reference to three-phase voltage source PWM inverters, the RMS value of the DC-link capacitor current, by using the time domain approach, is calculated in [11, 12]. In [13, 14], the DC-link current spectra is described by a double Fourier series. In [15], the DC-link current and voltage ripple are calculated for inverters and rectifiers in hybrid electric vehicle (HEV) converter/inverter systems, operated by sinusoidal PWM and six-step modulation.

Regarding the five-phase case, the analysis related to the output current ripple peak-to-peak value has been presented in [16], and a detailed experimental verification has been provided in [17]. A similar idea is presented in [18], where the current ripple prediction method for multiphase PWM converters is proposed on the basis of the equivalent single-phase circuit. A study related to the input current and voltage ripple RMS has been reported in [19] for a five-phase VSI. DC current ripple is compared for different modulation techniques and it is shown that it is practically independent of it. However, the voltage ripple envelope and, in particular, the maximum value (peak-to-peak) of voltage ripple has not been examined yet.

A comprehensive analysis of the dc-link voltage ripple has been presented in [20] for single-phase H-bridge PWM inverters, considering both switching frequency and double-fundamental frequency components. Based on the voltage ripple requirements, simple expressions for designing the DC-link capacitor have been proposed. A thorough experimental verification is included in [21]. A similar investigation is done for three-phase PWM VSIs in [22], where the expression of peak-to-peak DC-link voltage ripple amplitude has been derived and different diagrams have been investigated in order to properly design the DC-link capacitor.

Here, the analysis of the DC-link voltage ripple in five-phase PWM voltage source inverter is presented, with the reference to continuous symmetric centred PWM modulation (i.e. SVM). The peak-to-peak DC voltage ripple amplitude is analytically determined over the fundamental period as a function of amplitude and phase angle of the output current, and the modulation index. In order to show the behaviour of the peak-to-peak DC voltage ripple amplitude in the fundamental period for full range of modulation index and output phase angle, the normalised function is considered. Maximum of the peak-to-peak voltage ripple amplitude is determined as a function of modulation index. Based on the analysis of DC-link components, simple and effective analytical expression for calculating the DC-link capacitance is obtained. The simulations are carried out by Matlab/Simulink to identify the effectiveness of the proposed theoretical developments.

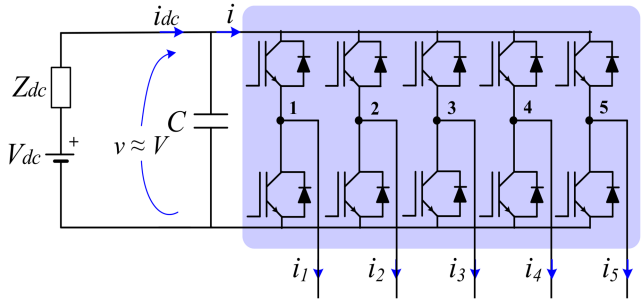

Fig. 1 *Circuit scheme of the considered five-phase VSI*

2 Basic inverter equations

2.1 System configuration

Fig. 1 presents the circuit topology of a five-phase VSI with balanced passive or motor-load. The input DC voltage (V_{dc}) is regarded as being constant. For PWM modulated inverter, by neglecting DC-link voltage oscillations and by considering only linear modulation range ($v \approx V$), the inverter output voltages averaged over the switching period correspond to five-phase sinusoidal reference signals:

$$v_k^* = mV\cos\left(\vartheta - (k-1)\frac{2\pi}{5}\right),\ k = 1, 2, \ldots, 5 \tag{1}$$

where $\vartheta = \omega t$, $\omega = 2\pi/T$ is the fundamental angular frequency, T is the fundamental period and m is the inverter modulation index. The modulation index is defined as a ratio between the desired amplitude of the fundamental output voltage, V_o, and the inverter dc-link voltage, V, i.e. $m = V_o/V$.

Considering sinusoidal PWM output voltages (1), in case of balanced load and neglecting the output current ripple, the corresponding five-phase output currents are assumed sinusoidal as well (2):

$$i_k = I_o\cos\left(\vartheta - (k-1)\frac{2\pi}{5} - \varphi\right), k = 1, 2, \ldots, 5. \tag{2}$$

where I_o is the output current amplitude and φ is the phase angle.

2.2 Inverter input current components

Talking about instantaneous input DC-link current $i(t)$, it can be expressed by three components: DC (average) component $I = I_{dc}$, low-frequency component, and high-frequency (switching frequency, few kHz) component $\Delta i(t)$. In the considered case of balanced load, low-frequency component is zero. Consequently, the inverter input current only contains the DC (average) and the high-frequency component, according to:

$$i(t) = I_{dc} + \Delta i(t)\,. \tag{3}$$

Under the assumption that the inverter is ideal and neglecting its losses, the input current averaged over the switching period T_{sw} can be obtained on the basis of the input/output power balance. Therefore, the averaged input current is given by (4):

$$I_{dc} = \frac{5}{2}mI_0\cos\varphi\,. \tag{4}$$

The input current i is the sum of five bridge leg currents. Each bridge leg current can be calculated from the switching function $S_k = [0,1]$, $k = 1,2,\ldots,5$ (0 upper switch of the leg is OFF, 1 upper switch of the leg is ON), and corresponding output current. Consequently, the input current can be expressed as:

$$i = S_1i_1 + S_2i_2 + S_3i_3 + S_4i_4 + S_5i_5\,. \tag{5}$$

The switching frequency input current component can be finally calculated utilising (3), (4) and (5) as:

$$\Delta i(t) = i - I_{dc} = (S_1i_1 + S_2i_2 + S_3i_3 + S_4i_4 + S_5i_5) - \frac{5}{2}mI_o\cos\varphi\,. \tag{6}$$

Due to the symmetry of the inverter input current waveforms, the analysis can be limited to one-tenth of the fundamental period ($T/10$), i.e. first $\pi/5$ radians.

2.3 Space vector PWM equations

After application of decoupling transformation matrix onto a set of five variables (e.g. leg/phase voltages or currents), the corresponding space vectors are defined. Space vectors are usually represented by projections into two planes (α-β and x-y) and onto one axis (0-axis). This axis represents zero sequence and assuming star connection of the system it cannot be excited [5]. The α-β plane is divided into 10 sectors to find the one that it contains the reference phase voltage space vector. Then, in order to get the sinusoidal output voltages, two large and two medium neighbouring vectors are used to reach the reference in the α-β plane. The voltage references in other planes are set to zero in the linear modulation region.

By using definition of the modulation index, the reference space voltage vectors in each plane can be defined as:

$$\begin{cases} \overline{V}_1^* = \overline{V}_o^* = mVe^{j\vartheta} \\ \overline{V}_3^* = 0. \end{cases} \tag{7}$$

Since the projection of the reference phase voltage space vector forms a circle in the first plane and is zero in the second plane, the switching sequences and the application times are selected in a way to obtain these reference values on average.

The times of application (or the times applied during the modulation period to reach V_o) are calculated for the linear region in every T_{sw}. For the first sector, the times of application of two large and two medium vectors, during one half of the switching period $T_{sw}/2$, can be determined as:

$$t_1 = mT_{sw}K_1\sin(\pi/5 - \vartheta),\ \{10000\} \tag{8}$$

$$t_2 = mT_{sw}K_3\sin\vartheta,\ \{11000\} \tag{9}$$

$$t_3 = mT_{sw}K_3\sin(\pi/5 - \vartheta),\ \{11001\} \tag{10}$$

$$t_4 = mT_{sw}K_1\sin\vartheta,\ \{11101\} \tag{11}$$

$$\begin{aligned} t_0 &= \frac{T_{sw}}{2} - (t_1 + t_2 + t_3 + t_4) \\ &= \frac{T_{sw}}{2}\left[1 - m\left(1 + \cos\frac{\pi}{5}\right)\cos\vartheta - mK_1\sin\vartheta\right]\{11111, 00000\} \end{aligned} \tag{12}$$

being

$$\begin{aligned} K_1 &= \sin\frac{\pi}{5} \cong 0.588 \\ K_3 &= \sin\frac{3\pi}{5} \cong 0.951. \end{aligned} \tag{13}$$

Equations (8)–(13) can be extended to any sector s by replacing the phase angle ϑ by ϑ-$(s$-$1)\pi/5$, $s = 1, 2, \ldots, 10$.

The application time t_0 is equally shared between the two zero voltage vectors, leading to so called 'centred modulation'. The limit of the linear modulation range is $m \le m_{max} \approx 0.526$, where m_{max} is given according to the generalised expression given for k phases, k is odd number $m_{max} = [2\cos(\pi/2k)]^{-1}$.

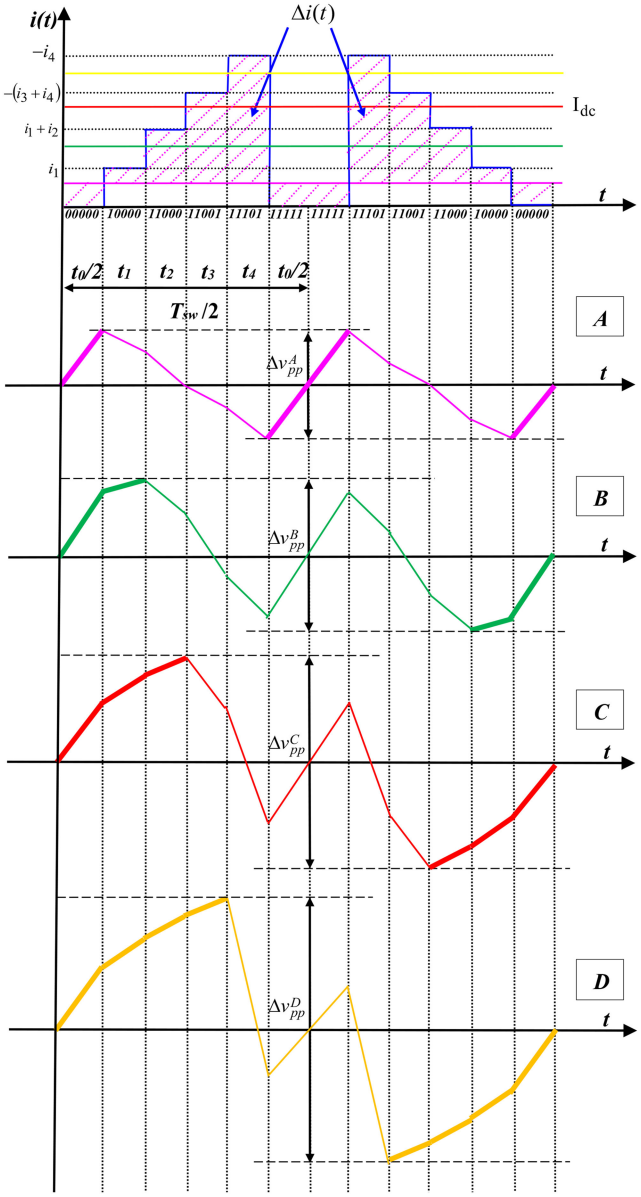

Fig. 2 *DC-link current and voltage ripple in one T_{sw}*
(a) Case A, ***(b)*** Case B, ***(c)*** Case C, ***(d)*** Case D

3 DC-link voltage ripple evaluation

3.1 Dc-link voltage components

As well as the inverter input current, the instantaneous DC-link voltage consists of three relevant components: DC (average) component V, low-frequency component, and high-frequency (switching frequency, few kHz) Δv component. The low-frequency DC-link voltage component is zero in considered case since it is determined on the basis of the corresponding current component. Consequently, the instantaneous DC-link voltage is expressed as:

$$v(t) = V + \Delta v(t)\,. \tag{14}$$

In case of presence of the series DC supply resistance R_{dc}, the average component V is calculated by subtracting the voltage drop on the DC supply resistance R_{dc} from the DC supply voltage V_{dc}, as:

$$V = V_{dc} - R_{dc}I_{dc}\,. \tag{15}$$

The peak-to-peak amplitude Δv_{pp} of the switching frequency DC-link voltage component Δv can be defined as the difference between its maximum and minimum value within a switching period:

$$\Delta v_{pp} = \max\{\Delta v(t)\}_{T_{sw}} - \min\{\Delta v(t)\}_{T_{sw}}\,. \tag{16}$$

Due to the symmetry among the five phases in the considered case of sinusoidal balanced output currents, only the first phase is examined in the following analysis.

3.2 Peak-to-peak voltage ripple evaluation

The peak-to-peak amplitude Δv_{pp} of the switching frequency DC-link voltage component can be evaluated on the basis of the switching frequency current component Δi. Assuming that the capacitive reactance $1/(\omega_{sw}C)$ dominates the equivalent DC source impedance at the switching frequency ($\omega_{sw} = 2\pi f_{sw}$), the whole Δi is circulating through the DC-link capacitor.

The corresponding voltage excursion can be calculated based on the equation for the voltage drop over capacitor by considering the instantaneous input current constant within each application time interval:

$$\Delta v_{pp} = \frac{1}{C}\int_0^{t_{pp}} |\Delta i|\mathrm{d}t\,. \tag{17}$$

The application time intervals are determined by the SV algorithm (8)–(12).

Due to the periodicity of the DC input current $i(t)$ waveforms, the evaluation of the voltage ripple can be reduced to the phase angle range $0 \le \vartheta \le \pi/5$ (the first sector of the space vector diagram). Within the first sector, depending on the value of I_{dc}, four different cases can be distinguished:

– caseA: when $i_1 \ge I_{dc}$
– caseB: when $i_1 \le I_{dc} < i_1 + i_2$
– caseC: when $i_1 + i_2 \le I_{dc} < -(i_3 + i_4)$
– caseD: when $-(i_3 + i_4) \le I_{dc} < -i_4$

The peak-to-peak DC-link voltage variation Δv_{pp} and the instantaneous input current $i(t)$ in one switching period are depicted in Fig. 2, for all aforementioned cases.

(Case A) Evaluation in the range $i_1 \ge I_{dc}$

According to Fig. 2 and considering application interval $t_{pp} = t_0/2$ (bold pink trace), peak-to-peak voltage ripple can be written on the basis of (17) as

$$\Delta v_{pp}^{A} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2}\right) = \frac{1}{C}I_{dc}t_0\,. \tag{18}$$

Introducing (4) and (12) into (18) leads to

$$\Delta v_{pp}^{A} = \frac{5}{4}\frac{I_o T_{sw}}{C} m\cos\varphi\left[1 - m\left(1 + \cos\frac{\pi}{5}\right)\cos\vartheta - mK_1\sin\vartheta\right]. \tag{19}$$

(Case B) Evaluation in the range $i_1 \le I_{dc} < i_1 + i_2$

Considering application interval $t_{pp} = t_0/2 + t_1$ (bold green trace) and conforming to Fig. 2, peak-to-peak voltage ripple can be written on the basis of (17) as

$$\Delta v_{pp}^{B} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2} + (I_{dc} - i_1)t_1\right). \tag{20}$$

Considering (4), (8) and (19) leads to

$$\begin{aligned}\Delta v_{pp}^{B} &= \Delta v_{pp}^{A} + \frac{2}{C}(I_{dc} - i_1)t_1 \\ &= \Delta v_{pp}^{A} + 2\frac{I_0 T_{sw}}{C} mK_1\sin\left(\frac{\pi}{5} - \vartheta\right)\left(\frac{5}{2}m\cos\varphi - \cos(\vartheta - \varphi)\right)\end{aligned} \tag{21}$$

(Case C) Evaluation in the range $i_1 + i_2 \le I_{dc} < -(i_3 + i_4)$

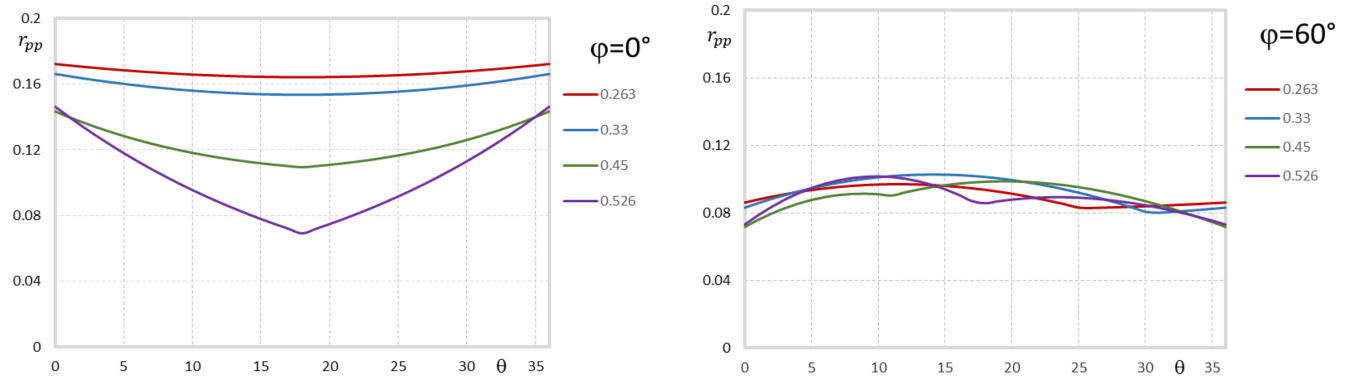

Fig. 3 *Normalised peak-to-peak DC-link voltage ripple amplitude r_{pp} (ϑ) over the period [0, 36°] for different modulation indices, m = 0.263, 0.33, 0.45 and 0.526, and output phase angles φ = 0° and φ = 60°*

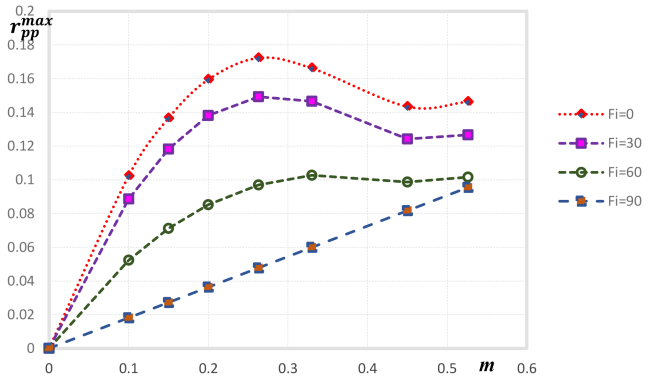

Fig. 4 *Maximum of normalised peak-to-peak voltage ripple amplitude vs. modulation index for φ = 0°, 30°, 60° and 90°*

According to Fig. 2 and considering application interval $t_{pp} = t_0/2 + t_1 + t_2$ (bold red trace), peak-to-peak voltage ripple can be written on the basis of (17) as

$$\Delta v_{pp}^{C} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2} + (I_{dc} - i_1)t_1 + (I_{dc} - (i_1 + i_2))t_2\right). \quad (22)$$

Taking into account (4), (9) and (21), it become (see (23))

(Case D) Evaluation in the range $-(i_3 + i_4) \le I_{dc} < -i_4$

According to Fig. 2 and considering application interval $t_{pp} = t_0/2 + t_1 + t_2 + t_3$ (bold orange trace), peak-to-peak voltage ripple can be written on the basis of (17) as

$$\Delta v_{pp}^{D} = \frac{2}{C}\left(I_{dc}\frac{t_0}{2} + (I_{dc} - i_1)t_1 + (I_{dc} - (i_1 + i_2))t_2 + (I_{dc} + (i_3 + i_4))t_3\right) \quad (24)$$

Considering (4), (10), and (23), peak-to-peak voltage ripple in considered range can be expressed as

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{2}{C}(I_{dc} + i_3 + i_4)t_3 = \Delta v_{pp}^{C} + 2\frac{I_o T_{sw}}{C} m K_3 \sin\left(\frac{\pi}{5} - \vartheta\right) \times \left(\frac{5}{2}m\cos\varphi + \cos\left(\vartheta - \frac{4\pi}{5} - \varphi\right) + \cos\left(\vartheta - \frac{6\pi}{5} - \varphi\right)\right) \quad (25)$$

The actual peak-to-peak DC-link voltage ripple amplitude Δv_{pp} is obtained by merging the results corresponding to these four cases:

$$\Delta v_{pp} = \max\left\{\Delta v_{pp}^{A}, \Delta v_{pp}^{B}, \Delta v_{pp}^{C}, \Delta v_{pp}^{D}\right\}. \quad (26)$$

Finally, from (26), one can see that the magnitude of the DC-link voltage ripple is always determined by the maximum value of those four.

DC-link peak-to-peak voltage ripple amplitude can be normalised according to

$$\Delta v_{pp} = \frac{I_o T_{sw}}{C} r_{pp}(m, \vartheta, \varphi). \quad (27)$$

Applying (27) to four cases A, B, C, and D ((19), (21), (23) and (25), respectively), the normalised peak-to-peak voltage ripple amplitude r_{pp} (m, ϑ, φ) is given by

$$r_{pp} = \max\left\{r_{pp}^{A}, r_{pp}^{B}, r_{pp}^{C}, r_{pp}^{D}\right\}. \quad (28)$$

3.3 Peak-to-peak voltage ripple diagrams

In order to show the behaviour of the peak-to-peak DC voltage ripple amplitude over a fundamental period ϑ = [0, 36°], the normalised function is shown in Fig. 3 for four values of modulation index (0.526 = m_{max}, 0.45, 0.33, 0.263) and two output phase angles (φ = 0 and φ = 60°).

It can be noted that normalised voltage ripple amplitude r_{pp}(ϑ) has different profiles, generally ranging between 0 and 0.18. It has a higher value corresponding to the lower load phase angle, actually the highest value for the unity power factor (φ = 0°), which represents the working condition for the most of grid-connected applications.

The maximum peak-to-peak voltage ripple amplitude $r_{pp}^{max}(\vartheta)$ as a function of modulation index is depicted in Fig. 4 for different output phase angles. In case of φ = 90°, r_{pp}^{max} is determined by properly interpolating data as:

$$r_{pp}^{max}(\varphi = 90°) = 0.18\,m. \quad (29)$$

For the other values of the output phase angles (φ = 0°, 30° and 60°), due to the cumbersome analytical determination, the maximum is not calculated analytically but the following analysis is based on Fig. 4.

4 DC-link capacitor design

If the switching frequency is in the order of kHz, the amplitude of the switching ripple is determined only by the size of the DC-link capacitor. Therefore, the selection and design of the DC-link

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{2}{C}(I_{dc} - i_1 - i_2)t_2 = \Delta v_{pp}^{B} + 2\frac{I_o T_{sw}}{C} m K_3 \sin\vartheta\left(\frac{5}{2}m\cos\varphi - \cos(\vartheta - \varphi) - \cos\left(\vartheta - \frac{2\pi}{5} - \varphi\right)\right) \quad (23)$$

Table 1 Simulation circuit parameters

Label	Description	Parameters
V_{dc}	DC voltage supply	100 V
R_{dc}	DC source resistance	5.5 Ω
L_{dc}	DC source inductance	19 mH
C	DC-link capacitance	1.1 mF
F	Fundamental frequency	50 Hz
f_{sw}	Switching frequency	3 kHz
I_o	Output currents amplitude	4.1 A

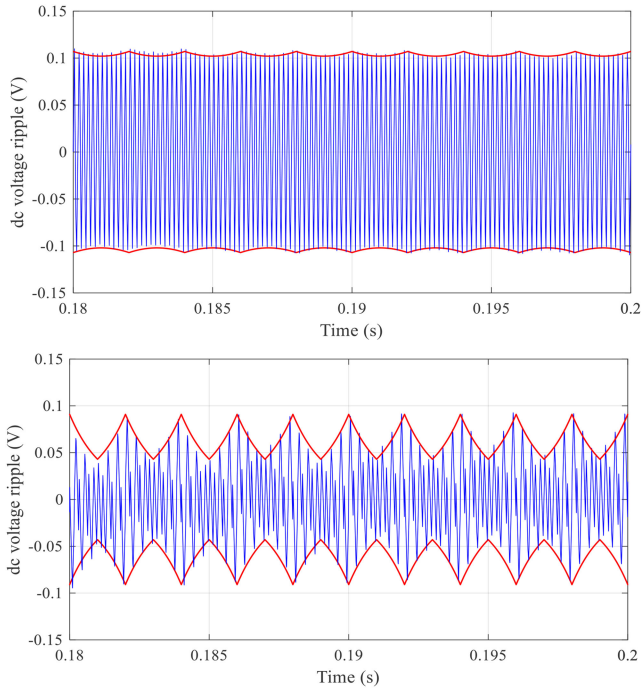

Fig. 5 *DC-link voltage ripple (v_{pp}): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) for $\varphi = 0°$, $m = 0.263$ (upper), $m = 0.526$ (lower)*

capacitor can be performed on the basis of the maximum peak-to-peak voltage ripple amplitude.

Fig. 4 shows that the maximum peak-to-peak voltage ripple amplitude r_{pp}^{max} has the highest value for the unity power factor ($\varphi = 0°$). The following simplification can be introduced:

$$r_{pp}^{max} = 0.1723 \cong \frac{\sqrt{3}}{10} \rightarrow v_{pp}^{max} = \frac{\sqrt{3}}{10}\frac{I_o T_{sw}}{C} \tag{30}$$

The DC-link capacitance can be easily calculated from (30) as

$$C = \frac{\sqrt{3}}{10}\frac{I_o T_{sw}}{v_{pp}^{max}} \tag{31}$$

In case of $\varphi = 90°$, r_{pp}^{max} is directly proportional to the value of modulation index m. In that case, the DC-link capacitor would be oversized if the design is based on (31). Therefore, observing Fig. 4 and considering maximum value of modulation index ($m_{max} = 0.526$), the following simplification can be considered:

$$r_{pp}^{max} = 0.095 \cong \frac{1}{10} \rightarrow v_{pp}^{max} = \frac{1}{10}\frac{I_o T_{sw}}{C} \tag{32}$$

Based on (32), the DC-link capacitance can be calculated as

$$C = \frac{1}{10}\frac{I_o T_{sw}}{v_{pp}^{max}} \tag{33}$$

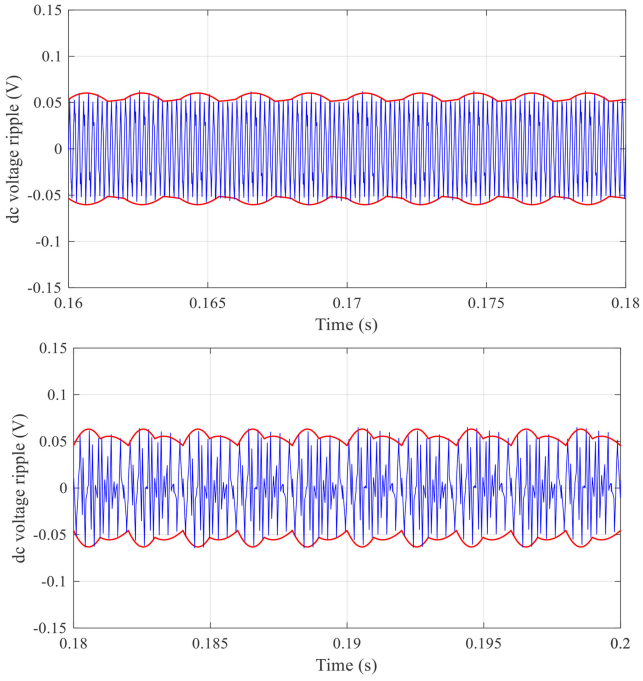

Fig. 6 *DC-link voltage ripple (v_{pp}): simulation results (blue trace) and calculated peak-to-peak envelope (red trace) for $\varphi = 60°$, $m = 0.263$ (upper), $m = 0.526$ (lower)*

5 Numerical results

The analysis of a five-phase inverter, shown in Fig. 1, was verified using Matlab/Simulink. The simulations were carried out considering the parameters given in Table 1. Continues symmetric centred PWM technique is used for VSI control.

The DC-link voltage switching ripple obtained by simulation (blue trace) is shown in Figs. 5 and 6. In the same figures, the corresponding envelopes, calculated based on Section 3, are shown as well (red traces). The envelopes are calculated as one half of the peak-to-peak voltage ripple value. Two cases of the output phase angles $\varphi = 0°$ (Fig. 5) and $\varphi = 60°$ (Fig. 6) are considered for m_{max} and $m_{max}/2$.

Obtained simulation results show good matching with calculated envelopes, for all considered cases in the whole fundamental period.

6 Conclusion

Here, in order to properly design and select the DC-link capacitor, the detailed analysis of the DC-link voltage ripple in five-phase PWM voltage source inverters with balanced load has been carried out.

The amplitude of the DC-link voltage switching ripple is analytically derived as a function of modulation index, and the amplitude of output current and phase angle. Different diagrams are introduced in order to show peak-to-peak voltage ripple distribution as well as its maximum amplitude as a function of modulation index. Based on the maximum peak-to-peak DC-link voltage ripple amplitude, simple and practical equations for designing the DC-link capacitor are proposed.

In order to verify proposed developments, simulations have been carried out by Matlab/Simulnik considering full range of modulation index and output phase angle. The obtained results show a very good agreement.

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