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Theoretical and Experimental Investigation of Switching Ripple in the DC-Link Voltage of Single-Phase H-Bridge PWM Inverters

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Abstract: Direct current (DC)-link voltage ripple analysis is essential for determining harmonic noise and for DC-link capacitor design and selection in single-phase pulse-width modulation (PWM) inverters. This paper provides an extensive theoretical analysis of DC-link voltage ripple for full-bridge (H-bridge) inverters, with simulation and experimental verifications, considering a DC source impedance (non-ideal DC voltage source). The DC voltage ripple amplitude is theoretically estimated as a function of the output current, both amplitude and phase angle, and the modulation index. It consists of a switching frequency component and a double-fundamental frequency component (i.e., 100 Hz), thereby both components are considered in the analysis. In particular, the peak-to-peak distribution, maximum amplitude, and root mean square (RMS) values of the voltage switching ripple over the fundamental period are obtained. Based on the DC voltage requirements, simple and effective guidelines for designing DC-link capacitors are obtained.

Keywords: voltage ripple; H-bridge inverter; pulse-width modulation (PWM)

1. Introduction

The full-bridge (H-bridge) inverter is the basic configuration used for single-phase direct current (DC)/alternating current (AC) power conversion. It can also be easily extended to multiphase and multilevel configurations, obtaining different output voltage levels. The single-phase configuration is used in many low-power applications (i.e., up to 5–10 kW), either grid connected or stand-alone, with special emphasis on the interface of renewable energy sources in distributed generation systems, such as photovoltaic (PV) power plants [1–3]. Since the performance of an inverter mainly depends on its modulation strategy, many carrier-based pulse-width modulation (PWM) techniques have been developed in the last decades [4–6]. The performance is evaluated by the total harmonic distortion (THD) of the input/output voltages and currents, switching losses, and efficiency.

Recently, there has been much work on inverter output voltage and output current characteristics considering PWM techniques. Simple and effective expressions for determining the peak-to-peak output current ripple amplitude over the modulation index range, for two- and multilevel inverters, are presented in [7–9]. An extension to multiphase inverters and a comparison among the cases with different phase numbers is presented in [10]. In [11], the analytical time-averaging approach is applied to a single-phase cascaded multilevel PWM inverter. The current quality is evaluated in the time domain by using the output current ripple normalized mean square (NMS) criterion.

However, a few analyses have been performed on estimating the inverter input (DC-link) characteristics, and in particular the DC voltage. Analyzing the inverter input side is important for DC-link capacitor design and selection in voltage source inverters (VSIs), since it contributes to

the cost, size, and failure rate on a considerable scale. In order to satisfy more stringent reliability constraints, DC-link capacitors face a few challenges. Some of them are reduction of weight and volume, reliability, being exposed to more harsh environments (high ambient temperature, high humidity, etc.) in emerging applications, prevention of overheating, and extension of life time [12,13]. In order to overcome the above challenges, it is necessary to carry out a detailed analysis of DC-link current and voltage ripples.

With reference to three-phase inverters, the developments related to input current and voltage characteristics are usually based on a Fourier analysis (harmonics) and root mean square (RMS) calculations. The RMS value of the DC-link capacitor current in three-phase voltage source PWM inverters is calculated by using the time domain approach in [14,15]. For synthesizing the DC-link current, only the fundamental component of the line current is considered, and the effect of the line current ripple is neglected. The fundamental and ripple line current components are presented together in [16,17]. In all of those papers, a balanced three-phase load is assumed for the DC-link current's analytical calculations. A variety of analytical approaches for the single- and three-phase voltage source inverters determining the DC-link current harmonics for any kind of modulation strategy based on a double Fourier analysis are presented in [18–21].

Generally speaking, the DC-link voltage ripple in single-phase inverters can be expressed considering three different components: the DC (average) component, the low-frequency component (double-fundamental frequency, 100 Hz), and the high-frequency component (switching, many kHz). In the literature, developments are usually focused on one of these components, neglecting the impact of the other two. In many applications, even if the DC supply is an almost ideal voltage source (having small equivalent impedance), only the low-frequency voltage ripple components are negligible, whereas the switching frequency components become relevant in the case of small DC capacitors. The low-frequency voltage ripple components can be relevant in the case of photovoltaic DC supply (high DC series resistance, R) or a DC-link inductive filter (high DC series reactance, ωL), as represented in basic circuit scheme of Figure 1.
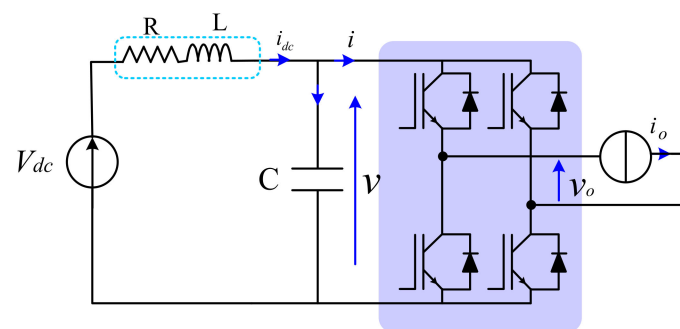

Figure 1. Basic circuit scheme of the single-phase full-bridge (H-bridge) inverter to determine the DC-link voltage ripple.

In [22], the analysis of and calculations for DC-link current and voltage low-frequency ripples under balanced and unbalanced loads for three-phase VSIs are presented. In particular, DC-link average and harmonic RMS currents are calculated, and DC-link voltage ripple under the unbalanced load is obtained considering only the double-fundamental frequency component, but the switching frequency voltage ripple has been examined shortly.

A preliminary theoretical analysis of DC-link voltage ripple, considering both the switching frequency and double-fundamental frequency components, has been presented by the authors in [23], for a single-phase H-bridge PWM inverter. This paper further develops and completes the work [23], also providing a complete set of experimental results taken in different operating conditions. Detailed analytical expressions for the peak-to-peak DC voltage ripple amplitude distribution over the fundamental period are reviewed, together with the maximum peak-to-peak amplitude and RMS

values of the voltage switching ripple component. Comprehensive simulation and experimental tests confirmed the validity of the theoretical developments.

2. Analysis of the Inverter Input Characteristics

2.1. System Configuration

Figure 1 shows the basic circuit scheme of a typical single-phase H-bridge inverter configuration. The inverter is connected to a constant DC voltage supply (V_{dc}) via a DC source impedance consisting of resistance (R) and/or inductance (L). These parameters represent the equivalent series impedance of the DC source. In parallel with the modelled DC source, a DC-link capacitor (C) is connected to smooth the voltage ripple. The load is represented by a sinusoidal AC output current (i_o), meaning the inverter supplies either a passive load or is being connected to the electrical grid with a negligible switching current ripple.

Using the sinusoidal PWM technique, and neglecting the DC-link voltage oscillation compared to its average value ($v \approx V$), the inverter output voltage, averaged over the switching period T_s, is calculated within a linear modulation range as

$$\bar{v}_o \cong v_o^* = m\, V\, \sin(\vartheta),\tag{1}$$

where $\vartheta = \omega t$, ω is the fundamental angular frequency ($\omega = 2\pi/T$), T is the fundamental period, and m is the modulation index ($m = V_o/V$). When the ratio between the fundamental and switching frequency is high enough, the reference signal is considered constant over one switching period. The output voltage and its fundamental component (averaged value) are represented in Figure 2.
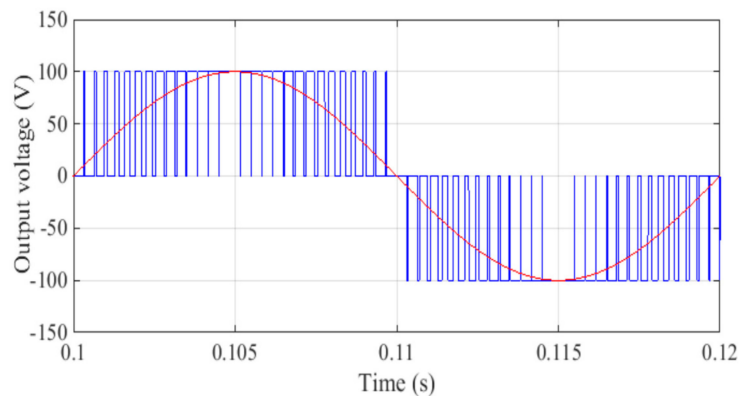
Figure 2. Ideal pulse-width modulation (PWM) inverter output voltage (instantaneous component, blue trace) and its averaged counterpart (fundamental component, red trace) in case of $V_{dc} = 100$ V and $m = 1$.

2.2. Input Current Analysis

Neglecting the switching ripple, the inverter output current is expressed as a sinusoid:

$$i_o = I_o\, \sin(\vartheta - \varphi),\tag{2}$$

being I_o the output current amplitude, and φ its phase angle compared to the voltage.

The instantaneous input current $i(t)$, shown in Figure 3, has three relevant components: DC (average) component I_{dc}, alternating double-fundamental frequency component $\tilde{i}(t)$ (100 Hz), and switching frequency component $\Delta i(t)$:

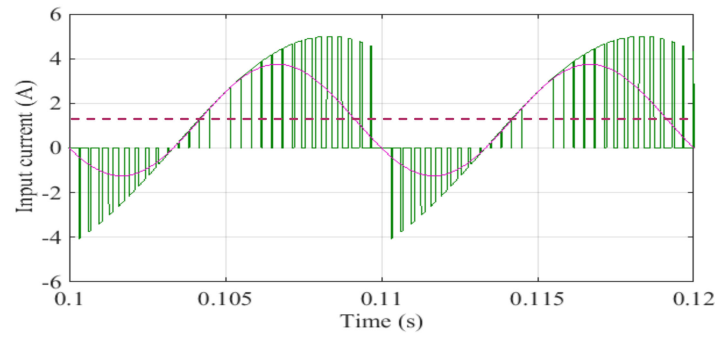$$i(t) = I_{dc} + \tilde{i}(t) + \Delta i(t).\tag{3}$$

Figure 3. Ideal PWM inverter input current (green trace), its averaged counterpart (purple trace), and average component (dashed line) in case of $m = 1$, $I_o = 5$ A (sinusoidal output current, 50 Hz), and $\varphi = 60°$.

The input current averaged over the switching period (T_s), representing the low-frequency input current harmonics, can be expressed as:

$$\bar{i} = I_{dc} + \widetilde{i}. \tag{4}$$

Neglecting the inverter losses, and supposing the inverter input voltage is almost constant and equal to V, the input/output power balance can be written as:

$$V\bar{i} = \bar{v}_o\, i_o. \tag{5}$$

Introducing Equations (1) and (2) in (5), the averaged input current is calculated as:

$$\bar{i} = m\, I_o\, \sin\vartheta\, \sin(\vartheta - \varphi) = \frac{m\, I_o}{2}[\cos\varphi - \cos(2\vartheta - \varphi)]. \tag{6}$$

The average (DC) and the low-frequency input current components (double-fundamental frequency, 100 Hz), can be simply expressed and readily obtained by Equation (6):

$$I_{dc} = \frac{m\, I_o}{2}\cos\varphi \tag{7}$$

$$\widetilde{i} = -\frac{1}{2}m\, I_o\, \cos(2\vartheta - \varphi). \tag{8}$$

According to Equations (3), (4), (6), and (7), the switching frequency input current component is finally calculated as:

$$\Delta i = i - \bar{i} = I_o\, \sin(\vartheta - \varphi)\,(1 - m\, \sin\vartheta). \tag{9}$$

3. Analysis of Input DC-Link Voltage

3.1. Low-Frequency (Averaged) DC-Link Voltage Components

As well as for the current, the instantaneous DC-link voltage consists of three relevant components: DC (average) component V, low-frequency component ($2f = 100$ Hz) $\widetilde{v}$, and switching frequency component Δv:

$$v(t) = V + \widetilde{v}(t) + \Delta v(t). \tag{10}$$

The average component V is calculated by subtracting the voltage drop on the series DC supply resistance R (if any) from the DC supply voltage V_{dc} as:

$$V = V_{dc} - R\, I_{dc}. \tag{11}$$

The low-frequency DC-link voltage component $\tilde{v}$ can be simply calculated on the basis of the amplitude of the low-frequency input current component (8) and the DC-link equivalent impedance Z_{2f}, as follows:

$$\tilde{v} = \frac{m\,I_o}{2}\,Z_{2f}\,\cos\,(2\vartheta - \varphi + \varphi_z),$$ (12)

being Z_{2f} the parallel between the equivalent DC source impedance and the reactance of the DC-link capacitor, both calculated at the double-fundamental frequency $2f$ = 100 Hz:

$$Z_{2f} = \frac{1}{2\,\omega\,C}\sqrt{\frac{R^2 + (2\,\omega\,L)^2}{R^2 + \left(2\,\omega\,L - \frac{1}{2\,\omega\,C}\right)^2}}$$ (13)

$$\varphi_z = \text{arctg}\left[\frac{2\omega L}{R}\left(1 - 4\,\omega^2 L\,C - \frac{R^2 C}{L}\right)\right].$$ (14)

3.2. Switching Frequency DC-Link Voltage Component

A typical instantaneous input current and voltage are depicted in Figure 4 over the switching period T_s. Considering sinusoidal PWM, the "on-time" interval t_{on} can be calculated as:

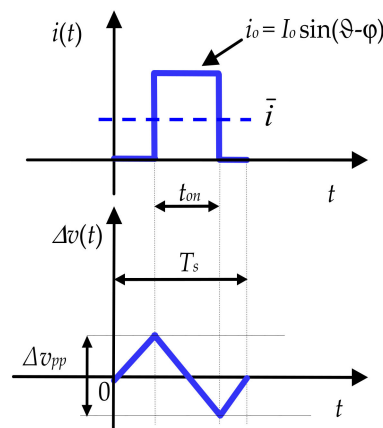$$t_{on} = m\,\sin\vartheta\,T_s.$$ (15)

Figure 4. Instantaneous input current and DC-link voltage over a switching period T_s.

Furthermore, neglecting the variation of the low-frequency DC-link voltage component within the switching period T_s (being the switching frequency much higher than the double-fundamental frequency), the peak-to-peak amplitude of the switching frequency DC-link voltage component can be expressed as follows:

$$\Delta v_{pp} = \max\{\Delta v(t)\}_{T_s} - \min\{\Delta v(t)\}_{T_s}.$$ (16)

In order to obtain the peak-to-peak voltage switching ripple Δv_{pp}, the input current switching frequency component Δi has to be determined.

Assuming that the reactance of the DC-link capacitor $1/\omega_s C$ dominates the DC source impedance at the switching frequency, the DC-link equivalent impedance becomes:

$$Z_{f_s} = \frac{1}{\omega_s\,C}\sqrt{\frac{R^2 + (\omega_s\,L)^2}{R^2 + \left(\omega_s\,L - \frac{1}{\omega_s C}\right)^2}} \cong \frac{1}{\omega_s\,C}.$$ (17)

As a result, the whole switching current component Δi circulates through the DC-link capacitor, and only the capacitance C determines the amplitude of the voltage switching ripple component. Introducing the "on-time" interval t_{on} calculated in (15), the corresponding peak-to-peak switching voltage ripple over the interval (0–t_{on}) is given by:

$$\Delta v_{pp} = \frac{1}{C} \int_0^{t_{on}} \Delta i \, dt. \tag{18}$$

Equations (18), (15), and (9) can be utilized in order to calculate the peak-to-peak amplitude of the DC-link voltage switching ripple:

$$\Delta v_{pp} = \frac{I_o T_s}{C} m \, | \sin \vartheta \, \sin(\vartheta - \varphi)(1 - m \sin \vartheta) \, |. \tag{19}$$

Equation (19) suggests normalization for Δv_{pp}, as follows:

$$\Delta v_{pp} = \frac{I_o T_s}{C} r_{pp}(m, \vartheta, \varphi), \tag{20}$$

being the normalized peak-to-peak voltage switching ripple amplitude $r_{pp}(m, \vartheta, \varphi)$ expressed as:

$$r_{pp}(m, \vartheta, \varphi) = | m \, \sin \vartheta \, \sin(\vartheta - \varphi)(1 - m \sin \vartheta) \, |. \tag{21}$$

3.3. Peak-to-Peak Voltage Ripple Diagrams

Figure 5 shows the distribution of the normalized peak-to-peak voltage switching ripple amplitude calculated by Equation (21) over the half-fundamental period, i.e., $\vartheta = (0, 180°)$. Four modulation indices have been selected in the range $m = (0, 1)$ with the step 0.25. Also, four output phase angles are considered, $\varphi = 0, 30°, 60°$, and $90°$.
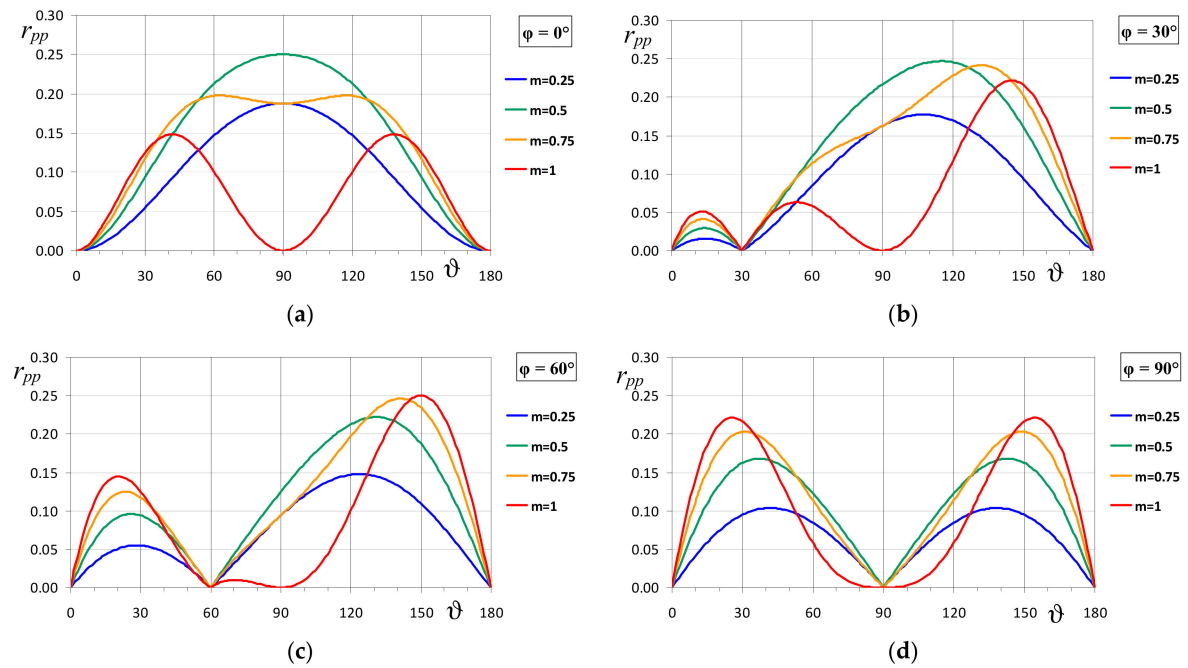

Figure 5. Normalized peak-to-peak DC-link voltage ripple amplitude $r_{pp}(\vartheta)$ in a half-fundamental period $(0, 180°)$ for different modulation indices, $m = 0.25, 0.5, 0.75$, and 1, and output phase angle (**a**) $\varphi = 0°$; (**b**) $\varphi = 30°$; (**c**) $\varphi = 60°$, and (**d**) $\varphi = 90°$.

According to Figure 5, the normalized voltage switching ripple amplitude $r_{pp}(\vartheta)$ varies between 0 (min) and 0.25 (max). In each of those four cases, the $r_{pp}(\vartheta)$ minimum and maximum for different m appear at different angles ϑ over the half-fundamental period.

In the case of a unity output power factor ($\varphi = 0$), as for most of the grid-connected applications, the maximum of the normalized peak-to-peak voltage switching ripple amplitude is obtained from Equation (21), as:

$$r_{pp}^{max}(m, \varphi = 0) = \begin{cases} m(1-m) & \text{for } 0 \leq m \leq \frac{2}{3} \\ \frac{4}{27}\frac{1}{m} & \text{for } \frac{2}{3} \leq m \leq 1 \end{cases}. \tag{22}$$

Figure 6 shows the maximum of the normalized peak-to-peak ripple amplitude r_{pp}^{max} over the whole modulation index range, for $\varphi = 0°, 30°, 60°$, and $90°$. In the case of $\varphi = 0°$, r_{pp}^{max} was analytically determined by Equation (22) (red trace), while for other three cases it was done numerically.
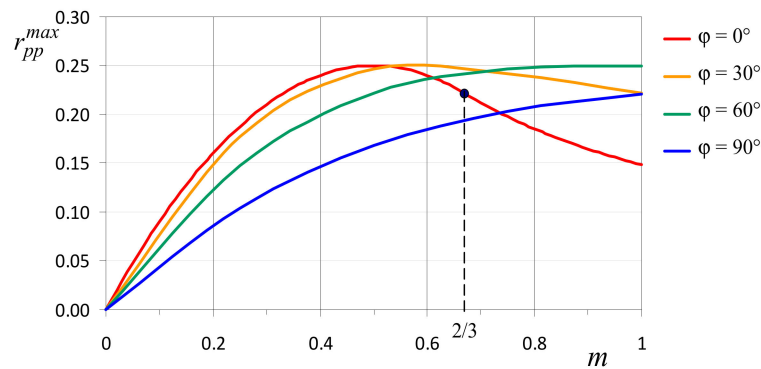

Figure 6. Maximum of normalized peak-to-peak voltage switching ripple amplitude vs. modulation index for different output phase angles $\varphi = 0°, 30°, 60°$, and $90°$.

3.4. RMS of Instantaneous Switching Voltage Ripple

The instantaneous DC-link voltage switching ripple $\Delta v(t)$ is a symmetric triangular waveform with the amplitude corresponding to the half of the peak-to-peak ripple envelope ($\Delta v_{pp}/2$). The RMS value of the triangular signal ΔV_{rms} can be easily determined by dividing its peak value by $\sqrt{3}$. In the case of variable amplitude, the RMS over a (half) fundamental period can be calculated as:

$$\Delta V_{rms} = \sqrt{\frac{1}{\pi}\int_0^\pi \Delta v^2 \, d\vartheta} = \frac{1}{\sqrt{3}}\sqrt{\frac{1}{\pi}\int_0^\pi \left(\frac{1}{2}\Delta v_{pp}\right)^2 d\vartheta}. \tag{23}$$

Introducing Equation (19) into Equation (23), and integrating, yields:

$$\Delta V_{rms} = \frac{I_o}{f_s C}\frac{m}{4\sqrt{3}}\sqrt{\left(\frac{m^2}{2} - \frac{16}{5\pi}m + \frac{1}{2}\right)\cos(2\varphi) + \left(\frac{3}{4}m^2 - \frac{16}{3\pi}m + 1\right)}. \tag{24}$$

Normalizing Equation (24), similarly to Equations (20) and (21), results in:

$$r_{rms}(m, \varphi) = \frac{m}{4\sqrt{3}}\sqrt{\left(\frac{m^2}{2} - \frac{16}{5\pi}m + \frac{1}{2}\right)\cos(2\varphi) + \left(\frac{3}{4}m^2 - \frac{16}{3\pi}m + 1\right)}. \tag{25}$$

Figure 7 shows the normalized DC-link voltage switching ripple RMS given by Equation (25) as a function of the modulation index for different output phase angles φ.
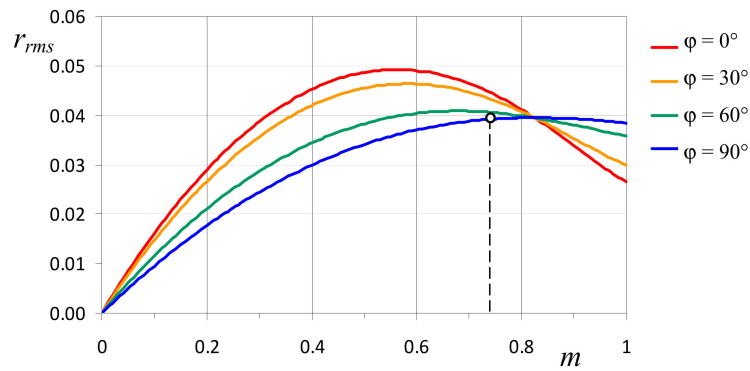
Figure 7. Root-mean-square (RMS) of normalized voltage switching ripple vs. modulation index for different output phase angles $\varphi = 0°, 30°, 60°$, and $90°$.

It can be noted that there is one value of the modulation index when r_{rms} becomes completely independent on the output phase angle φ, and it depends only on m.

By exploiting Equation (25), this specific value of m corresponds to the following condition:

$$\frac{m^2}{2} - \frac{16}{5\pi}m + \frac{1}{2} = 0. \tag{26}$$

Solving Equation (26) results in:

$$m = \frac{16 - \sqrt{256 - 25\pi^2}}{5\pi} = 0.825. \tag{27}$$

Introducing Equation (27) into Equation (25), the corresponding normalized DC-link voltage switching ripple RMS is: $r_{rms}\ (m = 0.825) \cong 0.04$, according to the diagram in Figure 7.

4. Guidelines for Designing the DC-Link Capacitor

Based on the analysis of the DC-link voltage components in Section 3, simple and effective guidelines for designing a DC-link capacitor are proposed in this section. In particular, the DC-link capacitance is calculated taking into account requirements or restrictions referred to in the switching frequency and/or double-fundamental frequency voltage ripple components.

4.1. Capacitor Design Based on Switching Frequency DC-Link Voltage Ripple Requirements

Concerning DC-link voltage ripple at the switching frequency (that is, in the order of kHz), the capacitive reactance $1/\omega_s C$ is certainly much lower than the DC source impedance. So, only the size of the DC-link capacitor is determining the amplitude of this ripple. The selection of the DC-link capacitor can be performed on the basis of one of these constraints: basing on the maximum amplitude of the peak-to-peak switching ripple Δv_{pp}^{max}; or basing on the RMS of the switching ripple ΔV_{rms}.

According to Figure 6, the maximum amplitude of the peak-to-peak ripple is determined as:

$$r_{pp}^{max} \approx \frac{1}{4} \rightarrow \Delta v_{pp}^{max} \cong \frac{1}{4}\frac{I_o T_s}{C}. \tag{28}$$

In this case, the DC-link capacitance can be readily calculated on the basis of Equation (28), also considering the maximum output current I_o^{max}, as:

$$C \cong \frac{1}{4}\frac{I_o^{max}}{f_s\,\Delta v_{pp}^{max}}. \tag{29}$$

Focusing on the voltage switching ripple RMS, a reasonable approximation of ΔV_{rms} for the whole range of the modulation index and output phase angle corresponds to the condition given by Equation (27), i.e., the operating point emphasized in Figure 7:

$$r_{rms} \approx 0.04 = \frac{1}{25} \rightarrow \Delta V_{rms} \cong \frac{1}{25} \frac{I_o T_s}{C}. \tag{30}$$

Given as conditions the RMS of the switching ripple and the maximum output current $I_o^{\max}$, by Equation (30), the DC-link capacitor can be sized as:

$$C \cong \frac{1}{25} \frac{I_o^{\max}}{f_s \, \Delta V_{rms}}. \tag{31}$$

4.2. Capacitor Design Based on Double-Fundamental Frequency DC-Link Voltage Ripple Requirements

Concerning the low-frequency DC-link voltage ripple, i.e., double the fundamental frequency, its amplitude $\widetilde{V}$ generally depends not only on the capacitance C, but also on the parameters of the DC-link impedance Z_{2f}. According to Equations (12) and (13), and taking into account the previous assumption, the DC-link voltage ripple amplitude (100 Hz) is calculated as:

$$\widetilde{V} = \frac{m \, I_o}{2} \frac{1}{2 \, \omega \, C} \sqrt{\frac{R^2 + (2 \, \omega \, L)^2}{R^2 + \left(2 \, \omega \, L - \frac{1}{2 \, \omega \, C}\right)^2}}. \tag{32}$$

While the solution given by Equation (32) could be adopted to design the DC-link's capacitance, it is a rather cumbersome calculation. A reasonable simplification can be introduced if one of the following assumptions can be made:

$$\begin{cases} 2 \, \omega \, L >> \frac{1}{2 \, \omega \, C} & inductively \, dominant \, dc-link; \\ R >> \frac{1}{2 \, \omega \, C}, \, 2 \, \omega L & resistively \, dominant \, dc-link. \end{cases} \tag{33}$$

Assuming that one of two assumptions in Equation (33) is satisfied, i.e., a photovoltaic DC supply having a high equivalent series resistance R (around the maximum power point (MPP) is $R_{PV} = V_{mpp}/I_{mpp}$), or a DC-link inductive filter having a high series reactance $2 \, \omega L$, the double-fundamental frequency DC-link voltage ripple $\widetilde{V}$ can be calculated by simplifying Equation (32) as:

$$\widetilde{V} \cong \frac{m \, I_o}{2} \frac{1}{2 \omega C}. \tag{34}$$

Finally, given $\widetilde{V}$ and the maximum output current $I_o^{\max}$ as a condition, the DC-link capacitor can be sized by reversing Equation (34):

$$C \cong \frac{m \, I_o^{\max}}{2} \frac{1}{2 \, \omega \widetilde{V}}. \tag{35}$$

4.3. Discussion

Generally speaking, the design of the capacitor C based on (35) (double-fundamental frequency) gives higher values compared to the value obtained by (29) or (31) (switching frequency), if comparable voltage ripple amplitude restrictions are set. On the other hand, considering the same capacitor as in the real circuit, the ratio between the two ripple amplitudes is practically given by the inverse ratio between the corresponding frequencies, which could be in the range 20–200, making the voltage switching ripple obviously much smaller than the voltage double-fundamental ripple.

However, the voltage switching ripple amplitude could have additional specific restrictions to limit switching noise, electromagnetic interferences, and voltage stress on the DC bus components. In this case, the capacitor could be oversized considering (29) or (31), compared to the use of (35).

It should be noted that there are specific cases in which the voltage switching ripple amplitude exceeds the double-fundamental ripple amplitude. In particular, this could occur if condition (33) is not satisfied, i.e., in the case of small DC source impedance at the double-fundamental frequency. This is the case for an almost ideal DC source, in which the double-fundamental frequency ripple practically disappears, and the voltage switching ripple can be evaluated by (28) or (30).

5. Numerical Results

In order to verify the results obtained by the analytical developments, MATLAB/Simulink simulations have been carried out for the H-bridge single-phase inverter topology (Figure 1) controlled by the sinusoidal PWM. The input terminals of the inverter are connected to the DC voltage supply with an air-core inductor (*RL*) DC-source impedance. Table 1 summarizes the circuit parameters and components used in the simulations. The output current has been approximated as a unity sinusoid (switching ripple free), so the output phase angle φ can be treated as a degree of freedom. The other simulation circuit parameters are set in the mind to match the corresponding experimental circuit parameters adopted in the following Section 6.

Table 1. Circuit parameters.

Label	Description	Parameters
V_{dc}	DC voltage supply	96 V
R	DC source resistance	5.4 Ω
L	DC source inductance	19 mH
C	DC-link capacitance	1.1 mF
f_S	Switching frequency	2.5 kHz
I_o	Sinusoidal output current amplitude	1 A
f	Fundamental frequency	50 Hz

In Figures 8 and 9, the instantaneous DC-link voltage switching ripple $\Delta v(t)$ (blue traces) is compared with the half peak-to-peak voltage ripple envelope $\pm \Delta v_{pp}/2$ calculated by Equation (19) (red traces), over one fundamental period (T = 20 ms). Two different output phase angles φ = 0° (Figure 8) and φ = 60° (Figure 9) are considered, and the four sub-cases (a–d) correspond to different modulation indexes *m*: 0.25, 0.5, 0.75, and 1.
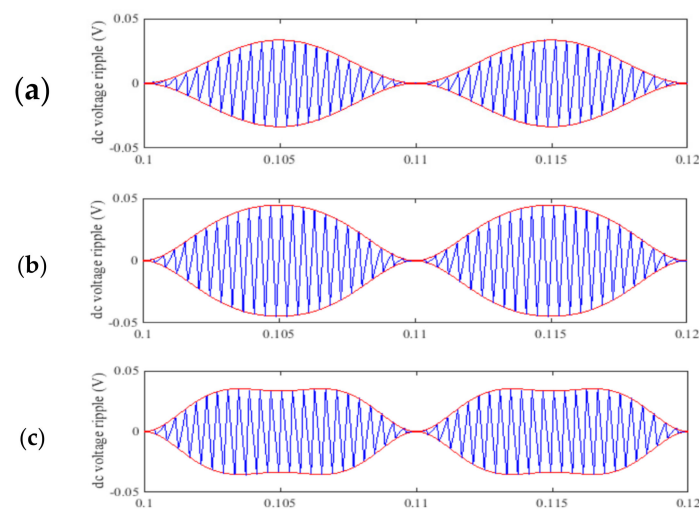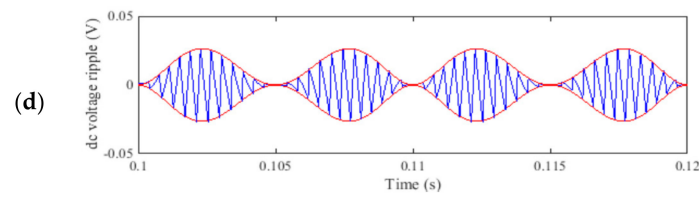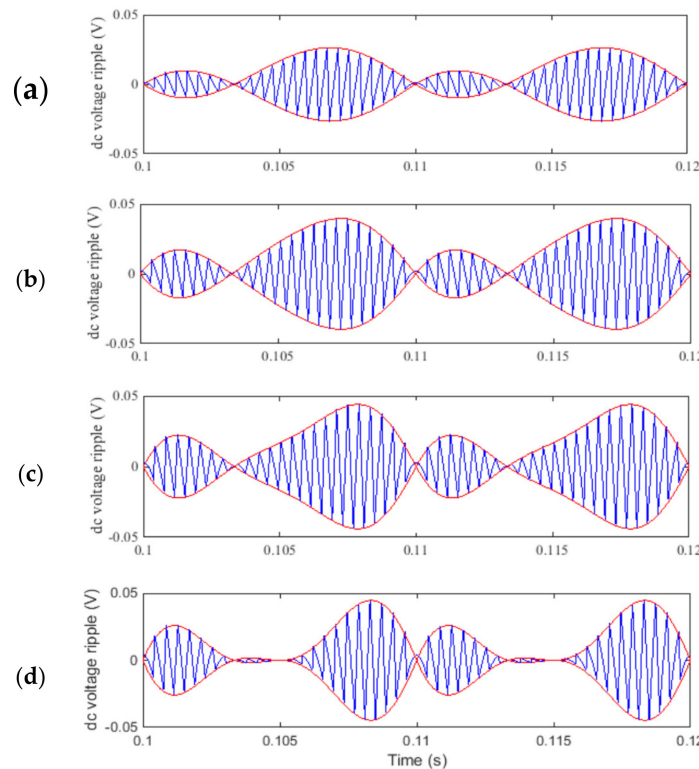

Figure 8. *Cont.*

Figure 8. DC-link voltage switching ripple: simulation results (blue trace) and theoretical peak-to-peak envelope (red trace) over a fundamental period for $\varphi = 0°$, (**a**) $m = 0.25$; (**b**) $m = 0.5$; (**c**) $m = 0.75$; and (**d**) $m = 1$.

Figure 9. DC-link voltage switching ripple: simulation results (blue trace) and theoretical peak-to-peak envelope (red trace) over a fundamental period for $\varphi = 60°$, (**a**) $m = 0.25$; (**b**) $m = 0.5$; (**c**) $m = 0.75$; and (**d**) $m = 1$.

Note that the switching ripple $\Delta v(t)$ has been numerically obtained by properly high-pass filtering the instantaneous DC-link voltage, according to Equation (10).

According to the Figures 8 and 9, numerical simulations perfectly match the theoretical DC-link voltage switching ripple amplitude in all of the considered cases, proving the effectiveness of the proposed analytical developments.

6. Experimental Results

Experimental verifications have been carried out in order to prove the theoretical developments and numerical results presented in previous sections. Two different kinds of load are considered in order to obtain two different output phase angles $\varphi = 0°$ and $\varphi = 60°$. Tables 2 and 3 summarize the main parameters of experimental setup and circuit load, respectively.

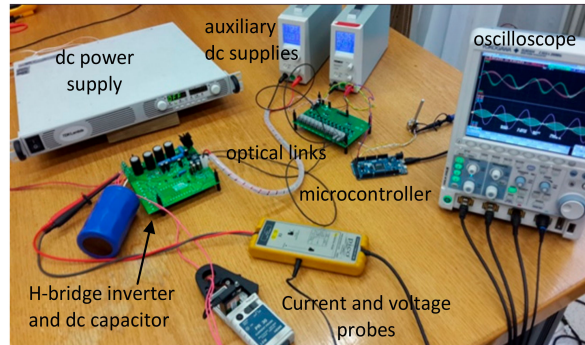**Table 2.** Experimental setup parameters.

Label	Description	Parameters
V_{dc}	DC voltage supply	96 V
R	DC source resistance	5.5 Ω
L	DC source inductance	19 mH
C	DC-link capacitance	1.1 mF
f_S	Switching frequency	2.5 kHz
f	Fundamental frequency	50 Hz

Table 3. Load parameters.

Load	$\varphi = 0°$	$\varphi = 60°$
R_L	4.7 Ω	13.9 Ω
L_L	43.3 mH	76.4 mH
R_o	29.7 Ω	0
C_o	43.3 μF	0

A picture of the whole lab setup is presented in Figure 10. It consists of a Mitsubishi power IGBT module IPM PS22A76 (1200 V, 25 A, Mitsubishi Electric Corporation, Tokyo, Japan), an "Arduino DUE" microcontroller board (84 MHz Atmel, SAM3X83 Cortex-M3 CPU, Somerville, MA, USA), and a Yokogawa DLM 2024 oscilloscope (Yokogawa Electric Corporation, Tokyo, Japan) with the PICO TA057 differential voltage probe (25 MHz, ±1400 V, ±2%, Pico Technology, Tyler, TX, USA) and LEM PR30 current probe (dc to 20 kHz, ±20 A, ±1%, LEM Europe GmbH, Fribourg, Switzerland). Additionally, not included in Figure 10, an air-core inductor (*RL*) is adopted as a DC-source impedance in series with the DC power supply.

Figure 10. Experimental setup.

In Figure 11 the electrical circuit scheme of the load is presented. The corresponding load parameters presented in Table 3 have been determined by the LCR meter Agilent 4263B.
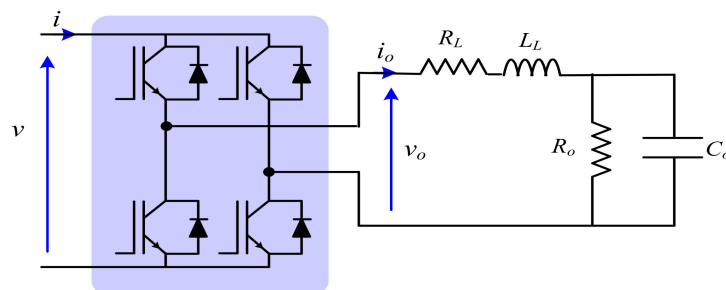
Figure 11. Load configuration for the experimental setup.

As a first experimental verification, the load voltage and current, and the DC-link voltage were measured. In Figure 12, the aforesaid variables are presented for the case $m = 0.75$ and $\varphi = 0°$, over five fundamental periods ($5T = 100$ ms). The top part of the oscilloscope screenshot presents the load voltage and current, the middle part presents the DC-link voltage, and the bottom part presents one zoomed part of the DC-link voltage emphasizing the presence of 100 Hz and switching ripple components. The zoomed part of the DC bus voltage is marked with the rectangle in the middle part of the screenshot, showing five periods of the 100 Hz components.
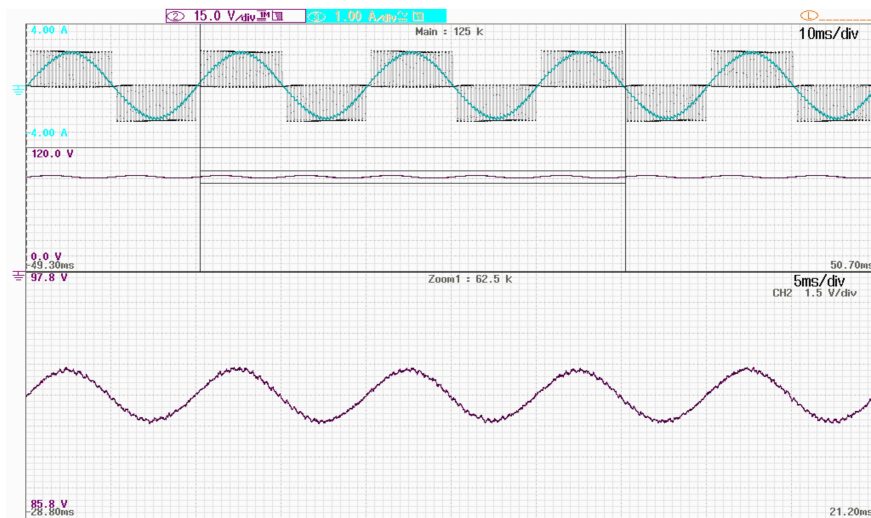

Figure 12. Output load voltage and current: upper part, dc-link voltage: middle part, and zoomed DC-link ripple components: lower part, for $m = 0.75$ and $\varphi = 0°$.

In Figures 13 and 14, experimental verifications were carried out considering four different values of the modulation index $m = 0.25, 0.5, 0.75,$ and 1, for the case of output phase angles $\varphi = 0°$ and $\varphi = 60°$, respectively. In both figures, there are five traces displayed over one fundamental period: top traces present the load voltage and corresponding load current; a violet trace presents the DC-link voltage switching ripple. The two blue traces present the two half envelopes of the mentioned ripple ($\pm\Delta v_{pp}/2$), obtained by implementing Equation (19) in the microcontroller board and sending to an output digital-to-analog converter (DAC) channel, with a proper scale factor.
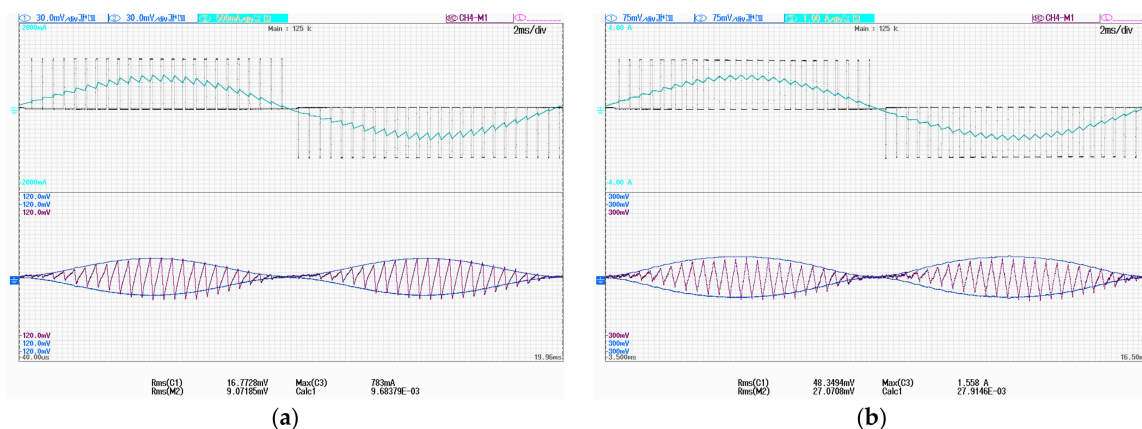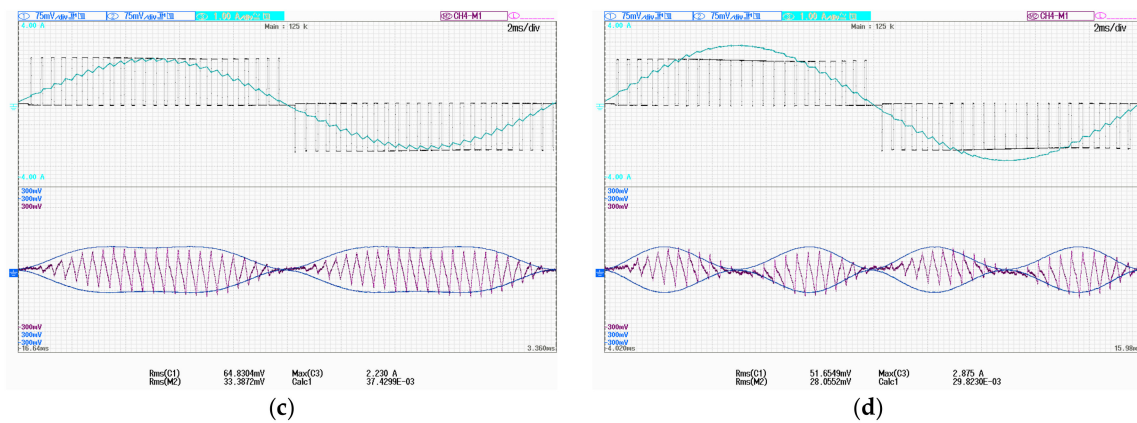

(a)

(b)

Figure 13. *Cont.*

Figure 13. Experimental results for $\varphi = 0°$: upper half, output voltage and current; lower half, analytically calculated envelope and measured DC voltage switching ripple. (**a**) $m = 0.25$; (**b**) $m = 0.50$; (**c**) $m = 0.75$; (**d**) $m = 1$.

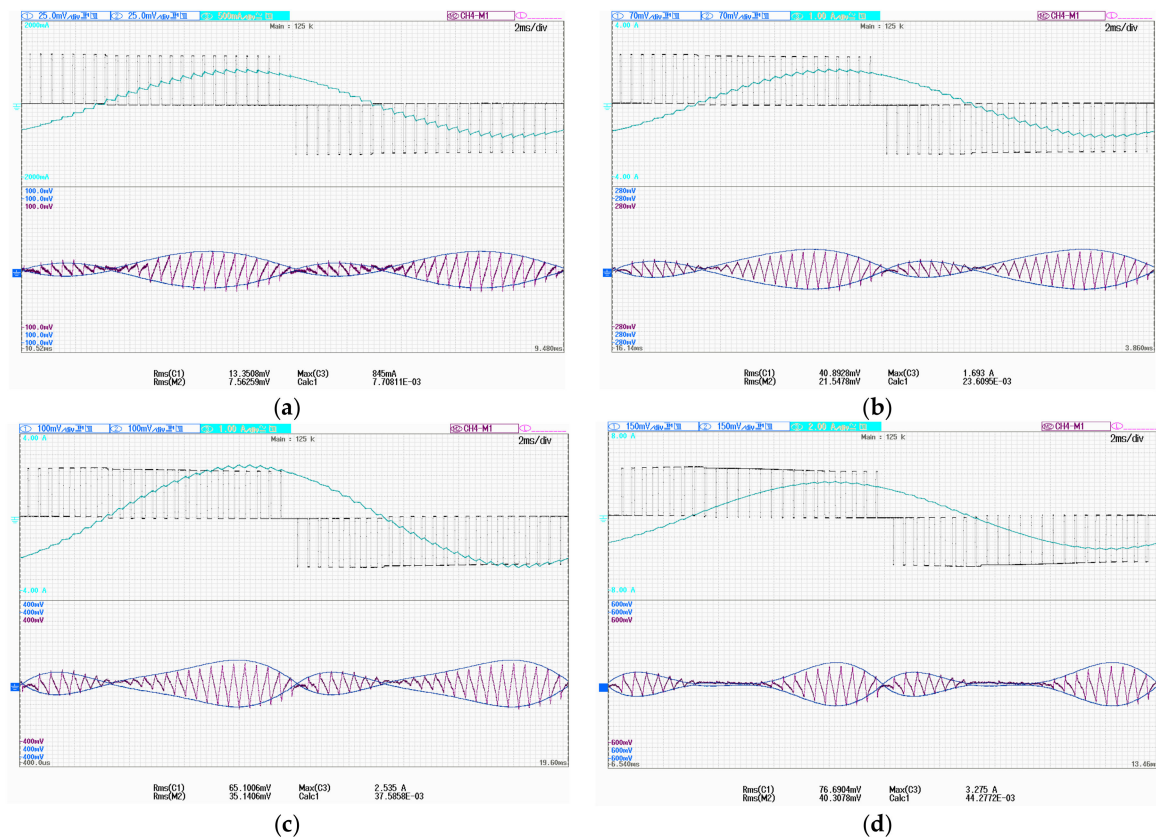**Figure 14.** Experimental results for $\varphi = 60°$: upper half, output voltage and current; lower half, analytically calculated envelope and measured DC voltage switching ripple. (**a**) $m = 0.25$; (**b**) $m = 0.50$; (**c**) $m = 0.75$; (**d**) $m = 1$.

Similarly to the simulations, the switching ripple component of the DC-link voltage has been obtained by filtering the instantaneous DC-voltage using the built-in math functions of the scope.

As it can be noticed, the experimental voltage ripples match the theoretical envelopes in a very satisfactory way for all the considered cases, both in the amplitude and the shape, confirming the effectiveness of the proposed analytical developments given by Equation (19).

The RMS of the envelope (Rms(C1)), maximum value of the output current (Max(C3)), RMS of the ripple (Rms(M2)), and RMS of the envelope divided by sqrt(3) (Calc1) are presented at the bottom of Figures 13 and 14.

Table 4 summarizes the analytical, numerical, and experimental RMS values of the DC-link voltage switching ripple (ΔV_{rms}) for the considered cases. The matching is generally satisfying within the expected resolution and considering the non-idealities of the experimental implementation.

Table 4. Summarizes the analytical (Theory), numerical (Sim.), and experimental (Exp.) RMS values of the DC-link.

m	Load Angle $\varphi = 0°$			Load Angle $\varphi = 60°$		
	Theory	*Sim.*	*Exp.*	*Theory*	*Sim.*	*Exp.*
0.25	9.7	9.6	9.1	7.8	7.8	7.7
0.5	27.5	26.8	27.1	23.6	23.6	21.6
0.75	37.4	35.6	33.4	37.5	37.5	35.1
1.00	29.9	28.7	28.1	44.23	44.3	40.3

7. Conclusions

An analysis, detailed calculations, and experimental verifications of the instantaneous DC-link voltage ripple in single-phase H-bridge PWM inverters have been carried out and presented in this paper, considering both the double-fundamental frequency component and the switching frequency component, and taking into account different types of DC source impedances.

In particular, the expression of the peak-to-peak voltage switching ripple amplitude was derived over the whole fundamental period as a function of the modulation index *m* and the output current phase angle φ. The normalized voltage switching ripple amplitude was introduced, and different diagrams were investigated. The maximum of the peak-to-peak amplitude and the RMS of the DC-link voltage switching ripple were determined, leading to simple and effective guidelines for designing a DC-link capacitor based on voltage ripple requirements.

The analytical developments have been experimentally verified using two different kinds of custom-made load, corresponding to φ = 0° (as for most of the grid-connected inverters) and φ = 60° (typical inductive load), and four modulation indexes to cover the whole modulation range. The RMS values of the switching ripple were calculated in real time using the advanced oscilloscope function and displayed together with the corresponding waveforms. For all considered cases, the theoretical and experimental results showed a satisfactory matching. All in all, the effectiveness and correctness of the developments have been successfully proven. The proposed methodology could be extended to different DC/AC conversion topologies, such as multilevel and multiphase inverters.

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