P-GaN Gate HEMTs: A Solution to Improve the High-Temperature Gate Lifetime

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***Abstract*— In this letter, we report an approach to improve the forward bias gate reliability of Schottky gate p-GaN HEMTs. In particular, a gate layout solution, namely Gate Within Active Area (GWA), aimed at improving the high-temperature time to failure (TTF), is proposed and validated. This solution allows to avoid the exposure of the gate finger (p-GaN/metal) to the nitrogen-implantation needed for termination and isolation purposes. GWA devices feature a significantly improved gate reliability at high temperature with respect to the reference ones, under both DC and pulsed stress tests. Finally, it is demonstrated that the Schottky gate p-GaN HEMTs show a positive temperature-dependent gate TTF in a range up to 150 °C, confirming the crucial role of impact ionization on the gate failure.**

***Index Terms*— Gallium nitride, HEMTs, reliability, Schottky gate, breakdown, time to failure, gate layout.**

I. Introduction

THANKS to superior properties with respect to silicon (Si) and silicon carbide (SiC) competitors, including larger bandgap, higher critical electric field and electron mobility, gallium nitride (GaN) high-electron mobility transistors (HEMTs) are experiencing rapid adoption in several power electronics applications, such as power supplies, fast chargers, data centers and Lidar systems [1], [2], [3], [4]. The smaller intrinsic capacitances and lack of an intrinsic body diode make GaN HEMTs unrivaled in terms of switching speed, enabling lighter, smaller, and more efficient power applications [5].

However, while GaN transistors are currently being exploited in different applications, further improvements regarding the stability, reliability and robustness are still possible [5]. For instance, the GaN HEMT with a Schottky metal/p-GaN gate (SP-HEMTs), a commercialized enhancement-mode solution, faces limitations in gate voltage swing compared to Si and SiC counterparts, making it more vulnerable to possible voltage ringing present in a circuit, increasing the complexity of the driver circuit, and thus only partially exploiting its potential. Therefore, an extensive effort is devoted to this topic [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], first seeking the most suitable test method, then understanding the mechanisms limiting the gate reliability, finally proposing solutions to increase the maximum gate voltage, currently limited to 6 V in commercialized SP-HEMTs.

Constant-voltage stress (CVS) or step-voltage stress tests have been widely adopted in [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], and [19], showing a gate time-dependent dielectric breakdown behavior with a Weibull distributed cumulative probability function (F) and a shape parameter (β) higher than 1, suggesting wear-out failure. Specific analyses were performed in [22], [23], [24], [25], [26], and [27] by adopting square-wave pulsed stress tests. In [22], a frequency-dependent gate failure analysis, up to 100 kHz, showed a weak frequency dependency of the gate mean TTF. On the contrary, by exploring higher switching frequencies, up to 3 MHz, the gate lifetime was found to decrease by increasing frequency and duty cycle [25], [27], due to the electrostatic behavior of the semi-floating p-GaN layer, determined by the related time-dependent charging and discharging processes.

Different gate process and geometry solutions have been proposed to enhance gate lifetime. In [13], [16], and [30], a correlation between gate TTF and magnesium (Mg) concentration in the p-GaN layer has been reported, i.e. the lower Mg concentration, the longer gate TTF. The role of the AlGaN barrier has been investigated in [13], revealing a longer gate TTF by reducing the aluminum content (Al%), and identifying an optimum barrier thickness at a given Al%. In [14], the gate lifetime has been improved by depositing an additional 30-nm n-GaN layer with a Si-doping concentration of 10^{19} cm^{-3} on top of the p-GaN, reducing the gate leakage and increasing the voltage swing. In [15], the lateral-etching of the gate metal interlayer on top of the p-GaN enhanced the gate TTF by suppressing leakage current at gate edges [16]. However, the high-temperature gate TTF, under both DC [15] and pulsed [27] stress tests, was still limited by the appearance of an additional failure mechanism, occurring in the regions where the gate finger (p-GaN/metal) is exposed to the N-implantation for device termination and isolation purposes.

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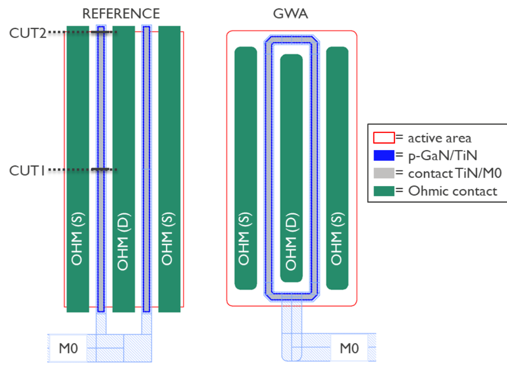

Fig. 1. Top view reference (left) and GWA (right) HEMT layout.

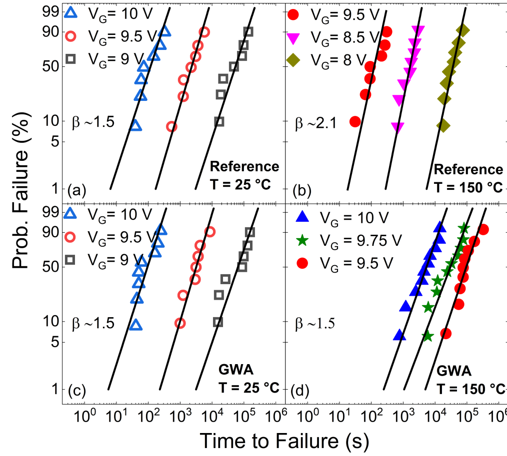

Fig. 2. Weibull plot with different pulsed stress voltages in the case of reference (top) and GWA (bottom) devices at the temperature of 25°C (left) and 150°C (right). GaN-on-Si devices have been adopted.

In this letter, we propose and validate a new gate layout that, keeping the same process and epi-stack, avoids the exposure of the p-GaN gate to the N-implantation, hence improving the high-temperature gate lifetime.

II. Device Under Tests (DUTs)

Lateral GaN-on-Si and GaN-on-SOI HEMTs with a Schottky metal/p-GaN gate fabricated by *imec* are considered in this study. The top epi-stack layers grown on a super lattice buffer and a C-doped GaN back-barrier are the same for both substrates, consisting of a 200-nm undoped GaN channel, a 16-nm thick AlGaN barrier with 23.5% Al content, a 80-nm p-GaN layer with Mg concentration of $3{\cdot}10^{-19}$ cm^{-3}, and a thin TiN metal interlayer which is laterally etched [15], followed by a thick interconnect metal deposition (M0). P-GaN and TiN are patterned to form the gate stack. An Al_2O_3/SiO_2 stack is deposited on the access regions and p-GaN sidewalls as surface passivation layer. Device's active area is defined by means of a nitrogen (N)-implantation. Ohmic contacts to the 2DEG are formed by etching, cleaning, Ti/TiN/Al-based metallization, and low-temperature anneal [31]. Finally, other two levels of Al-based interconnects are formed with SiO_2 inter-metal-dielectric layers. The wafer is passivated with a SiN layer. The DUTs have a gate-to-source and gate-to-drain distance of 1.5 μm. The gate width and length are 100 μm and 1.3 μm, respectively.

The reference device layout consists of a straight gate finger (p-GaN/TiN stack) placed between drain and source ohmic contact fingers. It extends beyond the active area boundary to avoid conductive paths (i.e. 2DEG) between drain and source. Conversely, the GWA device features a gate layout with a closed rectangular shape, completely enclosing the drain ohmic finger, as shown in Fig. 1. In both cases, the gate is connected to the probe pads by means of M0.

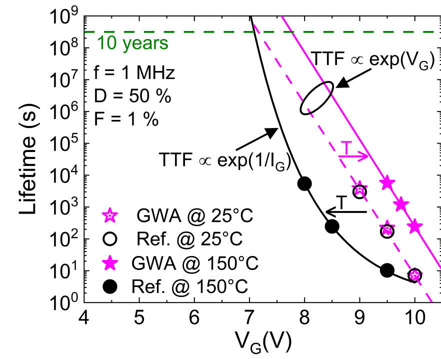

Fig. 3. Lifetime comparison in the case of reference (circles) and GWA (starts) devices at 25°C (open) and 150°C (solid). Failure criterion: 1 % of failure extrapolate from Weibull plots in Fig. 2.

Time-dependent gate breakdown (TDGB) analyses are performed under DC and pulsed stress conditions. For DC stress, a constant voltage is applied to the gate until its current abruptly increases above 1 mA, defining the TTF. In pulsed stress, a periodic square-wave is applied to the gate. Source and drain contacts are forced to 0 V for both stress tests. The square-wave features: frequency f = 1 MHz, duty cycle D = 50 %, and rise/fall time of 5 ns. The test temperatures (T) are 25 °C and 150 °C. Further details on the DC and pulsed experimental setup can be found in [15] and [25], respectively.

III. Results and Discussion

Fig. 2 shows the Weibull plots of the gate TTF, arising from pulsed stress tests at varied gate voltages (V_G) for reference (top) and GWA (bottom) devices at 25 °C (left) and 150 °C (right), while Fig. 3 reports the lifetime plot from Fig. 2 results using a 1% failure criterion (F). In Fig. 3 can be noticed that: i) reference and GWA devices show the same lifetime at 25°C (open circles and stars, respectively). We demonstrated in [13], [15] that the TDGB for T $<$ 80 °C occurs in the active gate area. Since there are no differences in terms of gate epi-stack, doping profile and equivalent area between the two structures, no differences are expected; ii) by increasing T the TTF shows the same V_G-dependency in the case of GWA devices (solid star-symbols in Fig. 3), i.e. TTF $\propto$ exp(V_G), whereas it changes in TTF $\propto$ exp(1/I_G) in the case of the reference ones. The latter TTF dependency is a feature of the isolation breakdown as demonstrated in [19] and [27]; iii) the TTF shows positive and negative T-dependency in GWA and reference devices, respectively. The positive T-dependency is ascribed to the role of the impact ionization (*ii*) in the depleted region of the Schottky junction where a high electric field is present [13], [15], hence associated to the active gate area. Indeed, as T increases, the *ii* rate decreases, along with the related current density, which reduces the probability of creating additional defects. The latter, adding up to pre-existing ones lead to the creation of a percolation path, eventually causing the gate failure [15].

In addition to a different adopted lifetime fitting-model and T-dependency, the failure in the isolation region or in the

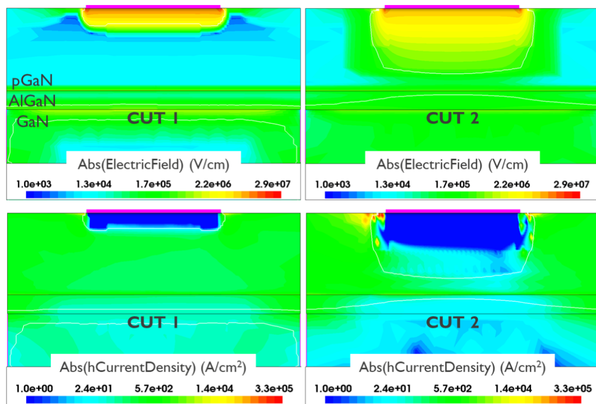

Fig. 4. Electric field (top) and hole current density (bottom) distribution monitored at cut 1 and cut 2 (Fig. 1). The bias condition is $V_G = 9$ V and $V_D = V_S = 0$ V.

active gate area is further supported by a different β reported in Fig. 2. Isolation failure, i.e. reference devices at 150 °C (Fig. 2b), exhibits a higher β compared to failures in the active gate area (Fig. 2a, c and d). It is reasonable to hypothesize that possible impurities and process variability have a greater impact on the electrostatic characteristics of the active area, e.g. the Schottky junction and/or the AlGaN barrier, compared to a heavily N-implanted (insulative) semiconductor region. Consequently, the mechanisms underlying gate breakdown in the active area exhibit larger variability, eventually leading to a smaller β.

To explain why reference devices are affected by isolation breakdown, three-dimensional TCAD simulations [32] have been performed. The gate leakage, crucial for the electrostatic potential of the semi-floating pGaN layer, has been modeled using the strategy reported in [33], i.e., considering nonlocal and trap-assisted tunneling through the Schottky and AlGaN barrier, respectively. Fig. 4 shows the electric field and hole current density distribution along the two cutlines shown in Fig. 1, i.e., in the middle of the gate finger (cut 1) and at the interface between the isolation region and the active gate area (cut 2). Along cut 2, a wider depleted region implies a broader high electric field area, with current density peaks at the edges of the gate metal. These peaks, combined with electric field peaks, can promote breakdown in localized regions independent of area and/or perimeter. Conversely, in cut 1, although electric field peaks are present, the current density is much less intense, making it less prone to degradation mechanisms.

The superior robustness of GWA devices to high-T TDGB has been proven also under static CVS tests in the case of GaN-on-SOI technology, as reported in Fig. 5. The adoption of a different technology allows us to demonstrate the effectiveness of the proposed solution regardless of the employed substrate, rather than a comparison with the GaN-on-Si. The isolation failure observed in reference devices (red diamonds) for $V_G \leq 9.5$ V, resulting in a shorter gate TTF, is not observed in the GWA ones, which show the same V_G-dependency (E-model) reported in pulsed tests (Fig. 3). It is worth noting that, as extensively demonstrated in [19], with V_G close to Schottky junction breakdown ($\geq \sim$10 V for this technology), reference devices also fail within the active gate area, as the Schottky junction is exposed to a high electric field. Indeed, as reported in Fig. 5, both structures show the same gate TTF at $V_G = 10$ V, given their identical gate area. This is

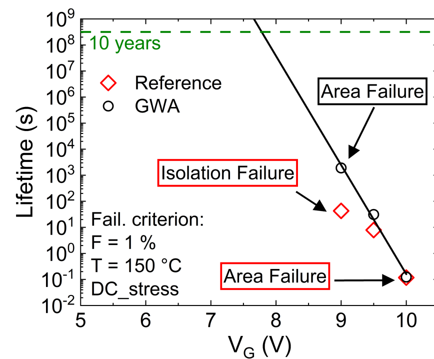

Fig. 5. Lifetime comparison under DC stress at 150 °C in the case of GWA (circles) and reference (diamond) devices. Same failure criterion as Fig. 3. GaN-on-SOI devices have been adopted.

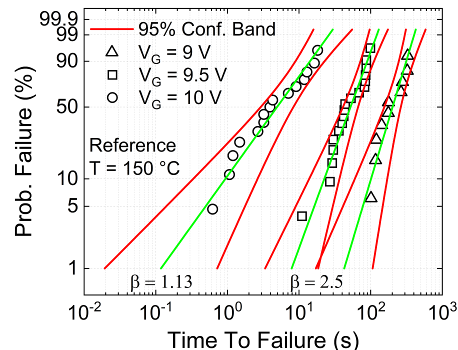

Fig. 6. Weibull plot with different DC stress voltages at 150 °C in the case of reference devices. GaN-on-SOI devices have been adopted.

corroborated by Fig. 6, reporting the Weibull plot for different V_G in reference devices. A lower β, indicative of area failure, is observed only at $V_G = 10$ V, further establishing the correlation between β and failure mechanism. Note that, the gate area failure of GaN-on-Si reference devices (Fig. 2b) is not observed as the gate stress is limited to 9.5 V, therefore in a bias region where isolation failure is dominant [19].

IV. Conclusion

In this letter, we proposed and validated a gate layout solution for p-GaN gate HEMTs, aimed at improving the robustness to high-T TDGB. It consists in avoiding the exposure of the p-GaN/TiN stack to the N-implantation used to define the active region of the device, therefore eliminating the associated wear-out failure. Results have shown a superior robustness under both high-T CVS and pulsed stress tests, demonstrating the occurrence of impact ionization during forward gate bias in a wide temperature range up to 150 °C.

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