Behavioral Modeling of GaN MMIC Varactors for Tunable Matching Networks

# Behavioral Modeling of GaN MMIC Varactors for Tunable Matching Networks

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## Abstract

This work proposes an automated framework for the characterization and behavioral modeling of varactor devices, targeting the implementation of tunable matching networks in Gallium Nitride (GaN) Monolithic Microwave Integrated Circuit (MMIC) technology. A preliminary study of various varactor implementations is conducted. For each considered layout, a behavioral approach is applied by vector-fitting the impedance response and automatically synthesizing an equivalent-circuit network. As a case study, the resulting model for an island-type varactor is then used in the design of an integrated tunable matching network, which addresses tracking of the supply-dependent optimum point of power-added efficiency (PAE) of an amplifier stage across different power levels.

## 1 Introduction

Variable capacitors, or varactors, are critical components in RF and microwave engineering, as they enable circuit reconfigurability. They are widely used in applications such as voltage-controlled oscillators (VCOs) [1], frequency-tunable patch antennas [2], filters [3], phase-shifters [4], and power amplifiers (PAs) [5]. From a technological standpoint, discrete varactor implementations can leverage a variety of material systems with tailored properties, as well as flexible spatial configurations [6]. They have been shown to support effective impedance tuning in matching networks [7], thereby enhancing PA performance under varying operating conditions.

In this context, varactors are expected to play a pivotal role in enabling reconfigurability to optimize functionality, efficiency, and linearity in RF front-end architectures [8] employed in modern communication systems. However, as 5G and emerging 6G technologies advance

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toward operating frequencies in the millimeter-wave range and beyond, there is a growing demand for fully integrated varactor solutions.

Various technologies have demonstrated the feasibility of integrating varactors into high-frequency reconfigurable circuits. In [9], a programmable gain amplifier with multi-band switching capability and operation up to the Ka-band was implemented in Silicon Germanium (SiGe) BiCMOS technology, utilizing an integrated varactor bank to achieve reconfigurability. A W-band voltage-controlled oscillator (VCO) realized in Gallium Nitride (GaN) technology is presented in [10], demonstrating the potential of GaN for high-frequency tunable components. The work in [11] employs MMIC GaN-on-Silicon Carbide (SiC) HEMTs configured in a cold-FET topology as varactor elements for implementing tunable bandstop filters using variable delay lines, with demonstrated operation up to 4 GHz. Furthermore, HEMT-based varactors in GaN-on-SiC technologies have been investigated for phase shifter designs operating at Ka-band [12] and W-band [13].

As demonstrated by these results, MMIC technologies offer an ideal platform for integrating varactors alongside active and passive circuitry, enabling significant reductions in size, insertion loss, and parasitic effects. Nevertheless, most MMIC High-Electron-Mobility Transistor (HEMT) processes do not include standard, ready-to-use varactor devices. As a result, designers are often required to adopt custom implementations. The most straightforward method to realize a varactor at high frequencies involves the use of a Schottky diode under reverse bias, where the depletion capacitance varies with the applied voltage. In cases where custom layouts are not feasible due to fabrication constraints or strict design rules, varactors are often realized by repurposing available layouts of transistors or switches [14, 15]. For enhanced performance, multiple basic varactor elements may be combined into more complex varactor cells [16].

Given these challenges, robust and flexible varactor modeling techniques are essential to ensure the success of MMIC design workflows. Ideally, such models should be described using equivalent circuit representations to facilitate seamless integration into Computer-Aided Design (CAD) tools. Traditional modeling approaches focus on capturing the physical mechanisms within the depletion region, as well as accounting for pad parasitics and leakage effects [17, 18, 19, 20]. However, these approaches typically require detailed knowledge of the process technology, which is often unavailable for commercial MMIC platforms. Furthermore, such information might be completely unknown when the varactor is implemented through a custom layout.

This article outlines the procedures adopted for implementing and utilizing varactors for the case of a 120-nm GaN MMIC process. Due to the unavailability of a nominal varactor device, diodes of various sizes were experimentally evaluated as varactors by extracting the relevant figures of merit. These diodes were also combined to form varactor cells, enabling independent voltage control through an additional bias contact.

A general-purpose behavioral modeling procedure—requiring no prior knowledge of the varactor—is then applied to both individual diodes and varactor cells. This modeling flow can be fully automated and produces an equivalent-circuit representation with adjustable complexity, which can be tailored by the designer based on the required accuracy. The behavioral model extracted for the varactor cell is subsequently used to design an integrated matching network that enables efficiency tracking across different supply voltage levels in a power amplification stage. Finally, conclusions are presented.

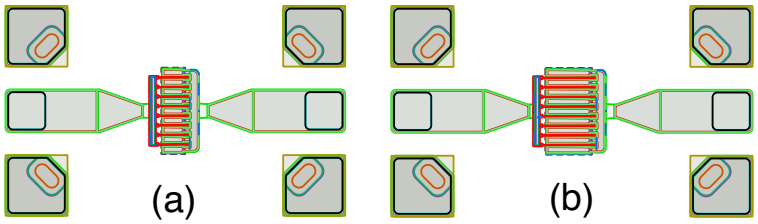


Figure 1: Interdigitated varactor layouts in the 120-nm GaN MMIC technology considered in this work. (a) 8×50 $\mu$m diode (**D1**); (b) 8×100 $\mu$m diode (**D2**).

## 2 Measurement-based characterization of varactors

Similary to other RF-GaN power technologies [18], no dedicated varactor device was available in the foundry PDK selected for this study. Therefore, a standard HEMT layout was adapted by internally short-circuiting the drain and source contacts, forming a so-called HEMVAR (high-electron-mobility varactor) diode structure [14, 19, 20]. In this configuration, the gate metal functions as the anode, while the combined drain and source contacts serve as the cathode, exploiting the variation of depletion charge in the GaN channel to achieve the desired variable capacitance effect.

Two HEMVAR diodes with interdigitated cells were fabricated. As illustrated in Fig. 1, both devices feature the same number of fingers but differ in finger length: Fig. 1(a) corresponds to an 8-finger × 50 $\mu$m configuration (**D1**), while Fig. 1(b) represents an 8-finger × 100 $\mu$m layout (**D2**). Both diodes are implemented as two-port devices, with the bias voltage $V_{\mathrm{B}}$, defined as the difference between the voltage applied to the DC path of the anode and that of the cathode, applied via two external bias-tees.

To evaluate the figures of merit of these two diodes as varactors, small-signal $S$-parameters are measured using a two-port vector network analyzer (VNA) over the 1–30 GHz frequency range, across a sweep of bias voltages $V_{\mathrm{B}}$. The bias is applied at the anode, while the cathode is connected to ground. The measurements are subsequently post-processed to de-embed the access structures, which are preliminarily characterized through electromagnetic (EM) simulations that account for the full substrate stack.

While **D1** and **D2** are measured as two-port devices, only the varactor effect between port 1 and port 2 is relevant in this case. Therefore, as done in [21], a $\pi$-network representation is adopted, in which the shunt elements are verified to represent only bias-independent parasitic effects to ground, whereas the varactor behavior is captured by $Y(V_{\mathrm{B}}, f) = -Y_{21}(V_{\mathrm{B}}, f)$, $Y_{21}(V_{\mathrm{B}}, f)$ being the element of the $2 \times 2$ $Y$-matrix obtained from the measured $2 \times 2$ $S$-matrix.

Two fundamental metrics were considered for the evaluation of the varactor behavior [22], namely, the equivalent capacitance ($C_{eq}$) and the quality factor ($Q$-factor). These can be seamlessly extracted as bias-dependent and frequency-dependent quantities from the one-port admittance $Y(V_{\mathrm{B}}, f)$ using the following equations:

$$C_{eq}(V_{\mathrm{B}}, f) = \frac{\Im\{Y(V_{\mathrm{B}}, f)\}}{2\pi f}; \qquad Q(V_{\mathrm{B}}, f) = \frac{\Im\{Y(V_{\mathrm{B}}, f)\}}{\Re\{Y(V_{\mathrm{B}}, f)\}}; \tag{1}$$

where $f$ is the frequency.

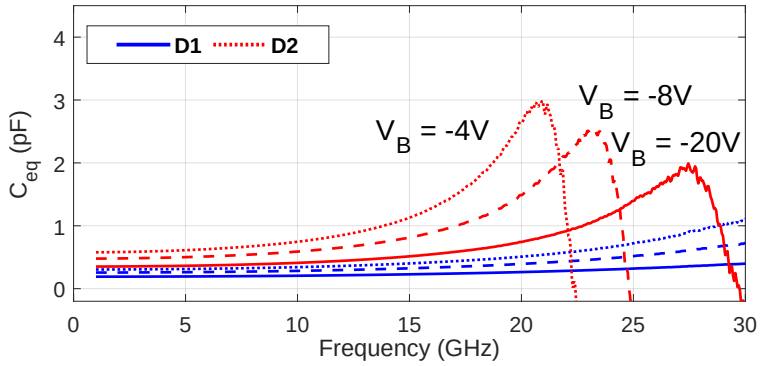


Figure 2: Equivalent capacitance ($C_{eq}$) extracted as from (1) for devices **D1** (blue) and **D2** (red) in Fig. 1. Solid lines correspond to $V_{\mathrm{B}} = -20$ V, dashed lines to $V_{\mathrm{B}} = -8$ V, and dotted lines to $V_{\mathrm{B}} = -4$ V.

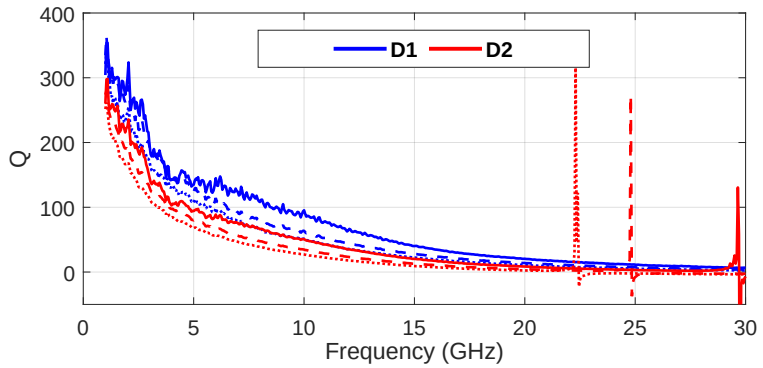


Figure 3: Quality factor ($Q$) extracted as from (1) for devices **D1** (blue) and **D2** (red) in Fig. 1. Solid lines correspond to $V_{\mathrm{B}} = -20$ V, dashed lines to $V_{\mathrm{B}} = -8$ V, and dotted lines to $V_{\mathrm{B}} = -4$ V.

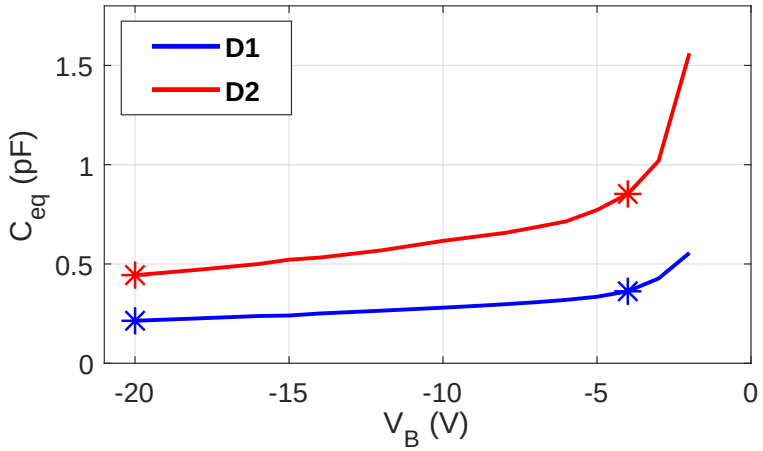


Figure 4: Equivalent capacitance ($C_{eq}$) extracted for the varactors in Fig. 1 at fixed $f = 12$ GHz. The points highlighted at $V_B = -20$ V and $V_B = -4$ V indicate the values used for calculating the $TR$ as from (2).

Table 1: Quality factor ($Q$), equivalent capacitance ($C_{eq}$), and tuning range ($TR$) at multiple frequencies for diodes **D1** and **D2**. $Q$ and $C_{eq}$ are extracted at $V_{\mathrm{B}} = -20$ V, while the $TR$ is computed considering $V_{\mathrm{B}} = -20$ V and $V_{\mathrm{B}} = -4$ V.

| **Frequency** | **D1** | | | **D2** | | |
|---|---|---|---|---|---|---|
| | $Q$ | $C_{eq}$ (fF) | $TR$ | $Q$ | $C_{eq}$ (fF) | $TR$ |
| 8 GHz | 108 | 200 | 24% | 66 | 387 | 27% |
| 10 GHz | 95 | 206 | 25% | 51 | 410 | 30% |
| 12 GHz | 64 | 213 | 26% | 35 | 443 | 32% |
| 15 GHz | 40 | 228 | 27% | 20 | 515 | 38% |
| 17 GHz | 30 | 240 | 29% | 14 | 584 | 43% |

The results are presented in Figs. 2 and 3, where three bias voltage values are considered across the measured range $V_{\mathrm{B}}$ = -20 to -2 V. As could be expected, the device having the higher active area exhibits a resonant frequency at around 18 GHz for the lower bias voltages, whereas the smaller device displays a capacitive behavior up to 25 GHz, due to lower value of $C_{eq}$. As $C_{eq}$ features negative values at high frequency, the inductive parasitic parts become predominant and the device no longer acts as a tunable capacitance. To quantitatively characterize the effective capacitance variation over the operating range of interest, the tuning range ($TR$) can be computed at each given frequency [23]:

$$TR = \frac{C_{\max} - C_{\min}}{C_{\max} + C_{\min}}, \tag{2}$$

where $C_{\max}$ and $C_{\min}$ are the maximum and minimum capacitance values, respectively.

This evaluation confirms that the devices can work as varactors, as the capacitance is effectively tuned by the applied bias voltage. Specifically, when considering a fixed single frequency, $C_{eq}$ can be plotted against the bias voltage, as shown in Fig. 4, where $C_{\max}$ and $C_{\min}$ are evaluated at $V_B = -4$ V and $V_B = -20$ V, respectively. These voltage values are used to ensure that the varactors remain in a charge-depleted state, avoiding the abrupt variation of capacitance linked to channel formation in HEMVARs [15]. The obtained results in terms of $TR$, defined as in (2), are reported in Table 1.

To employ diode-based varactors such as **D1** and **D2** in a matching network, DC voltage control must be provided through a dedicated bias network. In this case, two different varactor cells were created using **D1** as the base diode unit. In the first cell, shown in Fig. 5(a) and referred to as **C1**, two diodes are placed in an anti-series configuration sharing the anode contact. One cathode is connected to ground via a backvia, while the other serves as the RF input terminal, thereby creating a one-port structure. The bias is supplied through a separate contact pad using a $\lambda/4$ line at $f = 16.5$ GHz. This anti-series configuration is particularly suitable for high-RF-power designs, as it can compensate for odd-order nonlinearities, but suffers from a theoretically halved capacitance value [24, 25].

In the second cell, shown in Fig. 5(b) and referred to as **C2**, two anti-series cells are combined in parallel to increase the overall capacitance of the structure. The bias connection

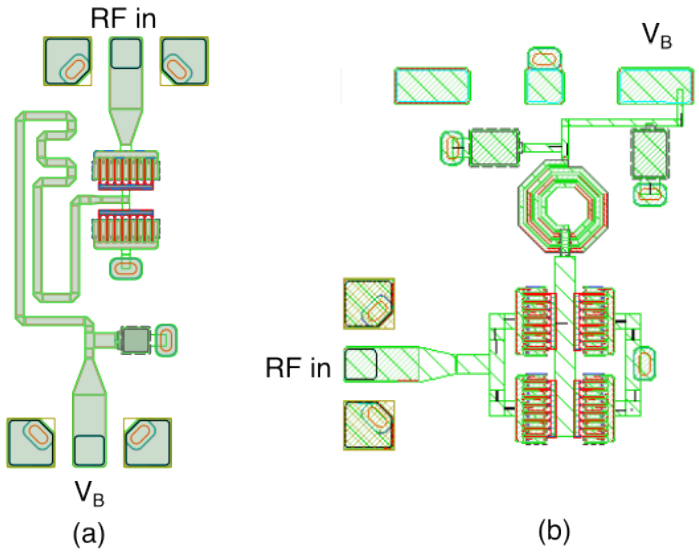


Figure 5: Layouts of varactor cells including the bias network. (a) Anti-series topology. (**C1**); (b) Island topology made by the parallel of two anti-series structures (**C2**).

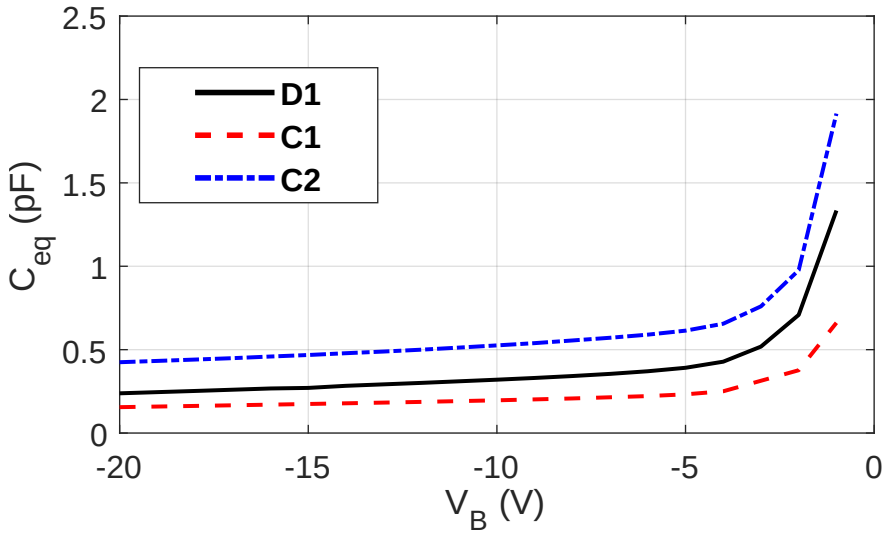


Figure 6: Equivalent capacitance ($C_{eq}$) extracted for cells **C1** and **C2** at 16.5 GHz across the bias voltage $V_{\mathrm{B}}$. The plot also reports the values of **D1** for comparison purposes.

is implemented using an $LC$ network centered at $f = 16.5$ GHz. The characterization previously described for the diodes was also applied to these cells, resulting in the figures of merit reported in Figs. 6 and 7 at 16.5 GHz.

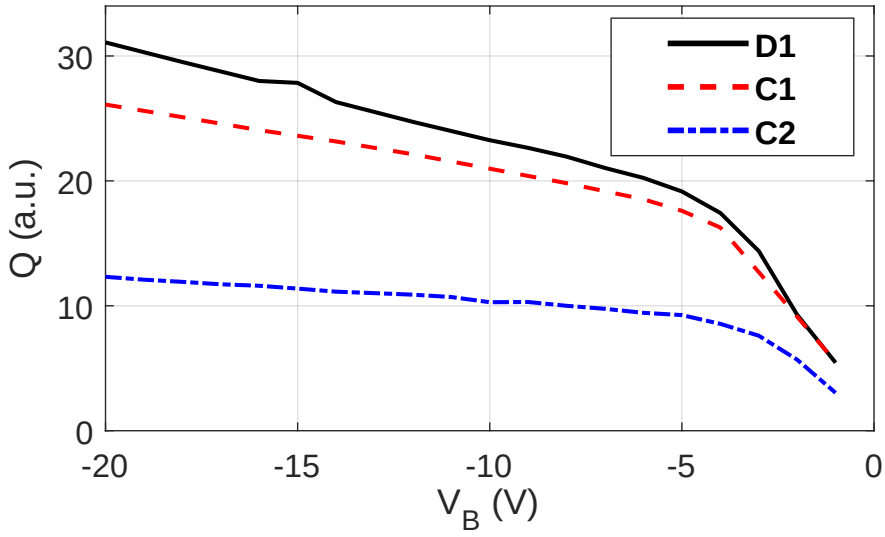


Figure 7: Quality factor ($Q$) extracted for cells **C1** and **C2** at 16.5 GHz across the bias voltage $V_{\mathrm{B}}$. The plot also reports the values of **D1** for comparison purposes.

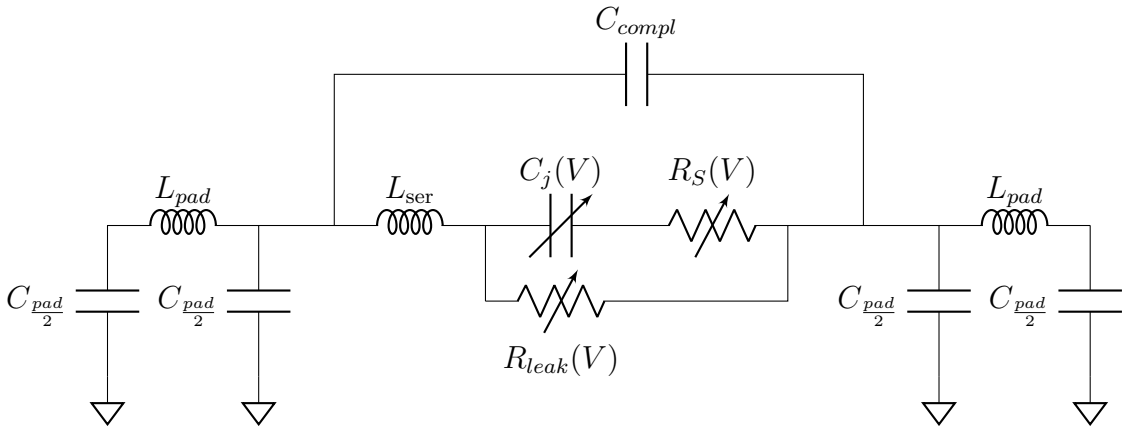


Figure 8: Equivalent-circuit model topology for a varactor diode as derived from a physics-based approach.

# 3 Varactor modeling

## 3.1 Physics-based approach

Irrespective of the actual varactor technology, the basic core elements in the small-signal model of a one-port diode in the depletion region are a series nonlinear capacitor and resistor (denoted as $C_j(V)$ and $R_S(V)$, respectively, in Fig. 8) [17, 14, 19]. In addition, a large resistor in parallel—with typical values ranging from 100 kΩ to 1 GΩ—is included to model the leakage current.

Additional inductors and capacitors can be incorporated to account for the typical distributed interdigitated structures and the corresponding physical interactions between the fingers ($C_{compl}$) and the ground plane, as well as the finger inductance ($L_{ser}$) [26]. Accesses pads are instead modeled using a $CLC$ $\pi$-network (with elements $C_{pad}$ and $L_{pad}$ in

Fig. 8) [14, 19, 27], or, depending on the access cells, even by a single capacitor [17]. This fixed network topology is derived from the knowledge of the dominant physical effects of the reverse-biased diode and suitable heuristics for the overall layout of the structure.

The typical strategy for identifying the elements in Fig. 8 is based on experimental data, particularly multi-bias small-signal $S$-parameter measurements. The approach relies on wideband measurements to capture both low-frequency behavior and high-frequency resonant effects. Measurements at different frequencies or bias-voltage subranges are used to separate the effects of different elements, under specific hypotheses on the physical behavior of the varactor [28]. Additional optimization steps may be necessary to properly account for extra elements excluded from the classical extraction process [19].

It is important to highlight that the described physics-based modeling approach and the corresponding schematic in Fig. 8 are generally limited to single-diode devices, as it is typically not possible to identify all the effects occurring in more complex varactor cells composed of several diode devices and additional biasing structures. This limitation is especially relevant for state-of-the-art MMIC processes, or when the varactor cell is arranged in a custom configuration.

## 3.2 Behavioral approach

In this work, an alternative behavioral approach [21] was adopted to model both single diodes and more complex varactor cells within the same framework. The methodology does not assume any *a priori* knowledge of the device under test (DUT) and, despite its empirical nature, it automatically yields an equivalent-circuit implementation suitable for CAD simulation. A diagram outlining the main conceptual steps of this approach is presented in Fig. 9.

As with other methods, the first step consists in collecting multi-bias $S$-parameter measurements across several reverse-bias $V_\mathrm{B}$ points. In this case, however, the frequency range can be freely chosen depending on the target operating frequency. If the DUT is measured as a two-port, the $S$-parameter data can first be converted into $Y$-parameters to easily allow for the de-embedding of shunt parasitic effects as discussed in Sec. 2, hence obtaining the one-port device admittance. In turn, this can be converted into the impedance function $Z$. Conversely, if the DUT is already in a one-port configuration [18], the $S$-parameter can be directly converted into the impedance $Z$.

The obtained bias-dependent impedance $Z(\omega_k)$, acquired in a discrete set of $K$ positive frequencies $\omega_1 \dots \omega_K$, can be fitted at each bias $V_\mathrm{B}$ with a rational function of the form:

$$Z(s) = \frac{b_0 s^m + b_1 s^{m-1} \dots b_{m-1} s + b_m}{a_0 s^n + a_1 s^{n-1} \dots a_{n-1} s + a_n}, \tag{3}$$

where $a_i$ and $b_i$ are real constants. Many methods, such as AAA [29], RKFIT [30], or vector fitting (VF) [31] are available in the literature for fitting a given frequency domain response with a rational function as in (3). VF is adopted in this work obtaining, for each bias $V_B$, with the following formulation:

$$Z_\mathrm{VF}(s, V_\mathrm{B}) = \sum_{p=1}^{P} \frac{r_n(V_\mathrm{B})}{s - p_n(V_\mathrm{B})} + D(V_\mathrm{B}) + sE(V_\mathrm{B}), \tag{4}$$

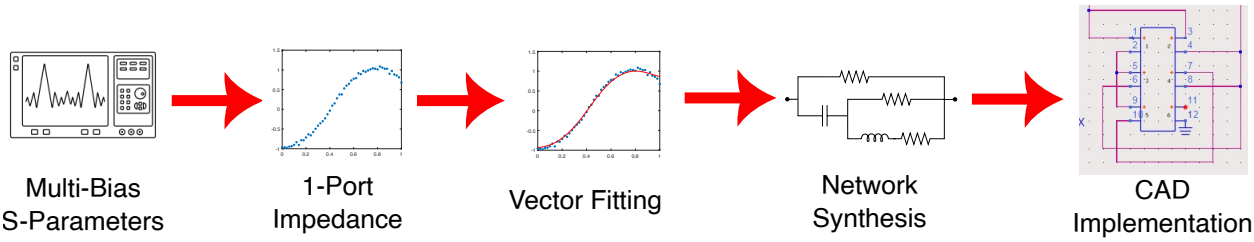


Figure 9: Conceptual steps of the proposed modeling approach.

where the complex $p_n$ (poles) and $r_n$ (residues) correspond are either purely real or appear as complex-conjugate pairs, while $D$ and $E$ are purely real parameters. The *order* of the rational representation in (4) is described using the triplet of integers $(P, Q, R)$, where $P$ is the number of poles, while $Q, R \in \{0, 1\}$ indicate the absence or presence of the terms $D$ and $E$, respectively.

The fitted impedance function can also be rearranged in the following form:

$$Z_{\mathrm{VF}}(s, V_{\mathrm{B}}) = \frac{\prod_{n=1}^{P} (s - z_n(V_{\mathrm{B}}))}{\prod_{n=1}^{P} (s - p_n(V_{\mathrm{B}}))} + sE(V_{\mathrm{B}}). \tag{5}$$

where the ratio between the numerator and denominator polynomials of degree $P$ is known as a $P$th order function (e.g., 2nd order or biquadratic for $P = 2$, 3rd order or bicubic with $P = 3$, etc.), with $P$ poles $p_n$ and $P$ zeros $z_n$. The function $Z_{\mathrm{VF}}(s, V_{\mathrm{B}})$ represents the impedance of a linear passive lumped electrical network (4) if and only if it is *positive real* (PR) [32, 33], which is equivalent to requiring the following conditions:

1. $Z_{\mathrm{VF}}(s)$ must be analytic in $\Re\{s\} > 0$, i.e., it has no poles in the open right-half $s$-plane;
2. $\Re\{Z_{\mathrm{VF}}(s)\} > 0$ for $\Re\{s\} > 0$;
3. $Z_{\mathrm{VF}}(s)$ must be real for real $s$.

These constraints can be automatically imposed during the VF procedure [34], so that any fitted impedance function at a given bias is guaranteed to be realizable as a passive linear lumped component network such as those used in classical approaches.

The bias-dependent VF in (5) could in principle result in a different complexity level $(P, Q, R)$ at each varactor bias voltage. However, the use of a fixed complexity level across the whole bias range is a necessary (but not sufficient) step in ensuring that the resulting equivalent circuit has a fixed topology with voltage-controlled components, as customary in standard modeling approaches. Therefore, the $(P, Q, R)$ values must be selected as the maximum values that ensure a good fit to the small-signal data across the entire bias range of interest [16].

Once the fitting in (5) is obtained at each bias voltage, several well-established methods for synthesizing circuits starting from a given PR impedance function are reported in literature. System-theoretic approaches [35, 36], in which the $Z_{\mathrm{VF}}$ in (5) is directly implemented as a series of first and second-order impedances, can result in negative-valued $RLC$ elements even for a PR function. Alternatively, classical network theory has produced several constructive results for the synthesis problem [32, 37, 38]. The most widely used approach is the

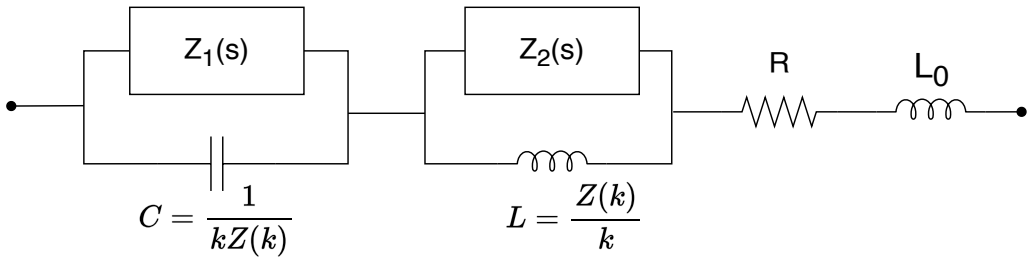


Figure 10: First step of the Bott-Duffin synthesis procedure.

so-called Brune synthesis [39], in which a PR impedance function with $P$ poles is synthesized using $P$ positive-valued $RLC$ components and ideal two-port transformers.

The use of transformers or negative $RLC$ components in the equivalent circuit of the varactor can be tolerated as a purely empirical modeling choice, provided that a close fitting is achieved. However, these approaches clearly fail to provide a physically-plausible equivalent circuits, such as those used in classical equivalent-circuit modeling methods (Fig. 8). Some level of interpretability is certainly a desirable feature also for behavioral black-box models, so as to provide a straightforward evaluation of the impact of physical parameters (e.g. layout, width, number of fingers) on the varactor electrical response.

The Bott-Duffin (BD) synthesis technique [32, 37] can provide an implementation of any PR function in terms of positive-valued $RLC$ components, at the cost of increasing the required number of elements above the minimum value of $P$. The algorithm for BD synthesis starts from the fact that PR impedance functions necessarily display an angular frequency $\omega_0$ at which its real part value is minimum (and positive). This allows to split the impedance function as $Z(s) = R_0 + Z^{\min}(s)$, where $R_0 = \Re\{Z(j\omega_0)\}$ can be seen as a resistor in series with the remainder of the network. The synthesis of the PR impedance function $Z^{\min}(s)$, for which $Z^{\min}(j\omega_0) = 0$, is then the main goal of the BD algorithm.

Richard's theorem [32, 37] is then applied by considering a function $R(s)$ computed as:

$$R(s) = \frac{kZ^{\min}(s) - sZ^{\min}(k)}{kZ^{\min}(k) - sZ^{\min}(s)}. \tag{6}$$

It follows that, for all real positive values of $k$, $R(s)$ is PR if $Z^{\min}(s)$ is PR. Solving for $Z^{\min}(s)$ from the expression above yields:

$$Z^{\min}(s) = \left(\frac{R(s)}{Z^{\min}(k)} + \frac{k}{sZ^{\min}(k)}\right)^{-1} + \left(\frac{1}{Z^{\min}(k)R(s)} + \frac{s}{kZ^{\min}(k)}\right)^{-1}. \tag{7}$$

Since (7) represents an impedance, the summation indicates that the two elements inside the brackets can be connected in series to obtain the overall expression for $Z^{\min}(s)$. Moreover, the terms $\frac{k}{sZ^{\min}(k)}$ and $\frac{s}{kZ^{\min}(k)}$ correspond to an inductor and a capacitor, respectively. The network can therefore be configured as shown in Fig. 10, where $Z_1(s) = Z^{\min}(k)R(s)$ and $Z_2(s) = \frac{Z^{\min}(k)}{R(s)}$ and both are still PR. A pair of critical frequencies on the $j\omega$ axis is then extracted from each of the two positive-real (PR) functions, $Z_1(s)$ and $Z_2(s)$, with each

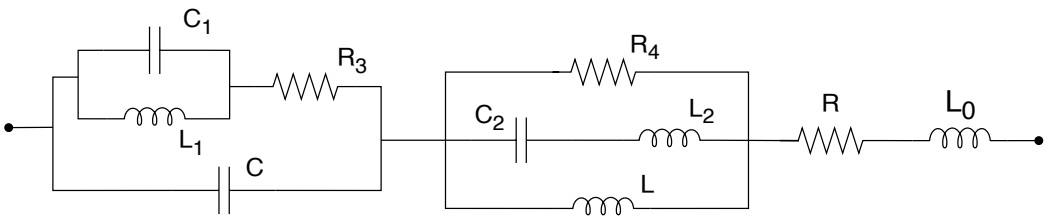


Figure 11: General network **N0** resulting from Bott-Duffin network synthesis of a biquadratic impedance function with $(P, Q, R) = (2, 1, 1)$.

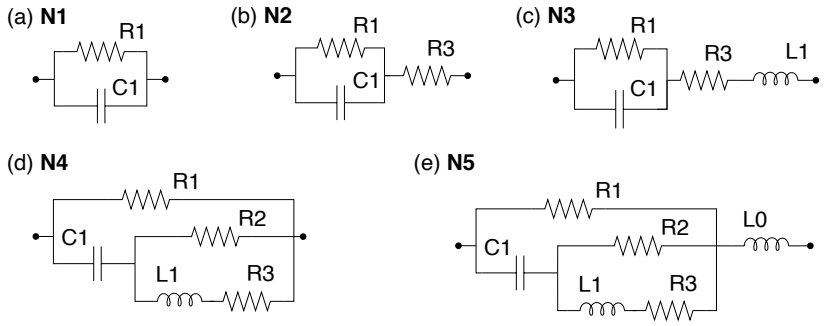


Figure 12: Examples of synthesized networks for fitting complexity of $(P, Q, R) = (1, 0, 0)$ (**N1**), $(P, Q, R) = (1, 1, 0)$ (**N2**), $(P, Q, R) = (1, 1, 1)$ (**N3**), $(P, Q, R) = (2, 1, 0)$ (**N4**) and $(P, Q, R) = (2, 1, 1)$ (**N5**).

realized as a resonant circuit. This procedure is repeated iteratively until $Z_1(s)$ and $Z_2(s)$ become constants (and thus implementable as purely dissipative elements) or are reduced to functions of degree less than 2.

As previously noted, the BD synthesis typically results in an exceedingly large number of reactive elements, i.e., the resulting realization is not *canonical* [40]. For example, for a general biquadratic function–with complexity $(P, Q, R) = (2, 1, 1)$, corresponding to a second-order state-space model–the minimum number of energy storage and resistive elements resulting from BD synthesis is 5 and 2 respectively, as shown in the resulting equivalent circuit **N0** of Fig. 11.

This aspect has driven recent research efforts to find specific compact circuit implementations for the cases of $P \leq 3$, under the hypothesis that the PR rational impedance function displays certain specific properties [41, 42, 43]. In particular, the work in [41] provides a minimal synthesis for all bicubic impedances containing three or less energy storage elements and displaying a series-parallel structure. Some examples of simplified network topologies are shown in Fig. 12. A vector fitting with complexity $(P, Q, R) = (1, 0, 0)$ directly results in network **N1**. Network **N2** can be derived for $(P, Q, R) = (1, 1, 0)$ and a series inductor can be added to obtain network **N3** with $(P, Q, R) = (1, 1, 1)$.

For impedance functions with $P \geq 2$, a given $(P, Q, R)$ complexity does not automatically map into a unique minimal network topology with positive $RLC$ components. Instead, the actual values of poles and residues determine which of several non-equivalent simplified

topologies for the network has to be adopted [16, 41]. For example, biquadratic impedance functions with $(P, Q, R) = (2, 1, 0)$ or $(2, 1, 1)$ would in principle by synthesized by the general network **N0**. However, reduced-order networks **N4** for $(P, Q, R) = (2, 1, 0)$ and **N5** for $(P, Q, R) = (2, 1, 1)$ can also represent the same impedance function, provided that specific provisions are respected [41]. This simplified low-order synthesis is in many cases sufficient to achieve high fitting accuracy for the varactors considered in this study. In the general case, the BD procedure still allows for the synthesis of an equivalent-circuit representation for any conceivable PR one-port impedance function.

The synthesis procedure of the equivalent-circuit, either through the BD method or a reduced order network, is applied separately to $Z_{\mathrm{VF}}$ at each bias-voltage. This could result in different circuit topologies across the voltage range even if a single maximal complexity $(P, Q, R)$ is used [16]. The use of a unique topology across the bias range has to be empirically checked on the actual data or enforced using a more general structure. For example, starting with a fitted impedance function with complexity $(P, Q, R) = (2, 1, 1)$, the provisions for which the simplified network **N5** is a valid implementation have to be satisfied at all bias voltages. Alternatively, the more general network **N0** has to be used for this case, even if some redundant components might have no actual impact on the impedance response [16].

In any case, the proposed behavioral modeling approach is able to produce an equivalent circuit implementation for the one-port varactor, featuring an empirically identified non-bias-dependent topology and multiple bias-dependent $RLC$ components.

## 3.3 Behavioral model validation

Following the outlined behavioral modeling approach, the VF procedure was applied with increasing complexity to the measured impedance of both diodes **D1** and **D2**, as well as cells **C1** and **C2**. The error resulting from the fitting procedure is quantitatively evaluated using the following normalized mean-square-error (NMSE) metric:

$$\mathrm{NMSE}(V_{\mathrm{B}}) = 10 \log_{10} \left( \frac{\sum_{k=1}^{K} \left| Z(\omega_k, V_{\mathrm{B}}) - Z_{\mathrm{VF}}(s, V_{\mathrm{B}})|_{s=j\omega_k} \right|^2}{\sum_{k=1}^{K} |Z(\omega_k, V_{\mathrm{B}})|^2} \right); \tag{8}$$

where $K$ is the number of data points collected at the angular frequencies $\omega_k$, $Z$ represents the measured impedance data, and $Z_{\mathrm{VF}}$ is the vector-fitted impedance. The results are reported in Figs. 13–14 for five selected bias values across the full voltage range, highlighting trade-offs between fitting accuracy and model order.

For both diodes evaluated in this work, good accuracy is achieved even with relatively low complexity. The error exhibits a decreasing trend with increasing fitting complexity, with only marginal improvements beyond a complexity of $(2, 1, 1)$.

The impact of the complexity on the fitting error has been evaluated in the operating frequency range of 16-22 GHz for increasing fitting order. As reported in Fig. 15 the (2,1,1)-**N5** network topology results in an absolute error less than 0.05 Ω for both DUTs across all frequencies and bias values, while higher values up to 1 Ω are observed for the (1,1,1)-**N3** and (2,1,0)-**N4** cases.

The resulting value for each element of the equivalent-circuit network is reported in Fig. 16 for **D1** and **D2**. The core nonlinear behavior is described by C1 and R3, whereas the

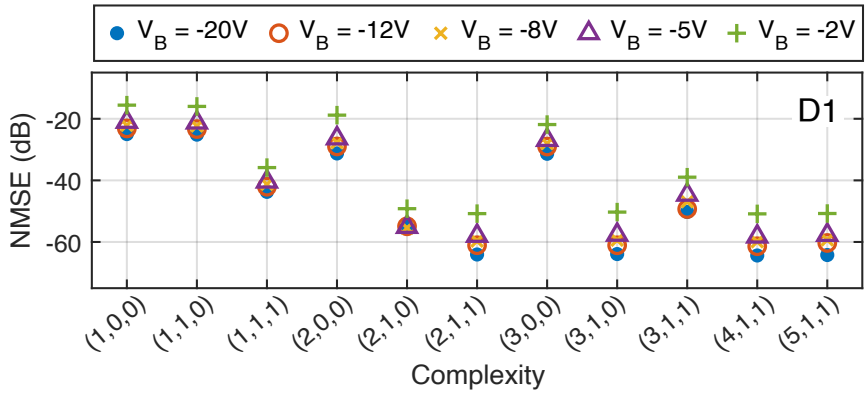


Figure 13: Modeling performance obtained by vector fitting the impedance data at several bias voltages $V_{\mathrm{B}}$ for **D1**. The triplet of integers linked to complexity refers to the expression in (4).

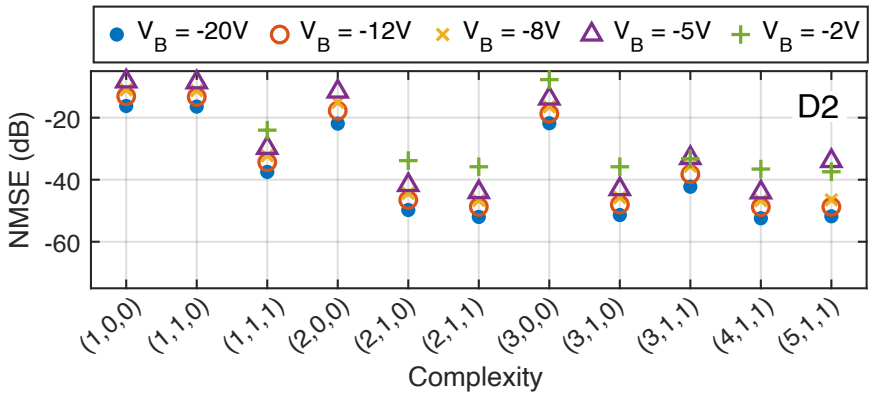


Figure 14: Modeling performance obtained by vector fitting the impedance data at several bias voltages $V_{\mathrm{B}}$ for **D2**. The triplet of integers linked to complexity refers to the expression in (4).

inductances L1 and L0 and parasitic resistor R2 have a relatively low impact on the voltage-dependent behavior of the varactor, and can rather be interpreted as quasi-linear parasitic elements. Coherently with other HEMVAR physical models [14], C1 increases proportionally to $V_{\mathrm{B}}$, with a sharp increase at around $V_{\mathrm{B}} = -4$ V. The R1 resistance, which models the small current leakage across the varactor, reasonably displays values in the MΩ range.

The full two-port varactor structures (including parasitic shunt elements) were implemented in the Keysight Advanced Design System (ADS) CAD environment using symbolically defined devices (SDDs), where the element values are defined as functions of the bias applied to the device terminals through interpolated look-up tables. The accuracy of the implemented equivalent circuits is evaluated in terms of two-port $S$-parameters by means of the following absolute error [44]:

$$E_S(\omega_k, V_{\mathrm{B}}) = \sum_{u=1}^{2}\sum_{v=1}^{2} \left| S_{u,v}^{\mathrm{meas}}(\omega_k, V_{\mathrm{B}}) - S_{u,v}^{\mathrm{model}}(s, V_{\mathrm{B}})|_{s=j\omega_k} \right|^2; \tag{9}$$

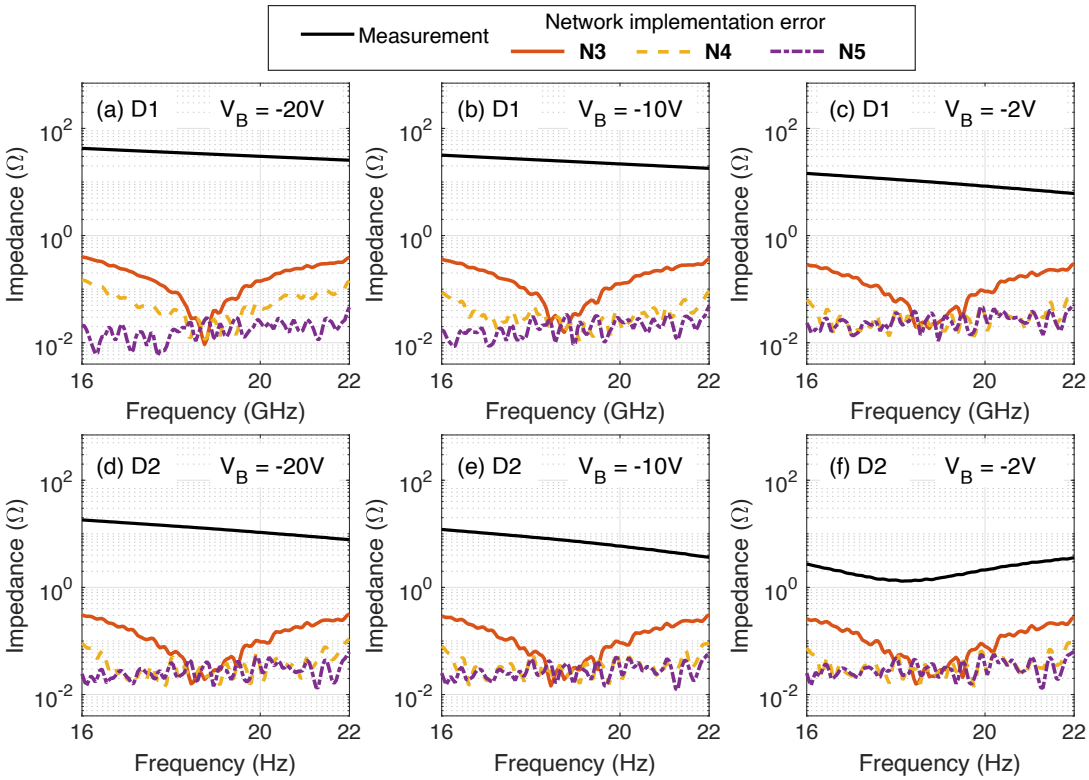


Figure 15: Measured $|Z(\omega_k, V_{\mathrm{B}})|$ impedance (black line) and absolute error across frequency between $Z(\omega_k, V_{\mathrm{B}})$ and the response of the relative circuit-equivalent network. The network synthesis is performed at three different complexities for $V_{\mathrm{B}}$ = -20 V, -10 V, -2 V. (a)-(c) report results for **D1**, while (d)-(f) refer to **D2**.

shown in Figs. 17 and 18 and reporting very small deviations across all tested frequencies and bias voltages.

One of the main advantages of the proposed behavioral framework lies in the flexibility of modeling different one-port structures, without any prior hypotheses on the layout or physical response, as long as they result in PR impedance functions. For example, the full antiseries cells **C1** and **C2** can be directly modeled as one-port equivalent circuits using the proposed global behavioral approach. This has been shown to yield superior performance with respect to a more traditional strategy, in which the lumped diode elements (i.e., **D1** in this case) and the distributed bias/access lines are modeled separately [16]. Indeed, the complex interaction and parasitics due to EM couplings between the different linear/nonlinear elements can greatly increase the complexity of classical modeling approaches, requiring a behavioral framework such as the one proposed here. In this case, however, the resulting equivalent circuit is not expected to bear a one-to-one correspondence to the actual circuit topology implemented in the cells, with the impact of both tunable nonlinear elements and parasitics spread across different $RLC$ components.

The results for cells **C1** and **C2** are reported in Figs. 19 and 20 in terms of NMSE at different complexity levels, and in Fig. 21 in terms of the resulting absolute error across the operating frequency range. The (2,1,1) complexity, with a resulting synthesized equivalent

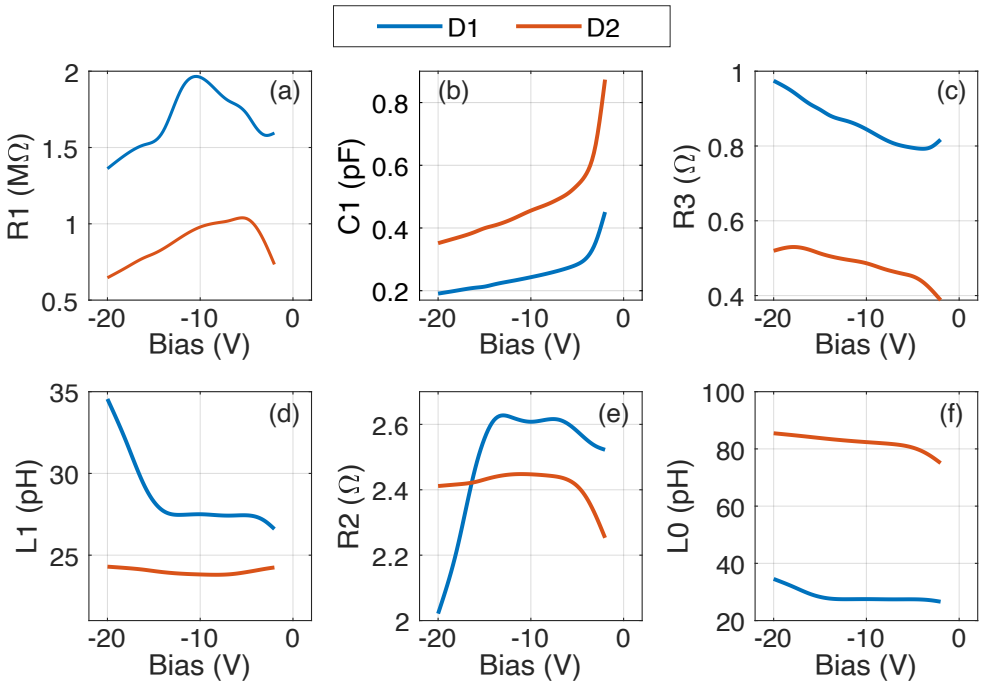


Figure 16: Bias dependency for the circuit elements of synthesized network **N5** in Fig. 12 for **D1** and **D2**.

circuit network with topology **N0**, is sufficient to reach NMSE values below -40 dB for both cells. Remarkably, with respect to the diodes **D1** and **D2**, the full BD network is necessary to synthesize the equivalent circuits for the full cells, without any possibility of resorting to lower order complexity networks such as **N4** or **N5**. The ten bias-dependent elements for **C1** and **C2** are reported in Fig. 22. As previously stated, due to the complexity of the equivalent circuit and the mixing of different effects in each component, the actual behavior is hardly interpretable from a physical standpoint, despite showing well-conditioned trends. The error on the one-port $S$-parameter in the CAD-implemented circuits for **C1** and **C2** is shown in Figs. 23 and 24, again showing a remarkable accuracy of the proposed method even for anti-series varactor cells.

# 4 Varactor-based tunable matching network

The outlined behavioral modeling approach has been applied to the design of tunable matching networks for PAs. While tunability can be exploited for a range of applications, this case study focuses on improving the power efficiency of a typical common-source HEMT stage operated in class-AB targeting a wide power range of operation. Indeed, the possibility to use different reconfigurable power modes is a common requirement in communication systems, as it is often necessary to statically adapt the PA settings to different transmit power levels depending on traffic data or channel conditions.

Standard class-AB operation suffers from low efficiency in the power back-off region [45]. This reduced performance in low-power mode can be partially mitigated by concurrently

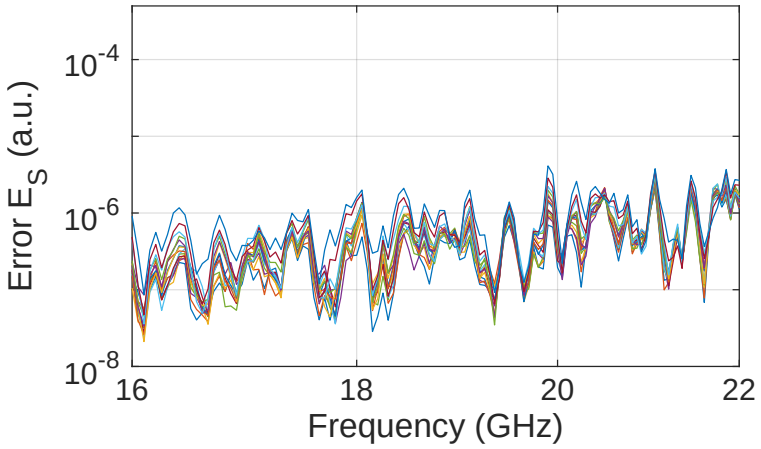


Figure 17: Modeling error $E_S$ as from (9) for **D1** across frequency. Each line corresponds to a different $V_\mathrm{B}$ in the range between -20 V and -4 V.

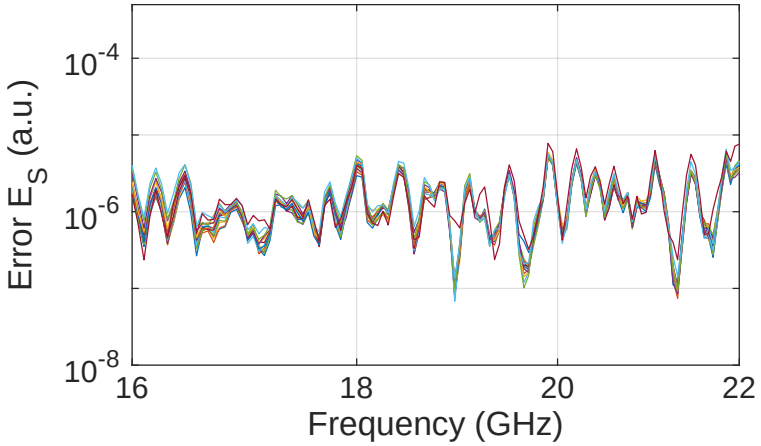


Figure 18: Modeling error $E_S$ as from (9) for **D2** across frequency. Each line corresponds to a different $V_\mathrm{B}$ in the range between -20 V and -4 V.

lowering the static supply voltage of the PA, thereby reducing the power drawn from the supply. However, this supply adaptation shifts the operating point and, correspondingly, generally alters the optimal output matching conditions of the PA stage. A tunable matching network can therefore be used to track the optimal load across the supply [46], thereby maintaining matched output conditions.

To determine the optimal loading conditions across the supply range for the considered PA stage — designed in CAD using the available PDK model from the target 120-nm GaN MMIC technology also used for the varactor design—a simulation-based load-pull study was performed. The dataset includes a sweep of the load reflection coefficient (across the entire Smith chart), along with a combined sweep of the drain-source supply voltage $V_{DS}$ (from $V_{DS} = 18$ V to the nominal value of $V_{DS} = 28$ V) and the available RF input power, ranging from small-signal levels up to values sufficient to reach and surpass the peak power-added efficiency (PAE).

The results in terms of PAE are reported in Fig. 25, with each black dot representing a

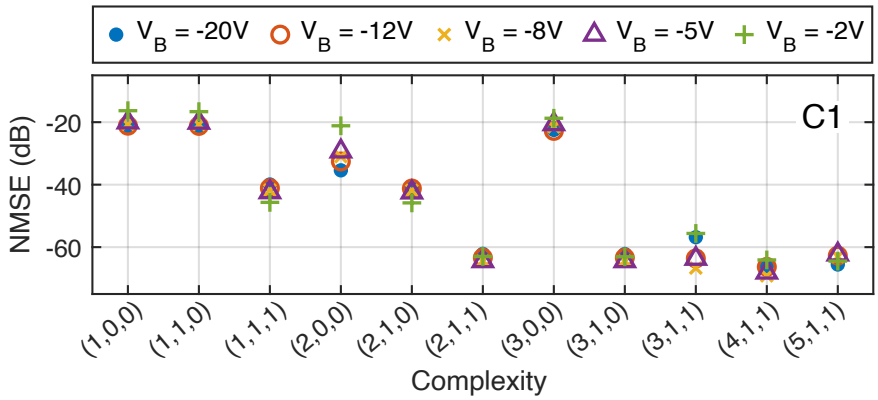


Figure 19: Modeling performance obtained by vector fitting the impedance data at several bias voltages $V_{\mathrm{B}}$ for **C1**. The triplet of integers linked to complexity refers to the expression in (4).

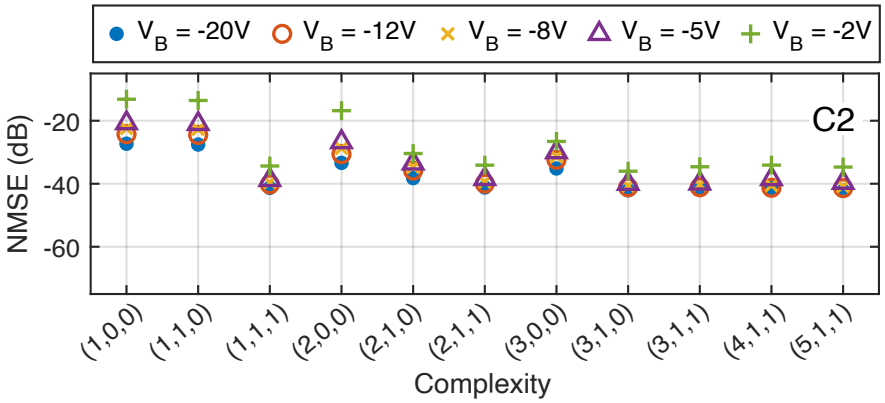


Figure 20: Modeling performance obtained by vector fitting the impedance data at several bias voltages $V_{\mathrm{B}}$ for **C2**. The triplet of integers linked to complexity refers to the expression in (4).

different operating condition. From this dataset, one can highlight the maximum achievable PAE profile across output power under different operating strategies. For example, the blue dots indicate the best PAE profile when only the supply voltage is allowed to vary while keeping a fixed load selected to obtain the best PAE performance at the highest $V_{DS}$ and obtainable by a conventional matching network. In contrast, the red dots show the performance obtained by selecting the optimal load at each power level while maintaining the supply at the nominal value of $V_{DS} = 28$ V. A significantly improved PAE performance can be achieved by jointly optimizing both the load and the supply voltage (pink dots). This combined optimization yields target supply and load profiles as a function of output power. In particular, the target load profile is later reported in Fig. 29.

The tunability functionality of a matching network can be achieved by introducing varactors, either as shunt or series elements [47, 48]. To implement the tunability required to track the load profile shown in Fig. 29, a cell composed of two anti-series diodes (island varactor cell **C2**) was considered. A conventional design of the matching network—comprising several

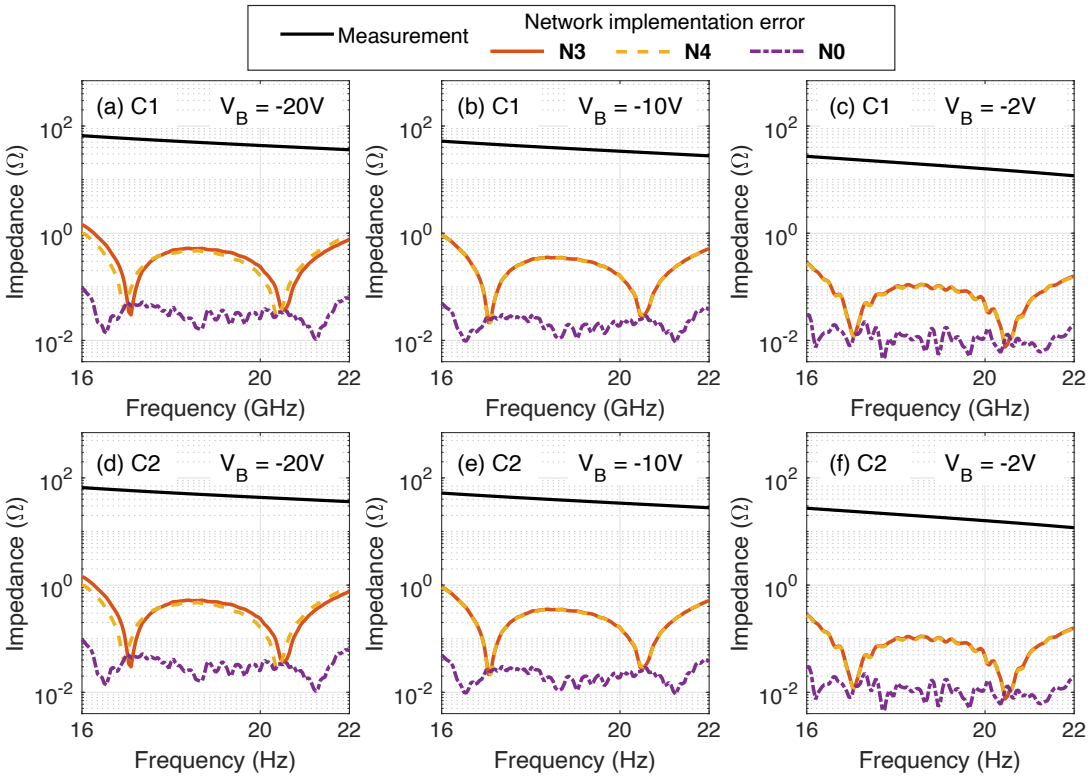


Figure 21: Measured $|Z(\omega_k, V_{\mathrm{B}})|$ impedance (black line) and absolute error across frequency between $Z(\omega_k, V_{\mathrm{B}})$ and the response of the relative circuit-equivalent network. The extraction is performed at three different complexities for $V_{\mathrm{B}}$ = -20 V, -10 V, -2 V. (a)-(c) report results for **C1**, while (d)-(f) refer to **C2**.

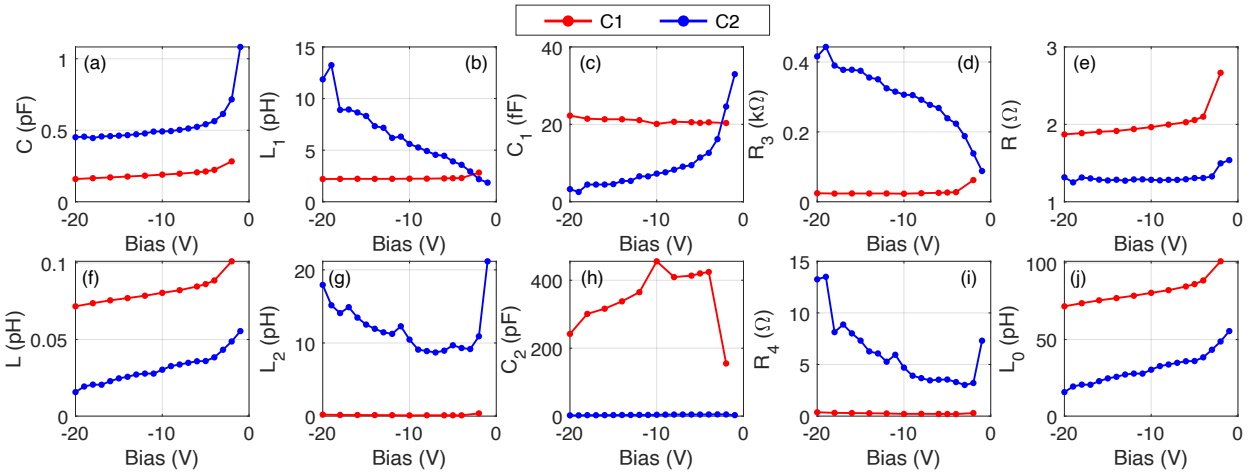


Figure 22: Bias dependency for the ten circuit elements of synthesized network **N0** in Fig. 11 for **C1** and **C2**.

striplines, along with inductors and capacitors as available in the MMIC process design kit (PDK)—was carried out to target the desired inductive region of the load. Two instances of the **C2** cells were inserted in a series configuration to maximize the tuning range of the

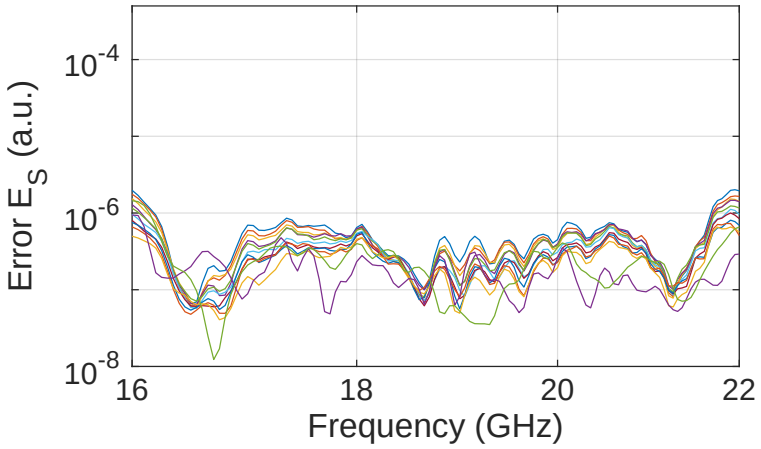


Figure 23: Modeling error $E_S$ as from (9) for **C1** across frequency. Each line corresponds to a different $V_{\mathrm{B}}$ in the range between -20 V and -4 V.

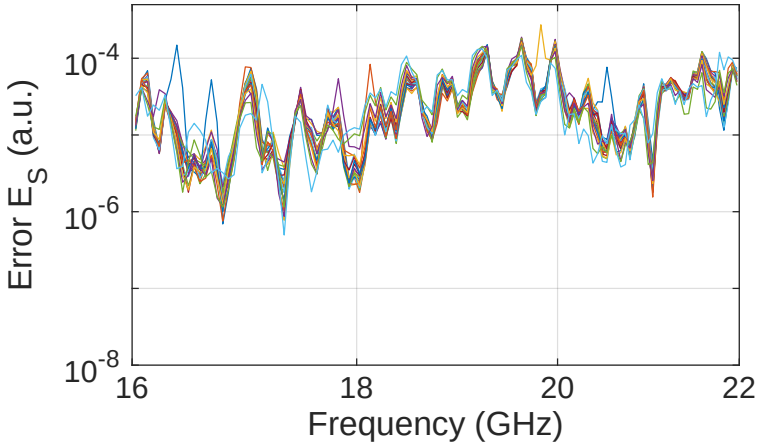


Figure 24: Modeling error $E_S$ as from (9) for **C2** across frequency. Each line corresponds to a different $V_{\mathrm{B}}$ in the range between -20 V and -4 V.

element, ultimately resulting in the circuit topology shown in Fig. 26. Figure 27 graphically illustrates the resulting load tunability range enabled by the two island varactor cells across the Smith Chart. The complete layout of the tunable matching network, including two bias networks that allow independent voltage control of the two island varactor cells, is shown in Fig. 28. This network was fabricated separately to evaluate its standalone performance.

An $S$-parameter measurement campaign was conducted by sweeping the two bias control voltages, $V_{B1}, V_{B2} \in \{-4, -30\}$, to characterize the full practical tunability range. The resulting area covered in terms of load impedances is shown in the Smith Chart plot in Fig. 29, and is found to be sufficient to reasonably cover the target load profile required for optimal matching of the PA stage under consideration. The set of control voltages capable of tracking the wanted impedance profile as a function of power are reported in Fig. 30.

Finally, Fig. 31 shows the insertion loss of the matching network across the selected control voltages for a 1 GHz bandwidth centered at 16.5 GHz. In this case study, substantial losses are observed across the operating band due to the introduction of multiple varactors,

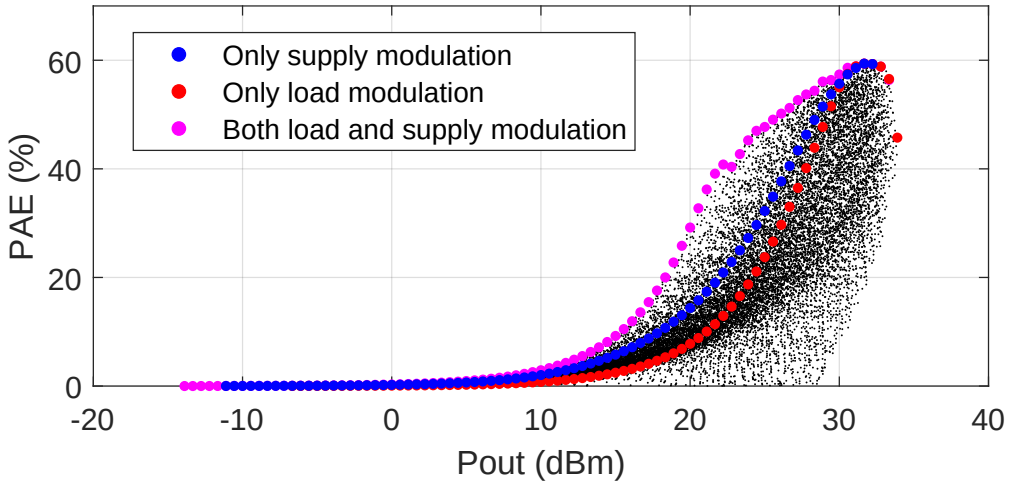


Figure 25: PAE performance extracted at 16.5 GHz for a common-source HEMT stage in the target 120 nm GaN MMIC technology. Blue dots represent the envelope when a fixed load is imposed across multiple $V_{DS}$; red dots are obtained selecting the best loads for the nominal $V_{DS} = 28$ V; pink dots are obtained by selecting the best load for each tested $V_{DS}$.

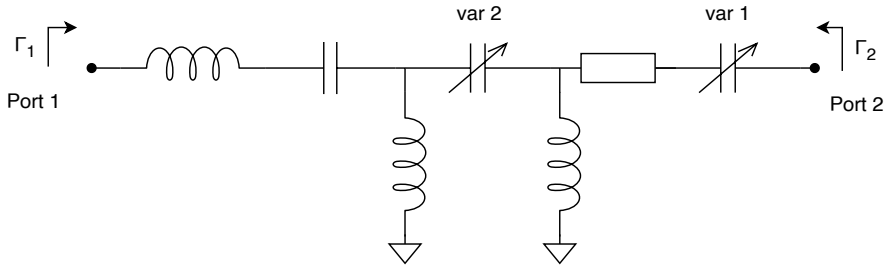


Figure 26: Schematic representation of the realized matching network including the varactor cells.

whereas the variation in loss across the different values of the control bias voltages $V_{B1}$–$V_{B2}$ at the center frequency of 16.5 GHz is approximately 0.5 dB. Overall, the lower performance that a tunable matching network generally yields compared to a conventional matching network requires a trade-off evaluation against the efficiency improvement resulting from load adaptation.

# 5 Conclusion

A framework has been proposed for the circuit-equivalent modeling of MMIC varactors. This behavioral approach is fully automated and allows users to select the desired circuit complexity based on the required model accuracy within the target frequency range. The approach was demonstrated through the realization of a tunable matching network that employs a modeled island varactor topology in order to track the maximum PAE of an amplifier stage across output power modes. While further advancements in baseline technology, var-

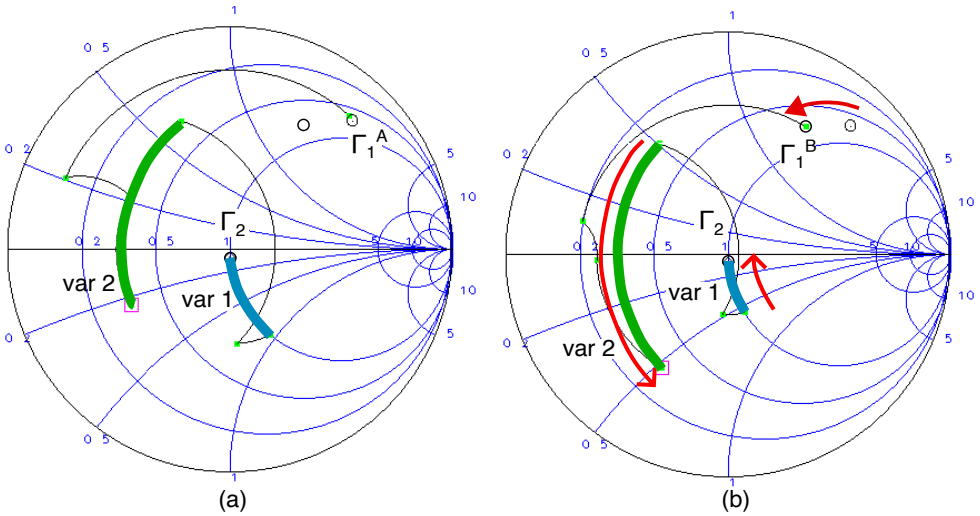


Figure 27: Reflection coefficient $\Gamma_1$ synthesized by the matching network at port 1 with the topology in Fig. 26. The effect of the two varactor cells (var1 and var2) is highlighted by reporting two extremal tuning configurations in (a) and (b), respectively.

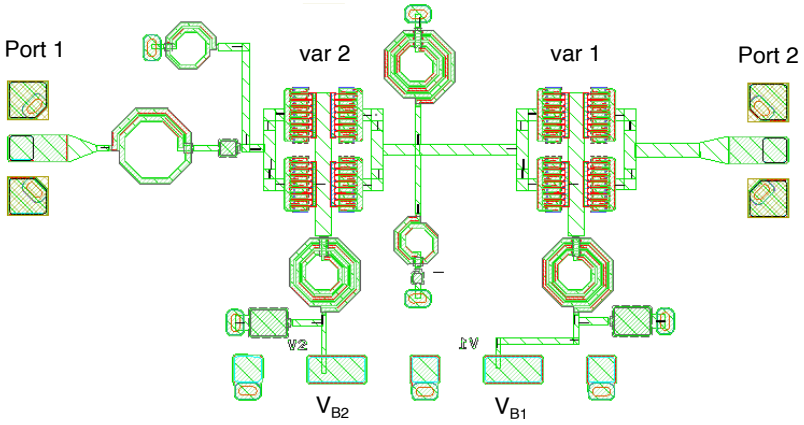


Figure 28: Layout of the designed tunable matching network. The target impedance is realized at port 1, while port 2 is to be terminated to the 50 Ω load. The two pads at the bottom allow to provide independent bias voltages to the two varactor cells.

actor layout, and matching network topology are necessary to enable reconfigurable efficient PA topologies at microwave frequencies, this automated framework offers a fast and accurate methodology for evaluating and demonstrating new varactor devices and varactor-based MMIC circuit implementations.

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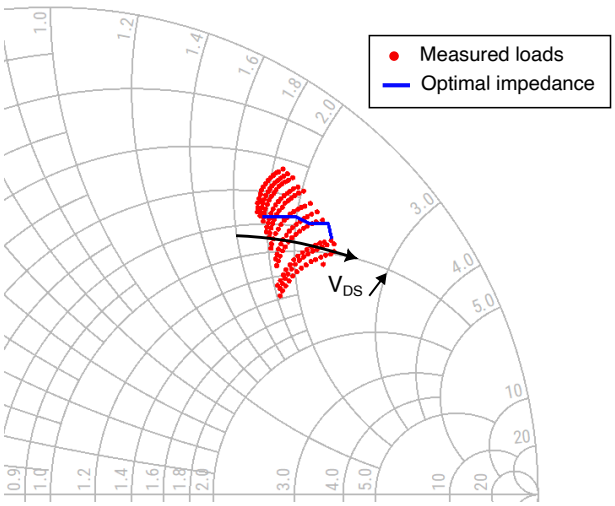


Figure 29: Loads extracted for all combinations of varactor biases (red dots) extracted at 16.5 GHz and best impedance trajectory (blue line) extracted from load-pull simulations with $V_{DS}$ swept from 18 V to 28 V.

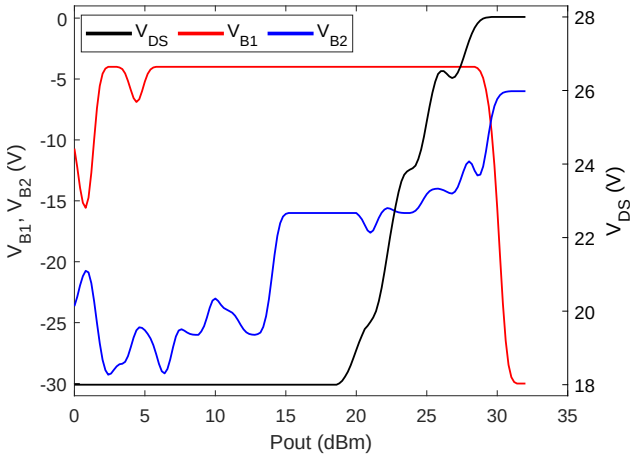


Figure 30: Control voltages for $V_{DS}$, $V_{B1}$ and $V_{B2}$ across output power $P_{\text{out}}$.

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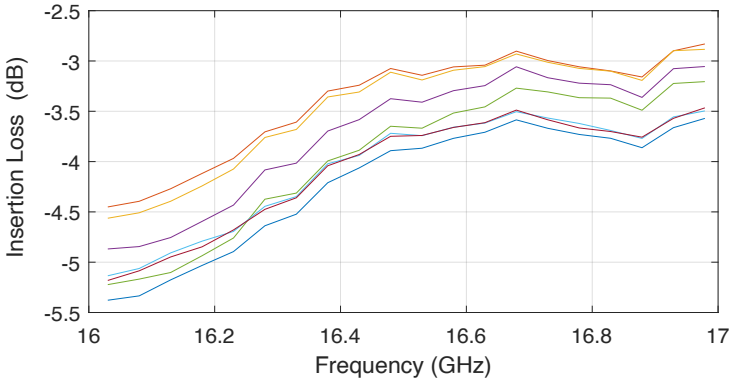


Figure 31: Insertion loss of the designed tunable matching network extracted from small-signal measurements at selected varactor bias voltages.

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