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Characterization of the Dynamic R_{ON} of 600 V GaN Switches under Operating Conditions

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Abstract: High-voltage GaN switches can offer tremendous advantages over silicon counterparts for the development of high-efficiency switching-mode power converters at high commutation frequency. Nonetheless, GaN devices are prone to charge-trapping effects that can be particularly relevant in the early-stage development of new technologies. Charge-trapping mechanisms are responsible for the degradation of the dynamic ON-resistance (R_{ON}) with respect to its static value: this degradation is typically dependent on the blocking voltage, the commutation frequency and temperature, and is responsible for the reduction of power converter efficiency. The characterization of this phenomenon is very valuable for the development of a new process to compare different technological solutions or for the final assessment of performance. This characterization cannot be made with traditional static or small signal measurements since R_{ON} degradation is triggered by application-like dynamic device excitations. In this paper, we propose a technique for the characterization of the dynamic R_{ON} of high-voltage GaN switches under real operating conditions: this technique is based on the design of a half bridge switching leg in which the DUT is operated under conditions that resemble its operation in a power converter. With this setup, the characterization of a 600 V GaN switch dynamic R_{ON} is performed as a function of variable blocking voltages and commutation frequency. Additionally, this technique allows the separation of thermal and trapping effects, enabling the characterization of the dynamic R_{ON} at different temperatures.

Keywords: GaN switches; trapping effects; ON-resistance; dynamic ON-resistance; GaN device characterization; GaN power converters

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1. Introduction

High-voltage (i.e., >600 V) GaN power switches are today the major enabler toward the development of a new generation of switching-mode power converters with upgraded performance in terms of power density, efficiency and simplified thermal management. The superiority of this wide band gap (WBG) technology can be mainly summarized as reduced conduction and switching losses with respect to silicon technologies.

Compared to SiC WBG technology, for nominal breakdown voltages up to 650 V, GaN has also demonstrated the capability of further increasing the application frequency, allowing for an additional enhancement of volumetric power density, due to the reduced dimensions of magnetics and capacitors [1,2]. Higher-frequency regimes with associated high efficiency have also a beneficial impact in the choice converter topologies [3,4] and on the power converter control bandwidth. High-voltage GaN switches for power conversion applications are typically AlGaN/GaN-on-Si high electron-mobility transistors (HEMTs) ([5]). This type of device (mainly with SiC substrates) has a 20-year heritage in the field of RF and microwave applications, where it is nowadays adopted for the implementation of analog amplifiers delivering up to tens of watts up to 40–50 GHz. The adaptation of these technologies to power-converter applications required technological solutions to obtain higher breakdown voltages [6] (from tens of volts to several hundreds of volts) and

the exploitation of p-doped GaN gate to get normally OFF devices [7] (RF/microwave GaN HEMTs are normally ON devices).

At present, these developments have led to the availability of GaN power switches with typical breakdown voltages up to 600–650 V and optimal driving voltage V_{GS} of about 5 V [8–10]. Other switches with 50 V, 100 V, 200 V breakdown voltage with very high current capability can also be found in the market [11,12], whereas only very few experimental devices of 900 V technologies have recently been proposed [13].

While there is a tremendous interest in this high-voltage GaN technology, especially in the automotive market [14], these products have a limited heritage, and several providers are still optimizing their processes internally or in contract research foundries. One peculiar characteristic of GaN technologies is the presence of charge-trapping effects. As documented in the literature, GaN transistors are always affected by trapping states that modulate the number of carriers available for conduction into the channel [15–18]. The high electric field induced by the high voltage applied to the device during the blocking state of switching-mode operation triggers charge capture. The charge trapping is a very fast process that is typically almost entirely activated even for a very short duration of the blocking voltage (ns). Conversely, when the device is driven into conduction with $V_{DS} \simeq 0$ V, the inverse phenomenon takes place, namely charge release [19], which is typically much slower. For this reason, operatively, when the blocking voltage is removed, and the device is switched ON for the conduction part of the period, several charges are not available for the conduction and the observed R_{ON} in dynamic condition is larger than its static value. The slower the charge release mechanism, the higher the degradation of dynamic R_{ON} [20,21]. The charge release time constants are accelerated by higher temperature. Thus, R_{ON} degradation is a function of the switching frequency (i.e., amount of time for charge release during the device ON time) and temperature. Moreover, it is also a function of the application voltage since the amount of charge trapping increases with the electric field, which is a function of the blocking voltage [22].

The dynamic modulation of R_{ON} is a very important topic since it directly affects the converter efficiency and can lead to reliability concerns due to the higher dissipated power than expected from nominal static characteristics of the device. While a complete elimination of this effect is impossible for GaN devices, its minimization is possible by means of technological choices and optimizations [23]. In this context, it is extremely useful for foundries and research centers to perform a reliable characterization of R_{ON} degradation in dynamic regime, in which the dependence of this phenomenon to voltage, frequency and temperature should be identified. Measurement set ups and procedures for this characterization are very challenging to develop, especially for the large-application voltages and very fast commutation dynamics of the technology. Several measurement techniques have been proposed in the literature [24–30], attesting to the importance of the topic. One of the targets of the measurement procedure must be the capability to test the DUT in a working regime as close as possible to the actual regime of the final application. Nonetheless, this is hardly achievable by the majority of the approaches proposed in the literature; hence, additional investigations are needed to precisely reproduce the application scenario during the device characterization. The proposed approach gives an additional contribution to the field of high-voltage GaN switches nonlinear dynamic characterization.

Toward this goal, in this paper, we propose a set-up and a measuring technique that accurately mimics the operating conditions of the real application. A custom switching module is designed in order to embed the DUT in a half-bridge switching-stage, and a measurement procedure is implemented to characterize its dynamic R_{ON} when operating as in a real power converter. The setup is designed to test 600–650 V switches in different voltage, frequency and temperature switching conditions. In Section 2, the measured procedure is described. The design and implementation of the switching module and of the measurement set up are described in Sections 3 and 4, respectively. Finally, the results of the experimental characterization of 600 V GaN switches are provided in Section 5.

2. Measurement Procedure

The measurement procedure is similar to the one proposed in [31] for low voltage devices. The circuit described in this section implements a half-bridge commutation leg with two identical device samples. The low-side switch is the DUT, whereas the high-side device is used to complete the switching leg that is necessary to operate the DUT in the same condition of the real application. The working principle of the measurement technique is outlined in Figure 1a,b.

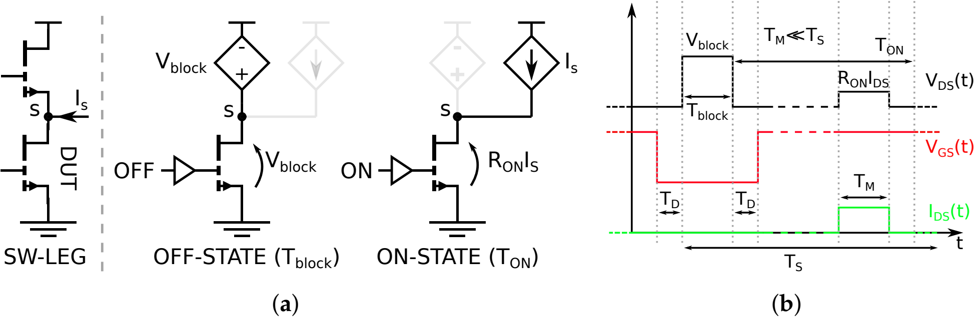


Figure 1. Measurement technique working principle. (**a**) Switching leg states during the dynamic periodic measurement procedure; (**b**) waveforms of the proposed measurement technique.

When the switching leg is commutating, the period can be divided in two parts: during T_{block} the DUT is OFF and the high side device connects the DUT drain to the blocking voltage V_{block} (triggering charge trapping); during T_{ON}, the DUT is in conduction and a precise current source connected to the switching node S is used to inject a measuring current I_{DS} into the DUT. The measuring window within T_{ON} is called T_M. During the measuring window, both the DUT current I_{DS} and the DUT voltage V_{DS} are sensed with accuracy so that the ON resistance is given by the ratio $R_{ON} = V_{DS}/I_{DS}$. According to Figure 1b a safety dead time is introduced between V_{DS} and V_{GS} transitions to avoid shoot through as in a real application. There are two ways to characterize the DUT dynamic R_{ON} as a function of the switching frequency, which are illustrated in Figure 2.

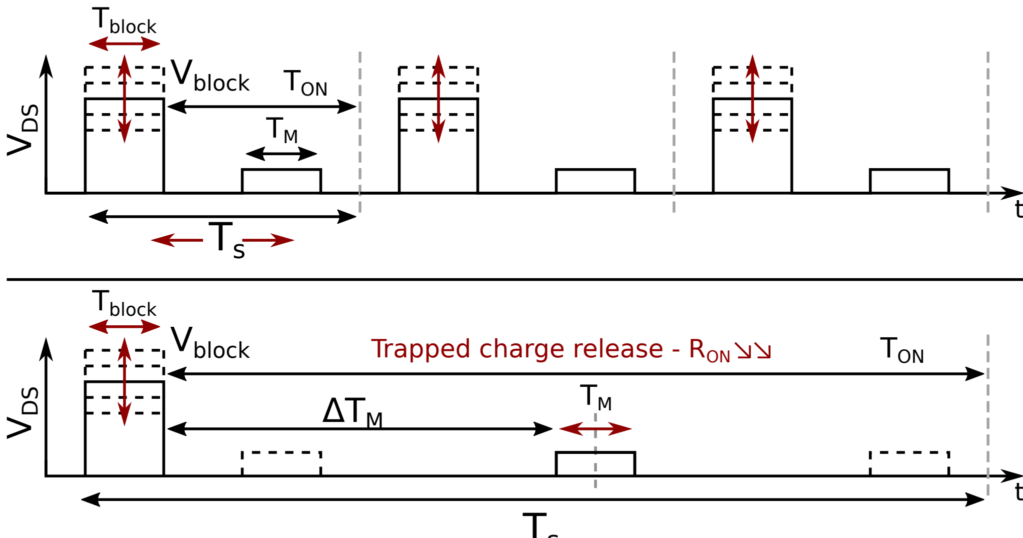


Figure 2. Two different measurement regimes. Upper: direct characterization of $R_{ON}(f_S)$ varying the period $T_S = 1/f_S$. Lower: indirect characterization of $R_{ON}(f_S)$ at fixed period T_S and varying ΔT_M.

The more direct method is to vary the period T_S within the values of interests for practical applications and measure R_{ON} for every different switching frequency $f_S = 1/T_S$ regime. The waveforms corresponding to this method are shown in the upper part of Figure 2: the drawback of this method is that the switching losses also vary with T_S and so

the different characterizations are not isothermal. This inhibits the possibility to separate trapping and thermal effects. As described in the lower trace of Figure 2, the alternative solution that we propose is to maintain a fixed, very long period T_S with 99.9% V_{DS} duty cycle (i.e., $T_{block} << T_S$ and $T_{ON} \simeq T_S$) and characterize the R_{ON} variation over time by moving the measurement window T_M along the very long T_{ON} of the DUT. Indeed, during T_{ON}, the trapped charge release mechanism takes place, decreasing the R_{ON} over time. This is an indirect, still equivalent, way to characterize the dependence of the dynamic R_{ON} vs. frequency since we can consider R_{ON} measured in ΔT_M equal to $R_{ON}(f_S)$ with $f_S = 1/(\Delta T_M)$. As can be observed in Figure 2, ΔT_M is the distance between the beginning of T_{ON} and of the associated trapped charge release mechanism, and the measuring instant. This consideration strictly holds if the duration of T_{block} is not important for the observed device performance, which is an alternative way to state that the charge trapping event can be considered almost instantaneous, with respect to the application time scale. This has been verified and will be documented in the measurement section, and it was also observed in other studies [31]. With the proposed procedure, the characterization of the dynamic R_{ON} over time, and then, equivalently, over switching frequency, is isothermal, allowing to separate the thermal and trapping effects. Moreover, the DUT temperature can be known with fairly good precision by controlling the temperature of the testing module: indeed, by selecting values of the measuring current I_{DS} and measuring window T_M small enough to have a negligible self-heating effect on the DUT, the DUT channel can be considered at the same temperature as the module carrier. Finally, the dependence of the dynamic R_{ON} on the application voltage can be assessed by varying the value V_{block} applied to the DUT.

3. Design and Implementation of the Switching Module

As discussed in the introduction, the DUT is embedded in a switching module that accurately matches the actual operation of the DUT in a real application. Thus, the designed module is practically the active section of a half-bridge power converter. GaN technology characteristics set the specification for the module design. Here, the DUT is a 600 V p-GaN e-mode HEMT power device on silicon substrate of a process under development in a research foundry. In Table 1, the preliminary nominal electrical specifications of the switch are listed.

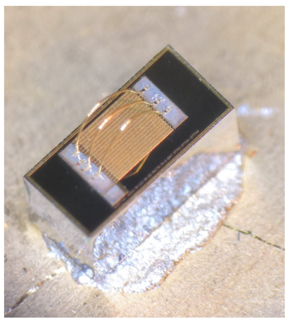
Table 1. DUT electrical specifications.

V_{BD}	V_{gs}	V_{th}	R_{DS}	C_{ISS} [1]	C_{OSS} [1]	C_{RSS} [1]
600 V	5–6 V	2–2.5 V	0.5 Ω	43 pF	18 pF	1 pF

[1] V_{DS} = 200 V.

The extremely low values of parasitic capacitances highlight the potentiality of this technology for very fast commutations. The expected commutation time is around 1 ns, which imposes to accurately design the power converter layout to minimize parasitic inductances and to select a proper driver and by-pass capacitors. As described in Figure 3, the DUT is in bare-die form with the gate, drain and source pads on the top of the die.

Therefore, all the connections to the rest of the module need to be provided with wire bonding, whose length must be kept as short as possible to minimize parasitics and have a minimal impact on commutation waveforms. Moreover, the die thickness of 1.05 mm further complicates the design of the switching module assembly (the die is not lapped to the typical 100 um thickness, since it comes from experimental wafers: this is very typical during process development). Thus, as illustrated in the sectional view of Figure 4, a double-board approach is followed.



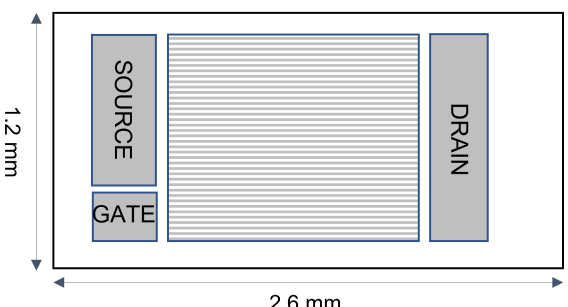


Figure 3. Picture of the bare-die GaN power switch with some test wire bonding between source and drain pads and corresponding dimensions.

A 2-layer 1 mm-thick FR4 board is dedicated to the placement of all the SMD components of the module, whereas the switches are placed at the same plane of the top of the FR4 board, exploiting two apertures implemented for their placement (see Figure 5). On the other hand, an IMS board is employed as a carrier of the GaN switches and stacked beneath the FR4 board. In this way, as can be appreciated in the photograph of Figure 5, the access points for the gate, source and drain pads are on the same level as the FR4 board, and the bonding wires' length from the board to the die is minimized. The switches' dies are attached to the IMS board by means of a high-thermal and high-conductive paste: the backside of the switches is the substrate potential, which must be connected to the source of each switch available in the upper side of the FR4 board, thanks to the wire bonding connections. Thus, as described in Figure 4, the filled VIAs in the FR4 board are used to connect the substrate potentials in the IMS board to the device sources on the top layer of the FR4 board.

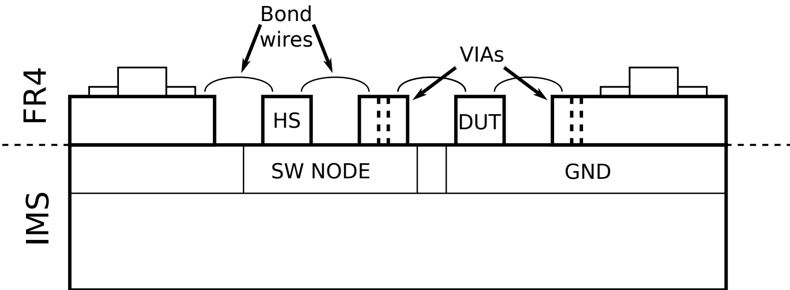


Figure 4. Lateral section of half-bridge module.

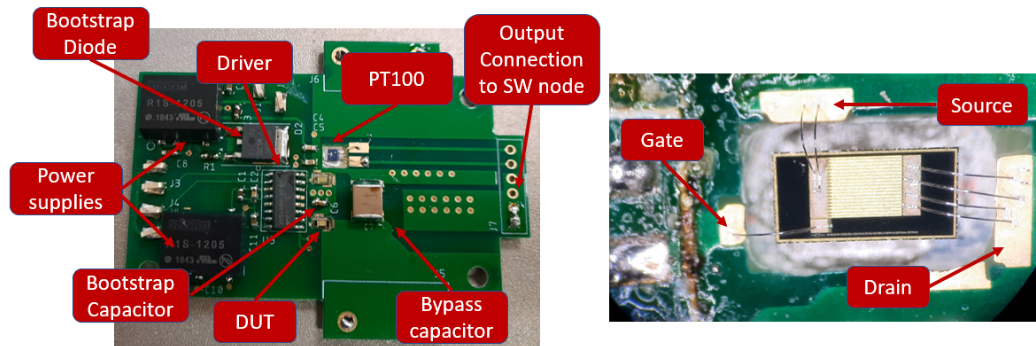
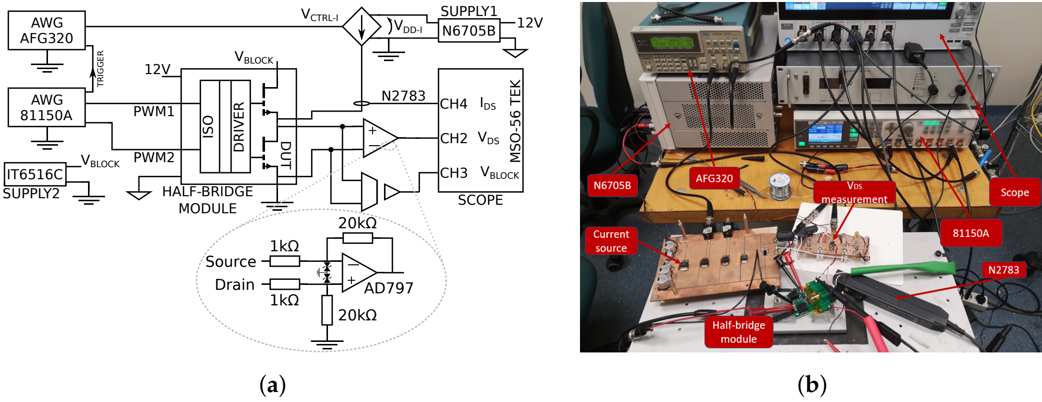


Figure 5. Photograph of the implemented half-bridge module with magnification of the die connections to FR4 board with wire bonding.

The FR4 board is populated with the SMD components, which are detailed in Figure 5. A high-side/low-side Si8273 isolated gate driver by Skyworks Solutions [32] is used to drive the GaN switches with $V_{GS,OFF}/V_{GS,ON}$ = 0 V/+5 V. The component guarantees 2.5 kV_{RMS} isolation, +1.8/−4 A forward/sink peak currents and very fast rise/fall times, which are ideal characteristics for GaN applications. The high-side driver configuration implements a diode-capacitor bootstrap circuit. The diode is a Schottky rectifier to reduce recovery time and withstand high blocking voltages [33], while $1uF$ is chosen as the bootstrap capacitance. It is noteworthy how the capacitance value could be selected to be ten times smaller for a typical design, given the very low gate charge of this device [34,35]; however, a bigger value was selected to sustain the high-side gate driving during the extended commutation periods used in the proposed characterization procedure described above. Two 1 W, 12 V–5 V low-ripple isolated DC/DC switching converters R1S-1205 by RECOM [36] were used to supply the first and second stages of the isolated gate driver. A 1 uF ceramic DC-link by-pass capacitor was placed close to the switching leg in parallel to the input voltage (V_{block}) to minimize the power loop stray inductance. The last component of the system is a PT100 thermistor directly placed on the IMS thanks to a third opening in the FR4 board. Even though the sensor is not very close to the switches, it provides a good temperature estimation, thanks to the wide aluminum substrate of IMS with high thermal conductivity.

4. Measurement Set-Up

As described in Section 2, the measurement of the dynamic R_{ON} implies the accurate sensing of the drain-source voltage V_{DS} and of the drain current I_{DS} during T_{ON}. As can be appreciated in Figure 5, the switching node of the half-bridge is easily accessible: at this node, the measuring current I_{DS} is injected, and V_{DS} is sensed, as described in the schematic of the set up in Figure 6a.



(**a**) (**b**)

Figure 6. Characterization set-up description. (**a**) Characterization set-up schematic; (**b**) photograph of the characterization set-up (IT6516C and isolated probe are not visible).

The measuring current I_{DS} is provided with a current source circuit already described in [31], made by two power Si P-MOS devices in cascode mode to maximize the generator output impedance. As described in [31], the current source is controlled with a ON/OFF command V_{CTRL-I}, while the current value I_{DS} is regulated by the value of the supply voltage V_{DD-I}. As observed before, it is important to regulate the amplitude and duration of the measuring current pulse in order to have a well-detectable V_{DS}, without inducing non-negligible self-heating to maintain isothermal conditions. The current value is measured by the Keysight high-bandwidth (100 MHz) Hall-effect probe N2783A with 1% accuracy. As described in Figure 6a, there are two different paths for the sensing of V_{DS}. One path with high dynamic range acquires the entire V_{DS} waveform along the period: in this path, an isolated active differential probe with 40 MHz bandwidth (Aaronia ADP1) is used to scale the V_{DS} waveform 100:1 to fit the oscilloscope voltage range. This channel is useful to monitor V_{block} during T_{block} and the synchronization with the measuring current, according to the measurement procedure described in Figures 1b and 2, but this acquisition does not

have enough sensitivity for a precise evaluation of V_{DS} during T_{ON} for the computation of R_{ON}. Thus, a second high-sensitivity and wide-band acquisition channel is implemented in a PCB visible in Figure 6b. In this channel, a low-offset and low-noise Analog Devices AD797 operational amplifier is used, in the $\times$20 voltage gain configuration described in the inset of Figure 6a. This acquisition channel enables the accurate characterization of V_{DS} waveforms during T_{ON} that are used for the computation of R_{ON}. Similar to that described in [31], with this configuration, the Op-Amp input is protected by means of two TVS diodes in anti-parallel configuration from high-voltage V_{block} during T_{block}. The presence of these didoes avoids the saturation of the oscilloscope acquisition channel and largely limits the saturation of the Op-Amp so that there are few µs after the blocking event, and the Op-Amp exits saturation and is capable of correctly measuring V_{DS}. The high-resolution Tektronix MSO-56 scope is used for the time-domain acquisition of waveforms. The control of the power module and of the current generator according to the measurement procedure is provided by two synchronized arbitrary waveform generators (AWG): Agilent 81150A and Tektronix AFG320. The first AWG generates the PWM signals for the half-bridge switching module, while the second controls the current source.

5. Measurements

The measurement procedure described in Section 2 is adopted with the described setup. The duration T_{block} of the blocking voltage V_{block} is initially set to 1 us. The dead time T_D is 500 ns. The value of the blocking voltage V_{block} is varied between 10 V and 400 V. The duration of the measuring window T_M is set to 40 µs. The amplitude of the current injected by the controlled current source is set to 0.45 A, guaranteeing isothermal tests, since the induced temperature increment due to self heating is estimated in ΔT = 0.22 °C. This is also confirmed by the flat I_{DS} shape during the entire measuring window T_M, which can be appreciated in the acquired waveforms (Figures 7 and 8). The distance ΔT_M is varied from 20 µs to 400 µs that, according to the consideration in Section 2, corresponds to an equivalent switching frequency $f_S = 1/\Delta T_M$ ranging from 50 kHz to 2.5 kHz. The acquired waveforms of the DUT V_{DS}, and I_{DS} for different blocking voltages are shown in Figure 7 for the acquisition at ΔT_M = 20 µs and in Figure 8 for the acquisitions with ΔT_M = 400 µs, respectively.

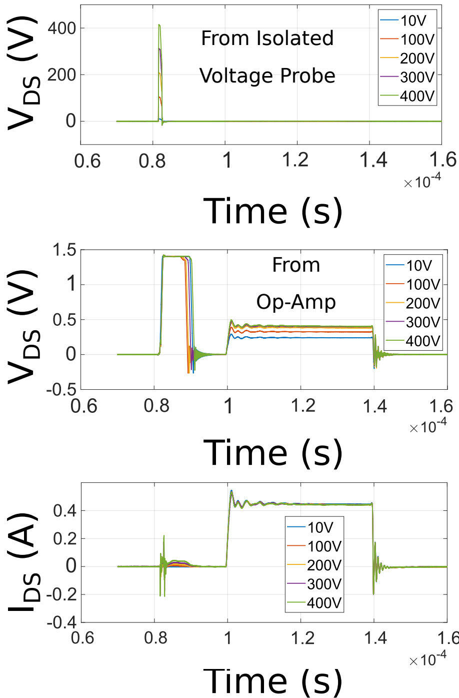


Figure 7. V_{DS} and I_{DS} DUT waveforms acquired by the scope for ΔT_M = 20 µs.

It can be observed that T_{block} saturates the Op-Amp of the accurate acquisition channel of V_{DS}, but after less than 10 µs, the Op-Amp exits saturation, and the measurement is available. The saturation of the Op-Amp and the presence of some residual ringing prevent the decrease of ΔT_M to lower values and thus directly observe R_{ON} for higher equivalent switching frequency. To this aim, the minimum ΔT_M can be reduced by a different selection of the Op-Amp. Nonetheless, observing the flat shapes of V_{DS} and I_{DS} pulses during T_M suggests that negligible recovery is observed up to 60 µs (i.e., $\Delta T_M + T_M$) from the V_{block} event. Therefore, it is safely possible to conclude that trap recovery is very slow and R_{ON} degradation is the same for application frequencies from 50 kHz upwards. This is an indirect, still reliable, indication that for this technology, the observed R_{ON} at 50 kHz is representative also for higher application frequencies.

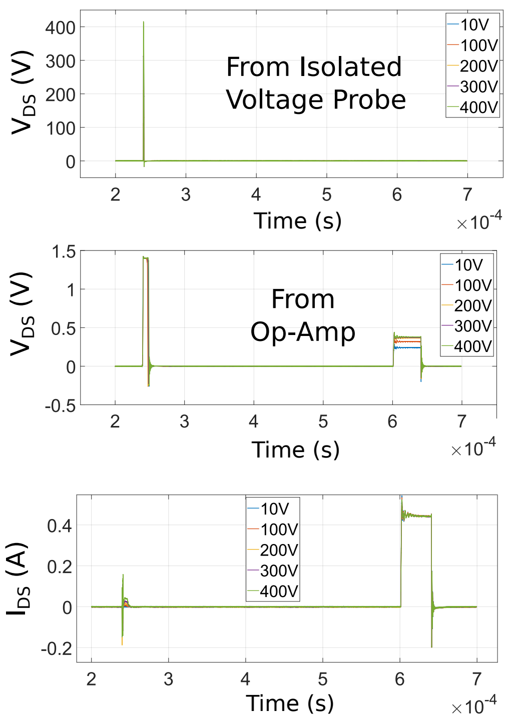


Figure 8. V_{DS} and I_{DS} DUT waveforms acquired by the scope for ΔT_M = 400 µs.

From waveforms as the ones described in Figures 7 and 8, $R_{ON} = V_{DS}/I_{DS}$ is computed for different ΔT_M. The trends of the R_{ON} as a function of the blocking voltage evaluated at ΔT_M = 20 µs, ΔT_M = 100 µs and ΔT_M = 400 µs are plotted in Figure 9, where the normalization factor is the value at V_{block} = 0 V for all cases. The observed degradation of the dynamic R_{ON} is relevant.

It is useful to recall (as suggested in Figure 9) that the corresponding application frequencies $f_S = 1/(\Delta T_M)$ are 50 kHz, 10 kHz and 2.5 kHz. Thus, since the target switching frequencies for high voltage GaN technology are typically in the range 50–500 kHz, the trap recovery does not give any beneficial effect to dynamic R_{ON} in the real application scenario. Therefore, the significant curve in Figure 9 is the one associated to ΔT_M = 20 µs/f_S = 50 kHz (green curve), and for the consideration made before about the practical absence of recovery in the window ΔT_M = 20–60 µs, this curve is the right reference also for higher switching frequencies. For this particular DUT, we can observe that the degradation of R_{ON} versus V_{block} appears to saturate after 300 V. The explanation of this behavior is not immediate and should be investigated with a physic-level insight that is outside the scope of this paper.

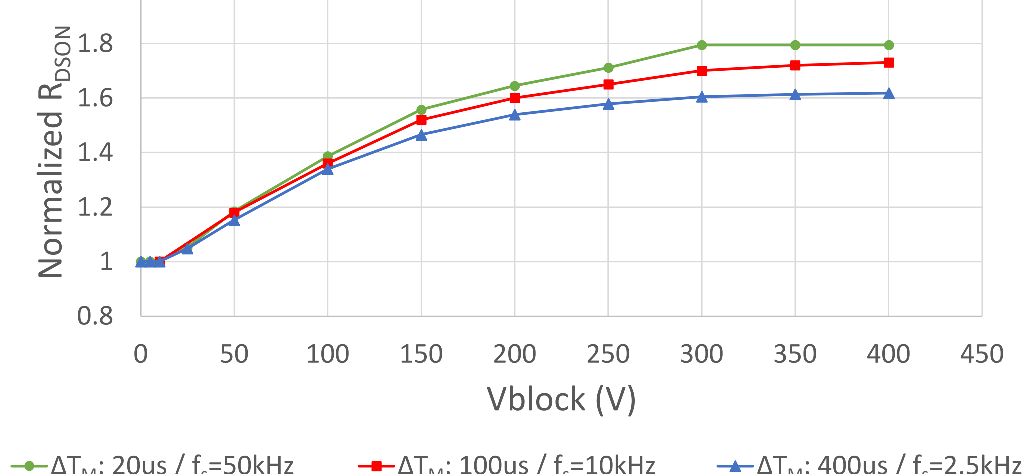


Figure 9. Normalized dynamic R_{ON} VS V_{block} evaluated at ΔT_M = 20 µs, ΔT_M = 100 µs and ΔT_M = 400 µs, with a T_{block} = 500 ns blocking voltage impulse.

The observed R_{ON} degradation is significant, with a maximum increase up to 80% with respect to the static value. This is quite typical for new GaN technologies under development, such as the one evaluated in this work, whereas more limited dynamic R_{ON} degradation can be observed for more mature commercial processes [18,29,30]. In this sense, the proposed technique can be a useful asset not only for the assessment of the performance of GaN transistor under operating regime, but also for the evaluation of the technological advances of a process under development.

Finally, Figure 10 describes the sensitivity of the dynamic R_{ON} to the duration T_{block} of the blocking voltage V_{block}. As expected, the effect is very limited and probably within the accuracy of the measurements. This corroborates the observation that the majority of charge-capture mechanisms are very fast.

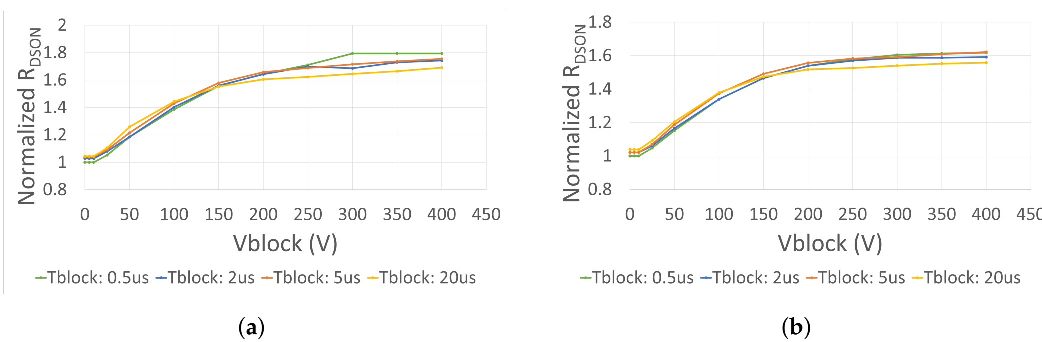


Figure 10. Normalized R_{ON} VS V_{block} evaluated in two distinct time instants ΔT_M. (**a**) R_{ON} at ΔT_M = 20 µs for different T_{block}; (**b**) R_{ON} at ΔT_M = 400 µs for different T_{block}.

All the measurements were performed at 30°C DUT temperature (it is the temperature of the IMS, which corresponds to the DUT temperature since the measurement is isothermal with practically zero ΔT temperature increase). By varying the IMS temperature, the same characterization can be made to determine the variation of the degradation of dynamic R_{ON} vs. temperature. Unfortunately, these data are not available since we did not have a proper thermal controlled carrier capable to house the power module. When performing the same measurements at increasing IMS/DUT temperature, we expect a slight improvement of RON performance, as observed in [31] for lower voltage technologies. Finally, it is interesting to note that the proposed set up is also suitable to work in different regimes with respect to the one exploited for this characterization. Thus, other tests on the DUT

dynamic R_{ON} can also be performed, forcing other conditions, such as hard/soft-switching, inductive load, double pulse, high-impedance, resonant-mode.

6. Conclusions

The Dynamic R_{ON} degradation of high-voltage GaN power transistors is a relevant topic that affects probably the most emerging semiconductor technology in the field of power electronics for automotive applications. The characterization of this phenomenon is a challenging research subject since it cannot be performed with standard techniques and instrumentation typically used for power transistor performance assessment. Indeed, static or small signal conductance measurement techniques cannot be applied, but unconventional non-linear dynamic approaches must be used. The main challenges associated with the set ups and measurement procedures are related to the need for a precise sensing of low-resistance values in the presence of fast commutations of high voltages.

Indeed, the most suitable method for the characterization of the dynamic R_{ON} of high-voltage GaN transistors is to measure this quantity during an operating regime of the DUT that resembles a real application scenario. For this reason, a measurement technique and a dedicated switching power module were developed and exploited for the characterization of bare-die 600 V GaN switches of a process under development. The measurements show a relevant degradation of R_{ON} that increases with the applied blocking voltage. This degradation fully applies to the entire range of switching frequencies of interests for this technology (i.e., >50 kHz). Indeed, due to the observed long time constants associated with trap-recovery mechanisms, a partial improvement of the dynamic R_{ON} is observed only for switching frequencies below 10–20 kHz, which are of very limited interest for this technology.

The proposed technique can be a useful method for the evaluation of high-voltage GaN switches' dynamic R_{ON} during a real application scenario.

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