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27-GHz Silicon-Integrated Rectenna Based on Novel Multilayer Substrate

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***Abstract*— This paper presents the design, fabrication, and characterization of a multi-layer 27-GHz rectenna integrated entirely on silicon, aimed at achieving full CMOS compatibility for energy harvesting applications. The device is fabricated on a high-resistivity silicon (HRSi) substrate, which is selectively etched to create a low-permittivity region for the antenna while maintaining a high-permittivity full substrate for the rectifier circuit. The rectenna, operating in the millimeter-wave (mmWave) band, features a compact single-cell design with dimensions of 13 x 13 mm² only, making it suitable for integrating IoT devices to support energy autonomy. The rectenna utilizes a GaAs diode rectifier and achieves a measured maximum RF-to-DC power conversion efficiency (PCE) of about 49% at an input power of 12 dBm. This work demonstrates the potential of HRSi-based, silicon-integrated rectennas for efficient energy harvesting in IoT applications. The proposed multilayer fabrication technology allows the realization of high-radiation-efficiency directive antennas and RF circuits directly onto the CMOS substrate, without increasing the overall size of the circuit and maintaining the structural integrity of the device.**

***Keywords*— Millimeter waves, rectennas, silicon integration, system on a chip.**

I. Introduction

With the advent of 5G communications and the resulting increase in radiofrequency (RF) devices, the mmWave spectrum has attracted significant interest for new applications such as Wireless Power Transfer (WPT) and Energy Harvesting (EH), which are usually exploited at lower frequencies [1]. The adoption of reduced wavelengths for rectenna design involves new challenges, such as the adoption of new topologies and technologies for antenna realization. Usually, rectennas operating in the mmWave spectrum adopt low permittivity and low losses commercial substrates such as Rogers, Duroid, etc [2],[3]. Utilizing the mmWave spectrum enables antenna miniaturization, facilitating the integration of the radiating element with digital baseband and/or RF modules. For this reason, CMOS solutions and fabrication technologies have triggered increasing interest in the last years [4]. However, on-chip antennas present limitations such as poor radiation efficiency and difficulties in the on-wafer measurements. The combination of a high permittivity and a thick substrate leads to the generation of surface waves, which significantly degrade the antenna’s radiation performance.

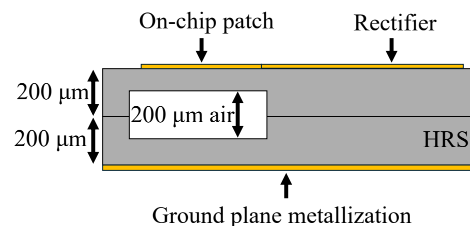

Fig. 1. Cross-section of the proposed multilayer silicon substrate. The patch antenna is deposited onto a synthesized low-permittivity region and is realized using selective etching of two 200-µm thick silicon wafers, while the rest of the circuit adopts a 400-µm thick Si-substrate.

Multiple on-chip antennas have been proposed for mmWave rectennas such as dipole and monopole antennas [5],[6], which are less affected by the silicon substrate. Anyway, these types of antennas, presenting low gain, may not be suitable for mmWave EH applications where high propagation losses and additional ambient attenuation are involved. For this reason, directive antennas can be adopted to maximize the amount of harvested power. Usually, on-chip patch antennas rely on hybrid integration with a silicon substrate, employing coupling structures [7] or a passivation layer based on silicon oxide (SiO_2) to reduce the effects of surface wave propagation [8],[9],[10],[11]. Despite these technologies effectively increasing the radiation efficiency of the patch, multiple materials or a precise oxide growth process is needed, increasing the complexity of the fabrication. The solution proposed here offers a novel technology for the fabrication of CMOS-integrated rectennas, adopting multiple layers of silicon substrate, which are etched and stacked together to enhance the radiation efficiency of mmWave rectennas. CMOS processing is a fabrication process that is used to make integrated circuit (IC) chips, such as digital logic circuits, analog circuits, and highly integrated transceivers. Using ion-implantation techniques, it is possible to deploy high-resistivity silicon (HRSi) wafers to create both active/nonlinear devices (e.g., diodes and amplifiers) and passive components (e.g., antennas, transmission lines, filters, etc.) on the same substrate, thus avoiding any hybrid integration.

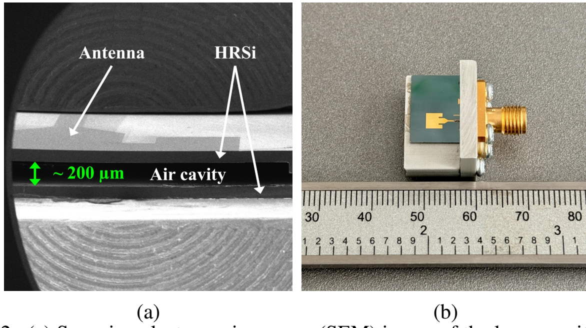

Fig. 2. (a) Scanning electron microscope (SEM) image of the low-permittivity region realized with the proposed multilayer Si-substrate, and (b) photo of the fabricated and assembled 27-GHz patch antenna.

The antenna, adopting the synthesized low-permittivity substrate, is first designed and manufactured, and then the rectenna at 27 GHz is tested in a free-space scenario. The proposed rectenna is based on a stacked topology to reduce the surface wave excitation of typical silicon-integrated rectennas, without the adoption of coupling structures and/or passivation layers. Moreover, the proposed rectenna presents measured PCE comparable to or higher than state-of-the-art Ka-band rectennas, which adopt traditional substrates [12] or multiple antenna systems to increase receiver gain [13].

II. 3D Design of the Multilayer Substrate

As anticipated, the adoption of silicon substrates, and in general, high-permittivity substrates, can be critical for the design and realization of antennas. For the proposed patch antenna operating at 27 GHz, a multilayer stacked structure, composed of two layers of HRSi (ε_r = 11.7), is chosen as the substrate. The engineered cross section of the multilayer structure, which includes the air cavity, is shown in Fig. 1. To realize the air cavity underneath the radiating element, two silicon wafers fabricated by Topsil are used. In particular, given the operating frequency of the proposed rectenna, only 200-µm thick wafers are considered. A selective etching of the two HRSi wafers was performed to create the synthesized low-permittivity region. From electromagnetic (EM) simulations, carried out in the CST Studio Suite, a 200-µm thick cavity is found to be the most promising for the realization of the rectenna. Cavity thickness values bigger than 200 µm are not investigated, to maintain the structural rigidity of the substrate, given the fragility of the chosen material. On the bottom wafer, a 250-nm thick titanium/gold metallization is adopted as a ground plane, whereas on the top of the upper wafer, the patch antenna and the rectifier circuit are configured. Through EM simulations, the patch antenna is simulated and tuned to work at the desired frequency. The fabrication of the prototype is divided into multiple stages: first, the metallization (Ti/Au, total thickness of 250 nm), is configured through a lift-off process. At the same time, another 250-nm thick Ti/Au metallization is deposited on the back of the second (bottom) wafer, this metallization being continuous and used as the reflector (ground plane) for the antenna (top circuitry). The low-permittivity area is realized by dry etching

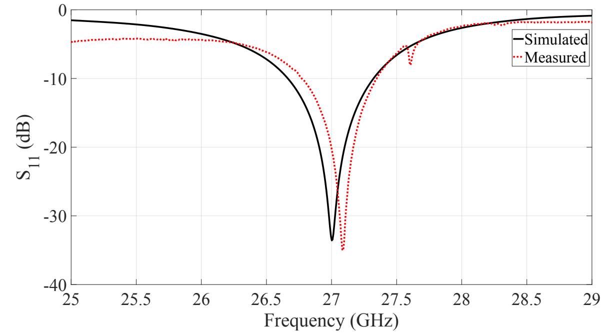

Fig. 3. Simulation and measurements of the antenna $|S_{11}|$ parameter in the 25÷29 GHz band. Measurements demonstrate good agreement with simulations with a 600 MHz 10-dB bandwidth.

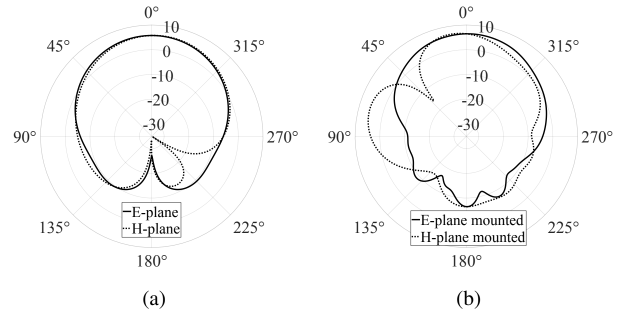

Fig. 4. (a) Simulated gain pattern of the 27-GHz on-chip antenna without (a) and with (b) the mounting support, on both E- and H-plane.

100 µm of silicon from each of the two wafers used. Finally, the two wafers are bonded one on top of the other, using a benzocyclobutene (BCB) layer for this purpose, so that the two cavities on the two separate wafers overlapped, thus forming the 200-µm thick cavity under the antenna. Fig. 2(a) shows the scanning electron microscope (SEM) image of the proposed multilayer substrate with the fabricated 200-µm thick air cavity, and in Fig. 2(b) the fabricated and assembled patch antenna, operating at 27 GHz, is reported. The total dimensions of the fabricated antenna are 3.32 x 3.32 mm^2. A 50-Ω input line is employed for the proposed antenna. Given that the low-permittivity region is etched exclusively near the radiating slots of the antenna, while the rest of the wafer remains filled with silicon, a tapered microstrip line is utilized for antenna feeding to ensure proper substrate transition matching. Measurements of the antenna $|S_{11}|$ parameter are carried out in the 25÷29 GHz band. Fig. 3 shows the comparison of the EM-simulated and the measured reflection coefficients. The measurements demonstrate a very good agreement with the simulations and a large 10-dB bandwidth (600 MHz). A 26 dB return loss is observed from the measurement at 27 GHz. Measurements of antenna gain are performed to validate the correctness of the design. As shown in Fig. 2, the assembled antenna presents a small metallic wall adopted as support for the connectors. The same wall is then adopted in the EM simulations to correctly represent the assembled antenna behavior. Fig. 4 shows the simulated gain patterns of the proposed on-chip antenna before and after the connection

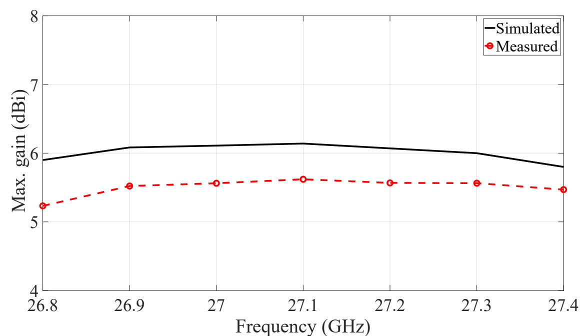

Fig. 5. Simulated and measured maximum gain on the E-plane, over the 10-dB bandwidth of the antenna. A good agreement is observed, with a measured gain of 5.6 dBi at 27 GHz.

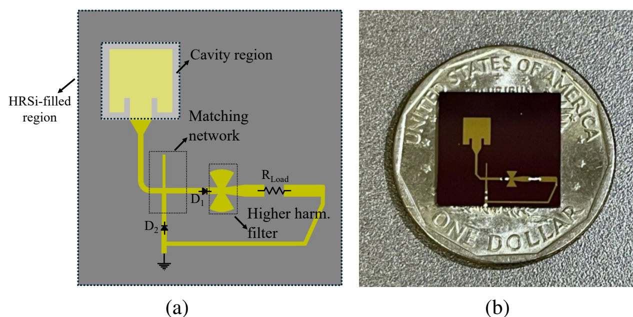

Fig. 6. (a) Layout of the proposed 27-GHz on-chip antenna based on the multilayer Si-substrate, and (b) photo of the fabricated rectenna prototype, compared to a one-dollar coin.

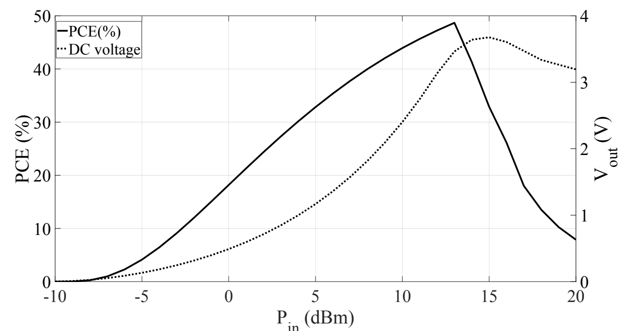

Fig. 7. HB-simulated PCE and DC output voltage in the -10÷20 dBm input power range for an optimized R_L = 1.3 kΩ load.

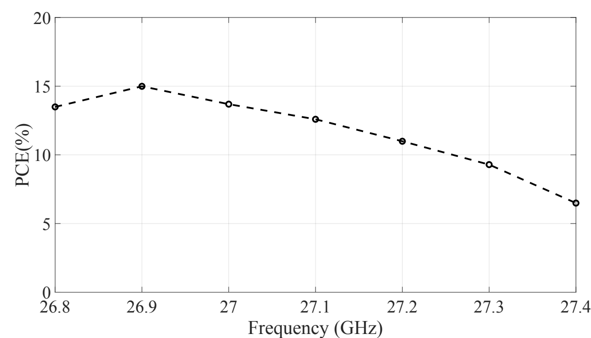

Fig. 8. Measured PCE over the 26.8÷27.4 GHz frequency band, for P_{in} = 0 dBm.

to the mounting structure. The simulations demonstrate that the proposed multilayer substrate does not significantly modify the radiation properties of the patch antenna, further validating the proposed concept. For measurement purposes, the mounting support has to be taken into account. As can be noticed in Fig. 4, a slight degradation of the gain patterns occurs for the mounted antenna (principally caused by the metal plate adopted as support), but keeping an optimal front-to-back ratio and the broadside radiation. Fig. 5 reports the comparison between the predicted and measured antenna maximum gain over the 10-dB bandwidth of reference, in the presence of the metal support. The measurements demonstrate a good agreement with the EM simulations over the entire frequency range. In particular, the measured gain is greater than 5.2 dBi over the entire 600-MHz antenna bandwidth. For brevity's sake, only the peak gain on the E-plane is shown.

III. Low-Permittivity Si-Substrate-Based Rectenna Design and Testing

For the rectenna design, a filled HRSi substrate hosts the rectifier circuitry. Given the high permittivity of the material, high miniaturization can be achieved. The rectifying circuit shares the same 400-μm thick multilayer substrate, with no air cavities. A voltage doubler configuration is adopted for the rectifier, to achieve higher DC output voltages for low-input power levels. GaAs diodes manufactured from MACOM (MA4E1317) are chosen for the proposed rectifier. A single open-stub network is adopted to realize conjugate matching between the rectifier complex input impedance and the 50-Ω patch antenna. Residual harmonics generated by the diode's nonlinearity are filtered out through a butterfly radial stub. The layout and photo of the proposed rectenna is shown in Fig. 6, where the low-permittivity region surrounding the antenna is highlighted. Harmonic Balance (HB) simulations are carried out to predict the performance of the rectenna in different input power conditions. Fig. 7 reports the rectenna PCE at 27 GHz, calculated as P_{DC}/P_{in}, where P_{DC} is the DC output power of the harvester, and P_{in} is the RF incident power on the rectenna, as computed in [14]. HB simulations of the rectenna DC output voltage, at 27 GHz, are reported on the right axis of Fig. 7. The maximum observed PCE (%) is about 49% when a 12-dBm input power (power received by the antenna) is present at the antenna. At the same input power level, 3 V are observed at the DC output port of the rectenna. Simulations are carried out with the optimized resistive load R_L = 1.3 kΩ. The fabrication of the harvester structures involved the use of two HRSi wafers, each of them with a thickness of 200 μm. On the first (top) wafer, the antenna structure was fabricated, together with the matching network and the circuitry for the rectifier. The total dimension of the fabricated rectenna is 13 x 13 mm^2. Firstly, fixed-input power measurements are performed to verify the actual rectenna operating frequency and DC load that maximizes the RF-to-DC conversion efficiency. Fig. 8 shows the measured PCE for an input power level equal to

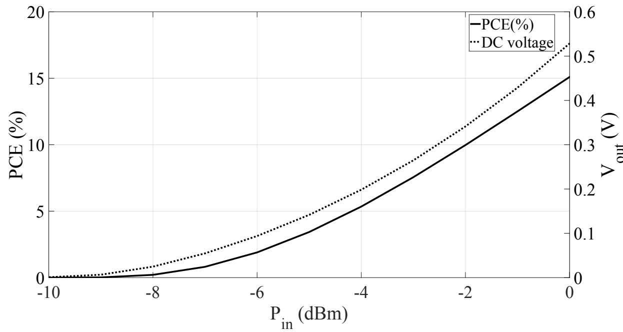

Fig. 9. Measured PCE and DC output voltage, in the -10÷0 dBm input power range, at 26.9 GHz and for R_L = 1.85 kΩ.

0 dBm, from 26.8 GHz to 27.4 GHz, which corresponds to the previously measured antenna bandwidth. Measurement of the PCE as a function of the DC load, which is not shown for brevity's sake, reports an optimal load of 1.85 kΩ, with a 550-Ω shift from the simulated one. This can be easily attributed to the diode model, whose circuit parameters may not be correctly extracted for the frequency of interest. For this reason, from now on, all measurements are carried out with the tuned DC load. The measurements shown in Fig. 7 indicate a 100-MHz detuning of the rectifying circuit, despite the actual operating frequency (26.9 GHz) differing from the simulated one (27 GHz) by only 1.5%. Measurement of the complete characteristic of PCE and DC output voltage as a function of the input power, are carried out at 26.9 GHz, and shown in Fig. 9. Given the limitation of free-space attenuation and available instrumentation, measurements of the PCE and of the DC output voltage are carried out in the -10÷0 dBm range of received available power. Measurements are in good agreement with simulations, showing a measured DC voltage of 515 mV and a 15% PCE for a 0-dBm received power.

IV. Conclusion

This paper presents novel topology and fabrication technology for the realization of silicon-integrated rectennas. A multilayer structure is proposed, in which a low-permittivity region is created underneath the radiating element, allowing one to overcome the poor radiation properties of on-chip patch antennas. The multilayer silicon substrate is first designed with EM simulations, and then fabricated by developing two separate solutions: a 27-GHz on-chip antenna and a 27-GHz integrated rectenna. The two prototypes are fully validated by an experimental campaign in which both the radiating properties of the antenna and the RF-to-DC conversion performance are verified. In particular, the rectenna shows a maximum conversion efficiency of 15% and a DC output voltage of 0.15 V at 0 dBm of received RF power, this performance being comparable or superior to the main state-of-the-art solutions in mmWaves that adopt GaAs diodes.

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References

[1] V. Palazzi, R. Correia, X. Gu, S. Hemour, K. Wu, A. Costanzo, D. Masotti, E. Fazzini, A. Georgiadis, H. Kazemi, R. Pereira, N. Shinohara, D. Schreurs, J.-C. Chiao, A. Takacs, D. Dragomirescu, and N. B. Carvalho, "Radiative wireless power transfer: Where we are and where we want to go," *IEEE Microwave Magazine*, vol. 24, no. 2, pp. 57–79, 2023.

[2] F. Deng and K. M. Luk, "A broadband high-gain multibeam ambient millimeter-wave energy-harvesting system," *IEEE Internet of Things Journal*, vol. 11, no. 3, pp. 4888–4898, Feb. 2024.

[3] C. Hannachi, S. Boumaiza, and S. O. Tatu, "A highly sensitive broadband rectenna for low power millimeter-wave energy harvesting applications," in *2018 IEEE Wireless Power Transfer Conference (WPTC)*, Montreal, QC, Canada, 2018, pp. 1–4.

[4] S. Trovarello, D. Masotti, M. Aldrigo, M. Modreanu, and A. Costanzo, "Design of a 24-ghz dual-polarized rectenna integrated on silicon," in *2021 51st European Microwave Conference (EuMC)*, London, United Kingdom, 2022, pp. 684–687,.

[5] M. Tabesh, N. Dolatsha, A. Arbabian, and A. M. Niknejad, "A power harvesting pad-less millimeter-sized radio," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 962–977, Mar. 2015.

[6] N. Weissman, S. Jameson, and E. Socher, "W-band cmos on-chip energy harvester and rectenna," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, Tampa, FL, USA, 2014, pp. 1–3,.

[7] O. Y. Kwon, C. Cui, J. S. Kim, J. H. Park, R. Song, and B. S. Kim, "A compact integration of a 77 ghz fmcw radar system using cmos transmitter and receiver adopting on-chip monopole feeder," *IEEE Access*, vol. 7, pp. 6746–6757, 2019.

[8] M. Sasaki, "Design of a millimeter-wave cmos radiation oscillator with an above-chip patch antenna," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 10, pp. 1128–1132, Oct. 2006.

[9] L. Jiang, J. F. Mao, and K. W. Leung, "A cmos uwb on-chip antenna with a mim capacitor loading amc," *IEEE Transactions on Electron Devices*, vol. 59, no. 6, pp. 1757–1764, Jun. 2012.

[10] H. S. Bakshi *et al.*, "Low-cost packaging of 300 ghz integrated circuits with an on-chip patch antenna," *IEEE Antennas and Wireless Propagation Letters*, vol. 18, no. 11, pp. 2444–2448, Nov. 2019.

[11] H. P. Phan, T. P. Vuong, G. Rehder, and C. A. Balanis, "60 ghz antennas on silicon with embedded cavity-backed structure," in *2014 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Memphis, TN, USA, 2014, pp. 99–100,.

[12] Y. Wang, X. X. Yang, G. N. Tan, and S. Gao, "Study on millimeter-wave siw rectenna and arrays with high conversion efficiency," *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 9, pp. 5503–5511, Sep. 2021.

[13] J. H. A. Eid and M. M. Tentzeris, "A scalable high-gain and large-beamwidth mm-wave harvesting approach for 5g-powered iot," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, Boston, MA, USA, 2019, pp. 1309–1312,.

[14] A. Costanzo, D. Masotti, M. Fantuzzi, and M. D. Prete, "Co-design strategies for energy-efficient uwb and uhf wireless systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 5, pp. 1852–1863, May 2017.