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Evaluation of AC Current Ripple in case of Split-Capacitor Three-Phase Four Wires Inverters

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***Abstract*— This paper deals with a split capacitor three-phase four-wire inverter, able to deal with unbalanced ac currents and/or voltages. The considered topology can be used in many applications such as photovoltaic systems, chargers for electrical vehicles, active filters, and in general all the grid-connected applications. One parameter that must be considered in the converter design is the ac (output) current ripple, which should be determined and minimized in order to improve the system efficiency. In this paper, the evaluation of the ac current ripple for the three-phase split-capacitor inverter is developed with reference to both balanced and unbalanced output conditions. In particular, the peak-to-peak and the rms current ripple are analytically determined as a function of the modulation index, for each phase. Initially, reference is made to single-carrier sinusoidal PWM, being, in general, a simple and effective solution. The interleaved multiple-carrier PWM strategy is then considered in order to mitigate the current ripple in the neutral wire, while not affecting its phase counterpart. Numerical simulations have been carried out in order to verify the analytical developments.**

Keywords—Split-capacitor, three-phase inverter, three-phase unbalanced systems, ac current ripple, inductor design.

I. Introduction

Three-phase four-wire (3P4W) voltage-source inverters (VSIs) have enabled many power applications involving unbalanced ac loads and ac sources. Thanks to their inherent capability to handle zero sequence components rather than the negative only, they have been employed in grid-forming inverters [1],[2], shunt active filters [3],[4], active rectifiers [5], renewable energy sources, and electric drives [6] applications. Moreover, it is worth noticing that the rising diffusion of electric vehicles enabled 3P4W inverters for providing vehicle-to-grid (V2G), vehicle-for-grid (V4G), vehicle-to-home (V2H), and vehicle-to-load (V2L) services in both three-phase and single-phase modes [7],[8]. Various neutral forming topologies such as three H-bridge [4],[9], split capacitors with [2],[4],[9],[10], and without [1],[3],[5] neutral inductor, four-leg with [3],[4],[9] and without [7],[11] neutral inductor, and independently controlled neutral module (ICNM) [2],[8],[12], have been proposed.

Carrier-based PWM schemes are widely employed in most of VSI applications because of their simplicity of implementation, in both digital and analog modes, and the well-known harmonic spectrum property [13]. Moreover, the fixed switching frequency makes switching losses control straightforward, and therefore more accurate converter design and losses computation can be achieved [14]. One of the most useful design parameters is the output current ripple, if precisely determined and optimized, it results on a system efficiency enhancement. In [14], the peak-to-peak current ripple in three-phase three-wire PWM inverters has been exhaustively analyzed and analytically described as a function of the modulation index. Furthermore, a ripple amplitude comparison for PWM inverters with different voltage levels was reported in [15]. In addition, the knowledge of the current ripple has been employed for a more precise compensation of the switches dead-time effects in VSIs [16]. Many papers deal with the analysis of the output current ripple in the three-phase three-wire topology. However, no analysis related to the split capacitor three-phase four-wire inverter has been reported in literature.

This paper aims to provide the analytical determination of the ac (output) current ripple in split capacitor three-phase four-wire VSIs in both balanced and unbalanced working conditions. Findings on peak-to-peak current ripple and its rms are reported as functions of the modulation index. Throughout the paper developments, comparisons and considerations with the three wires counterpart are provided. All the findings are reported considering the sinusoidal PWM (SPWM) because it is the only possible modulation in split capacitor three-phase four-wire VSIs.

Even though the three legs can be driven independently, the same fixed switching frequency has been considered for all the three carriers. However, a neutral current ripple mitigation attempt taking advantage of carriers shifting technique (popular in interleaved power converters) has been considered as well [5]. All the analytical developments are verified by numerical simulations carried out in the MATLAB/Simulink environment.

The paper is organized as follows. In Section II, the system configuration and the modulation principle are introduced. Section III presents the evaluation of the output current ripple in terms of peak-to-peak and rms values. A current ripple mitigation technique has been briefly discussed, pointing out its main features. In Section IV numerical verifications have been reported in case of balanced and unbalanced working conditions, and the conclusion is presented in Section V.

II. System Configuration

The circuit considered is represented in Fig. 1. It consists in a split-capacitor three-phase four-wire inverter supplying either a load or a grid. Compared with the three-phase three-wire inverter, a 4th wire is added to connect the midpoint of the dc-link capacitors to the neutral of the load/grid.

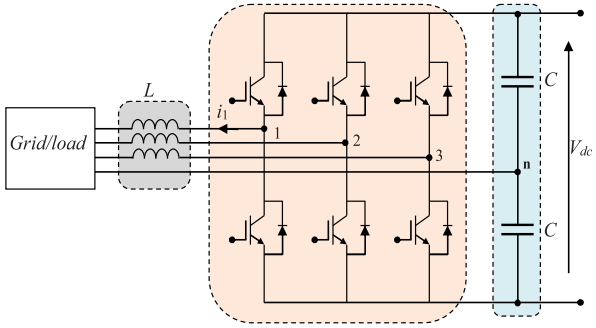

Fig. 1. Split capacitor three-phase four-wire inverter

For PWM-controlled inverters, considering sinusoidal modulation (SPWM) and within the linear modulation range, the averaged output voltages (over the switching period, $T_{sw}=1/f_{sw}$) correspond to the modulating signals scaled by a factor of V_{dc}:

$$\bar{v}_k = m_k\, V_{dc} \cos(\omega t - \varphi_k) = m_k\, V_{dc}\, \cos(\vartheta_k) \qquad (1)$$

where ω is the fundamental angular frequency, V_{dc} is the dc-link voltage source, m_k is the modulation index ($0 \le m_k \le 0.5$), φ_k is the phase angle, and $k = \{1, 2, 3\}$ is the phase index. For voltage balanced conditions: $m_1 = m_2 = m_3 = m$.

III. Evaluation of the Output Current Ripple

A. Evaluation of peak-to-peak current ripple

With reference to Fig. 1, the inverter output voltage can be written, for each phase k, as follows:

$$v_k(t) = R i_k(t) + L\frac{di_k(t)}{dt} + e_k(t) \qquad (2)$$

being R and L the resistance and the inductance of the ac-link inductor, i_k the ac output current, e_k the grid/load voltage.

By averaging (2) over the switching period T_{sw} gives:

$$\bar{v}_k = R\bar{i}_k + L\frac{d\bar{i}_k}{dt} + \bar{e}_k \qquad (3)$$

The instantaneous output current can be written as:

$$i_k(t) = \bar{i}_k + \hat{i}_k \qquad (4)$$

being $\bar{i}_k$ the averaged current component over the switching period, and the $\hat{i}_k$ switching current ripple component.

By replacing (4) in (2) and considering (3), the following equation is obtained:

$$v_k(t) = R\hat{i}_k + L\frac{d\hat{i}_k}{dt} + \bar{v}_k \qquad (5)$$

Neglecting the voltage drop across the resistance R, the current variation in the sub-period [0, t], can be calculated from (5) as:

$$\hat{i}_k = \frac{1}{L}\int_0^t [v_k(t) - \bar{v}_k]dt = \frac{1}{L}\int_0^t \hat{v}_k\, dt \qquad (6)$$

For the split capacitor inverter, there are two possible output voltage levels, i.e. $\pm V_{dc}/2$. In this case, the current ripple has a simple triangular profile.

Since the three-phase are independent in the case of the considered topology, the same expression of the output current ripple can be used in case balanced condition as well as in the unbalanced condition.

Considering the sinusoidal PWM principle, the "on-time" interval for each phase, t_{on}^k, is calculated as:

$$t_{on}^k = \left(\frac{1}{2} + m_k \cos\vartheta_k\right) T_{sw} \qquad (7)$$

Based on (1) and (6), the excursion of the current within the time interval (7) is:

$$\hat{i}_{pp}^k = \frac{1}{L}\left[\frac{V_{dc}}{2} - m_k\, V_{dc}\cos(\vartheta_k)\right] t_{on}^k \qquad (8)$$

corresponding to the peak-to-peak current ripple.

By introducing (7) in (8), the current ripple becomes:

$$\hat{i}_{pp}^k = \frac{V_{dc}}{f_{sw}L}\left[\frac{1}{4} - m_k{}^2\cos^2(\vartheta_k)\right] = \frac{V_{dc}}{f_{sw}L}\hat{r}_{pp}^k \qquad (9)$$

being $\hat{r}_{pp}^k$ the normalized peak-to-peak current ripple:

$$\hat{r}_{pp}^k = \frac{1}{4} - m_k{}^2\cos^2(\vartheta_k) \qquad (10)$$

Fig. 2. shows the distribution of the normalized peak-to-peak current ripple, given by (10), in the case of split-capacitor three-phase four-wire inverter for different values of modulation index m, in the phase angle range [0°,180°].

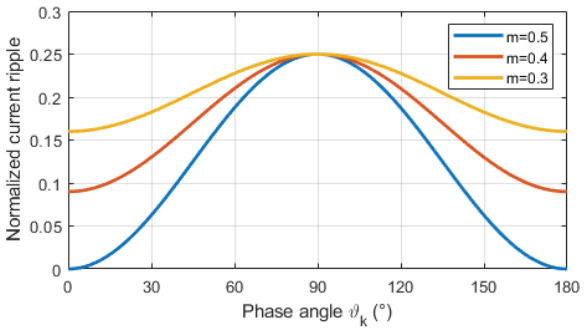

Fig. 2. Normalized current ripple for three modulation indexes, m = 0.3 (yellow), m = 0.4 (red), and m = 0.5 (blue), for phase angles [0°, 180°].

As it can be seen in Fig. 2, the maximum normalized current ripple occurs when $\vartheta = 90°$ and it is always equal to 0.25.

In order to compare the three wires VSI with the considered split capacitor four wires configuration, the maximum current ripple for both topologies are shown in Fig. 3 as a function of m. Reference is made to the system parameters given in Table I. A balanced case is considered.

It can be noticed that the maximum of peak-to-peak current ripple in case of three wires topology increases with the

modulation index. However, in case of split capacitor four-wire inverter the maximum is always constant and independent from the modulation index.

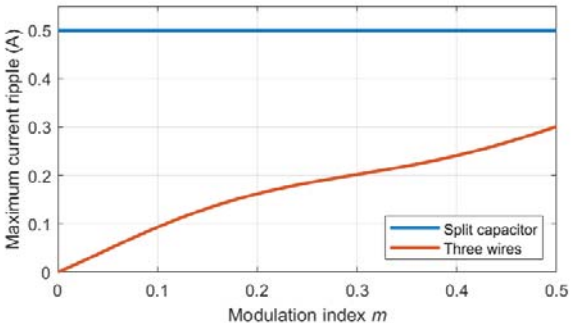

Fig. 3. Max peak-to-peak current ripple vs. modulation index in case of three wires and four wires split capacitor three-phase inverters (balanced).

B. *Evaluation of current ripple rms*

Based on previous discussion, the instantaneous current ripple is a triangular waveform with the peak-to-peak value determined by (9), valid for both balanced and unbalanced conditions. Knowing that the crest factor of a triangular waveform is √3, the rms over half of the fundamental period is calculated as

$$\hat{I}_{rms}^{k} = \sqrt{\frac{1}{\pi}\int_{0}^{\pi} \hat{i}_k^{\,2} d\vartheta} = \frac{1}{\sqrt{3}} \sqrt{\frac{1}{\pi}\int_{0}^{\pi} \left(\frac{\hat{i}_{pp}^{k}}{2}\right)^2 d\vartheta} \tag{11}$$

Replacing (9) in (11) and integrating leads to:

$$\hat{I}_{rms}^{k} = \frac{V_{dc}}{8\sqrt{3} f_{sw} L} \sqrt{6 m_k^{\,4} - 4 m_k^{\,2} + 1} \tag{12}$$

As shown in Fig. 4, there is a perfect matching between the current ripple rms obtained by numerical simulations and the value analytically calculated by (12) employing data of Table I.

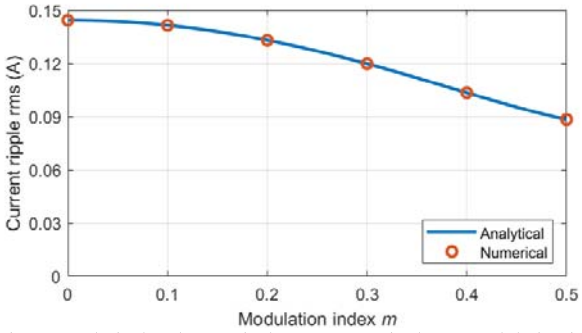

Fig. 4. Analytical and numerical rms current ripple vs. modulation index for split capacitor four-wire inverter.

Fig. 5 shows the current ripple rms in case of three-phase three wires inverter compared to the rms current ripple rms of the considered three-phase four wire split capacitor inverter. It can be noticed that the rms in case of the three wires inverter is almost a linear function of the modulation index. However, the rms in case of four-wire split capacitor inverter is higher for lower modulation indexes and it decreases by increasing the modulation index. At $m = 0.5$, the rms current ripple in case of four wires split capacitor inverter is almost the double of the rms current ripple in case of three wires inverter.

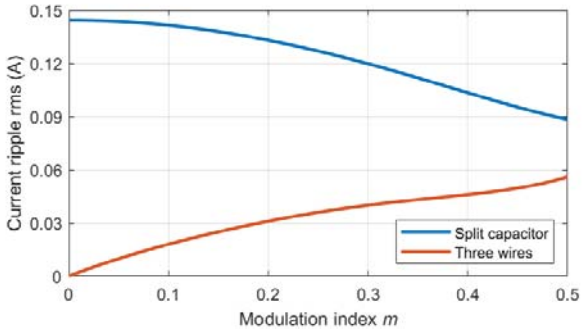

Fig. 5. Rms current ripple vs. modulation index in case of three wires and four wires split capacitor three-phase inverters (balanced).

For this reason, and in order to reduce the output current ripple, it would be more convenient to use the split capacitor four wires topology only in case of unbalanced working conditions. In case of balanced currents, the normal three wires inverter converter should be always used. It's important to underline that the calculation of the maximum current ripple as well as the rms current ripple for each phase in case of the split capacitor four wires topology is valid for both balanced and unbalanced conditions.

C. *Mitigation of neutral current ripple*

In the basic implementation, the modulating signals (1) and a single triangular carrier for all the three phases are adopted for the split-capacitor four wires inverter.

As mentioned in the previous section, the three phases of the considered topology are completely independent due to the four wires connection. For this reason, one possibility to achieve lower neutral current ripple and/or to mitigate the neutral current ripple is to introduce three interleaves carriers [5], i.e. to use three evenly shifted carriers, one for each inverter phase, without affecting the output voltage levels. The results of the neutral current ripple are shown in the next section in both balanced and unbalanced conditions.

IV. Numerical Results

In order to verify the theoretical developments shown in previous sections, numerical simulations are carried out by Matlab/Simulink considering split-capacitor three-phase inverter connected to an RLC load with unity power factor (grid emulation) with parameters shown in Table I.

As an example, Fig. 6 shows output voltage and current waveforms of phase 1 in case $m_1 = 0.3$, $m_2 = 0.4$, and $m_3 = 0.5$. As expected, the output voltage switches between $\pm V_{dc}/2$ (± 50 V) and the output current is sinusoidal.

TABLE I
SIMULATION CIRCUIT PARAMETERS

Label	Description	Parameters
V_{dc}	dc voltage supply	100 V
C	dc-link split capacitance (2x)	1 mF
R , L	ac-link filter reactor (series RL)	3.16 Ω, 20.1 mH
R_o,C_o	equivalent grid (parallel RC)	20 Ω, 58 µF
f	fundamental frequency	50 Hz
f_{sw}	switching frequency	2.4 kHz

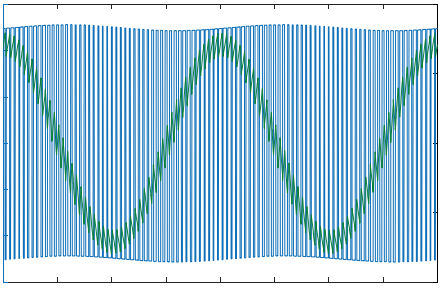

Fig. 6. Instantaneous output voltage (blue trace) and current (green trace) of phase 1 in case of unbalance: $m_1 = 0.3$, $m_2 = 0.4$ and $m_3 = 0.5$.

With reference to the same case reported in Fig. 6, Fig. 7 shows the three instantaneous output currents together with the upper/lower ripple envelopes analytically calculated considering $m_1 = 0.3$, $m_2 = 0.4$, and $m_3 = 0.5$. Fig. 8 shows, for each phase, the details of the current ripple with the corresponding peak-to-peak envelopes obtained by (9). As expected, the matching is satisfactory and the same equation (9) can be used for all the phases just introducing a different modulation index.

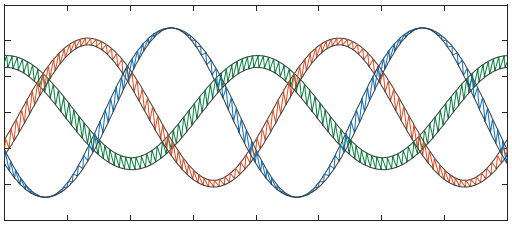

Fig. 7. Instantaneous phase currents with calculated current envelopes (pink) in case of m_1 =0.3 (green), m_2 =0.4 (orange) and m_3 = 0.5 (blue).

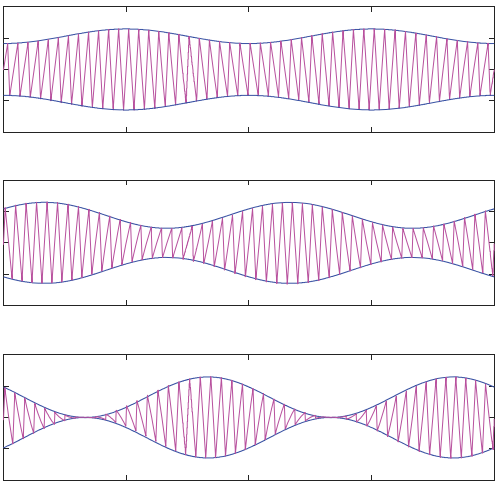

Fig. 8. Current ripple (pink) and calculated envelope (blue) for phase 1 (upper), phase 2 (middle) and phase 3 (lower), reference to Fig. 7.

The following simulations concern the current ripple on the 4th (neutral) wire in case of balanced and unbalanced working conditions.

Fig. 9 shows the neutral current in the balanced case $m_1 = m_2 = m_3 = 0.4$. The PWM logic has been implemented by a single carrier for all the three phases (red trace) and by three interleaved carriers (blue trace). As expected, the benefit of interleaving carriers is evident, leading to a mitigation of the current ripple (approx. 50%) without any drawback.

Fig. 10 shows the neutral current in the unbalanced case $m_1 = 0.3$, $m_2 = 0.4$, and $m_3 = 0.5$. Also in this case, the PWM logic has been implemented by a single carrier for all the three phases (red trace) and by three interleaved carriers (blue trace). Despite to the unavoidable 50 Hz current component due to the unbalance (the amplitude is approx. 0.8 A), the benefit of interleaving carriers is still evident, leading to a mitigation of the current switching ripple (lower than the half) without any drawback.

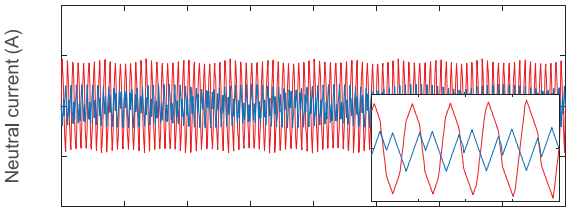

Fig. 9. Neutral current in case of single carrier (red trace) and interleaving three carriers (blue trace) in case of $m_1 = m_2 = m_3 = 0.4$, with zoom.

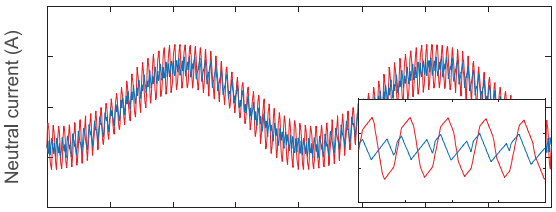

Fig. 10. Neutral current in case of single carrier (red trace) and interleaving three carriers (blue trace) in case of m_1=0.3, m_2=0.4 and m_3=0.5, with zoom.

V. Conclusion

In this paper, the analysis of the instantaneous ac output current ripple for three-phase four-wire split-capacitor inverters has been developed in detail. In particular, the peak-to-peak current ripple has been analytically derived in the whole fundamental period as function of the modulation index for both balanced and unbalanced working conditions.

Furthermore, basing on the peak-to-peak ripple envelope, the maximum and the rms current ripple have been easily obtained. It has been pointed out that maximum peak-to-peak current ripple is constant in all the range of the modulation index. The expression of peak-to-peak current ripple is valid for each phase despite balanced or unbalanced working conditions, since the three phases are independent.

In addition, interleaving the three carriers in the PWM logic has been considered and successfully verified in order to mitigate the current switching ripple on the neutral wire.

The analytical developments have been numerically verified by implementing a realistic circuit model with MATLAB/Simulink, with reference to some relevant cases.

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