IEEE Open Journal of
Power Electronics

Received 1 July 2026; revised 7 August 2026; accepted 15 August 2026. Date of publication 18 August 2026;
date of current version 3 September 2026. The review of this article was arranged by Associate Editor Liangzong He.

Digital Object Identifier 10.1109/OJPEL.2026.3725035

A Variation-Tolerant 1.25-MHz Multi-Resonant GaN Switched-Capacitor DC/DC Converter

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ABSTRACT Minimizing the size of passive components in DC/DC converters often leads to higher switching frequencies and losses. Resonant Switched Capacitor Converters (ReSCCs) mitigate losses by incorporating a flying LC tank and zero-current switching, but their efficiency is sensitive to component variations. To address this limitation, Multi-Resonant Switched Capacitor Converters (MuReSCCs) introduce a second resonance loop to preserve energy during switching. This paper presents the design and validation of a 48 V-to-lower-voltage MuReSCC, with a particular focus on robustness against variations in component parameters. A complete implementation of the power converter is proposed, supported by analytical models and design guidelines. Moreover, on-off control for output voltage regulation is implemented, and its impact on efficiency is investigated. Unlike previous works, this study targets operation at switching frequencies above 1 MHz through Gallium Nitride (GaN) devices and a planar printed circuit board (PCB) inductor. Experimental results, supported by theoretical models, demonstrate a peak efficiency above 98.9% at 45 W and a maximum observed output power of 200 W, with an efficiency of 94%. The immunity to variations in component parameters is experimentally verified. The efficiency of the MuReSCC decreases by less than 1% for deviations of up to ± 30% in resonant component values.

INDEX TERMS DC-DC power converters, resonant converters, voltage regulators, wide-bandgap semiconductors.

I. INTRODUCTION

Electronic power conversion aims to reduce the physical size of power converters and to improve their performance and energy efficiency. High efficiency is crucial, since it extends the operating life of battery-powered devices. Moreover, reliability is a critical factor to consider in power converter design [1]. In this context, a key metric is power density, defined as the amount of power converted per unit volume. Maximizing power density is essential to reduce operational costs, minimize converter dimensions, and meet today's and future integration challenges. Frequently, a significant portion of the volume in power converters is occupied by passive components, particularly inductors. One common strategy to reduce inductor size is to increase the operating frequency. However, this results in higher material costs for inductors and, more importantly, increased switching losses in power transistors [2]. These losses can be addressed primarily through technology advancements (e.g., by adopting wide-bandgap semiconductor devices) or through innovation in circuit topologies. In this sense, Series Inductor Converters (SICs) are among the most widely adopted topologies [3]. However, they typically require high inductance values and consequently larger volumes. Recent trends in SICs aim to increase the switching frequency [4], [5] to reduce the size of magnetic components. Yet, despite these efforts, inductor size still remains a limitation. In contrast, Switched-Capacitor Converters (SCCs) [6], [7] entirely eliminate inductors. Switched-capacitor converters (SCCs) can achieve higher energy storage density in their passive components than inductor-based converters, as capacitors typically store more energy per unit volume. However, SCCs face two main efficiency challenges. First, inherent charge redistribution between capacitors during normal switching operation results in energy losses, which limit overall efficiency [7]. To compensate, SCCs

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TABLE 1. Summary Comparison of Related Converter Topologies

Topology	Peak Efficiency	f_{sw}	Max reported P_{out}	V_{out}	Passives volume	Power Density	Reference
ReSCC/MuReSCC 2:1	98.9%	1.25 MHz	200 W	24-48 V	$380mm^3$	$0.53\,W/mm^3$	This work
Double mode SCC	92%	200 kHz	350 W	50-100 V	n.a.	n.a.	[11]
Multi-resonant Cascaded SCC	98.6%	50 kHz	400 W	6-48 V	$3076mm^3$	$0.13\,W/mm^3$	[15]
4x Serial-Parallel ReSCC	n.a.	100 kHz	100 W	n.a.	n.a.	n.a.	[13] [14]
MuReSCC 4:1	98.6%	200 kHz	500 W	20-30 V	$720mm^3$	$0.69\,W/mm^3$	[17]
4:1 Multilevel STC	98.92%	320 kHz	650 W	9-15 V	$830mm^3$	$0.78\,W/mm^3$	[16]
MuReSCC + Buck	97.9%	500 kHz	1.5 kW	12 V	n.a.	n.a.	[18]
Synchronous High-frequency GaN Buck	97.5%	400 kHz	400 W	40 V	$1400mm^3$	$0.29\,W/mm^3$	[4]
High-frequency Bidirectional GaN Buck-Boost	94.4%	10 MHz	100 W	30-60 V	$1800mm^3$	$0.06\,W/mm^3$	[5]
Cascaded Buck-Boost with auxiliary capacitor	98%	45 kHz	16-160 W	80-300 V	n.a.	n.a.	[19]
ReSCC with output inductance	98.7%	74 kHz	480 W	24 V	$2110mm^3$	$0.23\,W/mm^3$	[20]
Dickson 4:1 SCC	98.5%	100 kHz	420 W	12 V	n.a.	n.a.	[21]

are often operated at higher switching frequencies, but this approach increases switching losses and can affect efficiency gains. Second, when the converter is controlled to achieve an output-to-input voltage ratio different from that inherently provided by its topology, additional energy is dissipated due to partial charge transfers, further reducing efficiency.

One approach to overcome these limitations involves the class of Hybrid Converters (HCs), which combine the benefits of SCCs with the reintroduction of an inductor [8], albeit with significantly lower inductance and size compared to traditional SICs. The inductor [9] reduces or completely eliminates losses caused by direct charge redistribution between capacitors at different voltages, as occurs in SCCs. In HCs, the employed inductance has a much smaller value than in SICs [10], thereby combining the advantages of SICs (i.e., current limitation and absence of voltage discontinuities) with those of SCCs. Furthermore, by exploiting LC-tank circuits, the capacitors can be fully utilized, increasing energy density compared to both SICs and SCCs. Among HCs, Resonant Switched-Capacitor Converters (ReSCCs) [11], [12] [13], [14] [15] adopt an LC resonance loop to achieve soft charging. Zero-Current Switching (ZCS) is achieved by operating the converter at the same resonance frequency as the inductor-capacitance series. However, losses still increase when the switching frequency deviates from the actual resonance, which can occur due to component tolerances and aging. To address this issue, [16] proposes a Switched-Tank Converter (STC) that employs Class-1 capacitors with minimal tolerance ($<5\%$) in series with the inductor, enabling both soft charging and soft switching. In [17], an innovative approach proposes Multi-Resonant Switched-Capacitor Converters (MuReSCCs), which add a second resonance loop to the ReSCC by placing a capacitance in parallel with the inductor to achieve Zero-Voltage Switching (ZVS). The second resonance loop acts as an energy buffer, preserving energy in the presence of residual inductor current and automatically releasing it to the output. As a result, a precise match between the resonant and switching frequencies is not strictly required.

In ReSCCs, the resonant inductor shapes the current waveform into a quasi-sinusoidal form, which reduces the RMS current through the switches while maintaining the same average current in the slow-switching limit (SSL) region [9]. Compared to a conventional SC converter, an ReSCC can achieve the same power delivery at a lower operating frequency. Many resonant converter variants exist, as shown in Table 1, with at least one for each class of switched capacitor topology [21]. These include converters with output inductance [20], internal inductance [17], and resonant topologies merged with classic SICs [18] to overcome the complexity of the control system in resonant converters.

This work builds upon the initial proposal of MuReSCC [17], extending the study to address system-level design considerations. In particular, compared to [17], this work investigates the benefits of operating at higher, above-megahertz switching frequencies and integrating wide-bandgap power switches, with the goal of further reducing the volume of passive components and minimizing losses. Furthermore, this work introduces a fully autonomous system architecture that incorporates an on-off closed-loop control scheme, along with an investigation of its impact on power conversion efficiency. As an additional contribution, the robustness of MuReSCC is extensively evaluated under parameter and frequency variations and compared against ReSCC, with the support of experimental measurements. In a previous conference paper [22], only the main power stage was introduced in an open-loop configuration with fixed-output power measurements. Compared with [22], this paper introduces and evaluates closed-loop control and presents high-power and variable-load measurements in both open- and closed-loop configurations.

This paper is structured as follows: Section II introduces hybrid switched-capacitor converters and compares ReSCC and MuReSCC, focusing on the 2:1 open-loop topology and basic operating principles. Section III discusses the design process, followed by Section IV, which presents the MuReSCC prototype. Section V discusses the experimental results. Finally, Section VI concludes the paper.

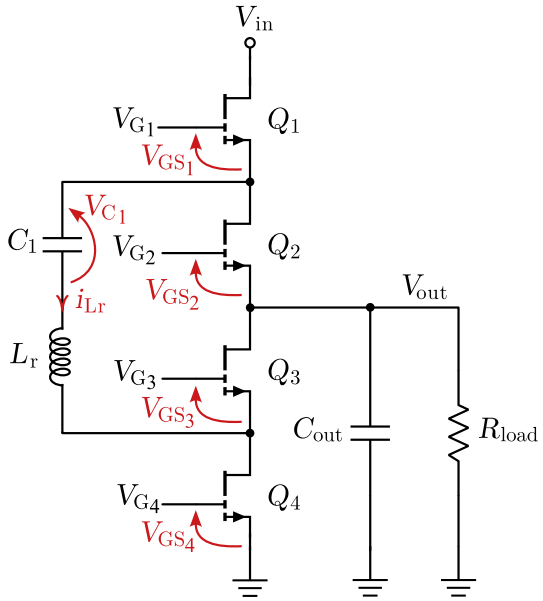

FIGURE 1. Schematic of a 2:1 Resonant Switched-Capacitor Converter (ReSCC).

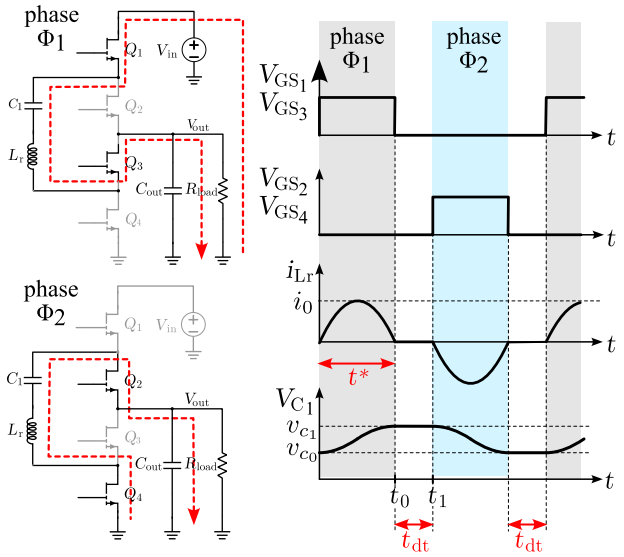

FIGURE 2. ReSCC control scheme, with phases and current loops highlighted.

II. ANALYSIS OF RESCCS AND MURESCCS

A. RESONANT SWITCHED-CAPACITOR CONVERTERS (RESCC)

The ReSCC topology was introduced by Shoyama et al. in [12] and is designed to reduce conduction losses arising from charge redistribution by inserting a series inductor into a 2:1 series–parallel switched-capacitor converter. A schematic of a ReSCC employing enhancement-mode GaN high-electron-mobility transistors (HEMTs) is shown in Fig. 1, where it is assumed that $C_1 \ll C_{out}$. In this converter, C_1 and L_r replace the flying capacitor used in conventional SCCs, thereby forming a flying LC tank. In open-loop operation, two non-overlapping switching phases are applied, as illustrated in Fig. 2:

- *Phase* Φ_1*:* Q_1 and Q_3 are turned on, charging the LC tank to the output.
- *Phase* Φ_2*:* Q_2 and Q_4 are turned on, discharging the LC tank back to the output.

Each phase starts and ends with a zero inductor current, and a dead-time $t_{dt} = t_1 - t_0$ is applied between phases to prevent cross-conduction.

Due to the natural resonance of the tank, the inductor current exhibits a weakly damped sinusoidal waveform with oscillation period

$$\tau = \frac{2\pi}{\sqrt{\left(\frac{1}{L_r C_1}\right)^2 - \left(\frac{R}{2L_r}\right)^2}} \approx 2\pi\sqrt{L_r C_1}, \tag{1}$$

where R is the resistance associated with the involved current loops. This approximation is valid when $\frac{2L_r}{R} \gg \sqrt{L_r C_1}$, which is a reasonable assumption for component sizing to minimize losses. To achieve ZCS, the switching frequency f_{sw} must match the resonance frequency $f_{res} = 1/\tau$, thus

$$f_{sw} = f_{res} = \frac{1}{2\pi\sqrt{L_r C_1}} \tag{2}$$

In case of mismatch between resonant frequency and switching frequency, two scenarios arise:

- Switching occurs too early ($f_{res} < f_{sw}$): the current in the LC tank has not yet reached zero.
- Switching occurs too late ($f_{res} > f_{sw}$): the current in the LC tank has already reversed its direction.

Besides production-related parameter variations, component values may also drift over time due to temperature fluctuations or aging. Hence, zero-current detectors may be used to control phase transitions and maintain a continuous alignment with the actual resonant frequency [23]. However, this strategy either increases the component count or, in the case of integrated converters, the required silicon area. Moreover, at high operating frequencies, the power consumption of the active detection circuitry becomes non-negligible, and comparator delays may compromise ZCS. This limitation is instead addressed at the topology level by the MuReSCC, which is described in the following paragraph.

B. MULTI-RESONANT SWITCHED CAPACITOR CONVERTERS (MURESCC)

Unlike the ReSCC, the MuReSCC (Fig. 3) is designed to operate at a switching frequency f_{sw} slightly higher than the resonance frequency f_{res}, which mainly depends on L_r and C_1. However, no precise or fine control of the switching frequency is necessary, since the MuReSCC inherently maintains immunity to parameter variations.

Let us assume in particular

$$f_{\mathrm{sw}} \triangleq k f_{\mathrm{res}}, \tag{3}$$

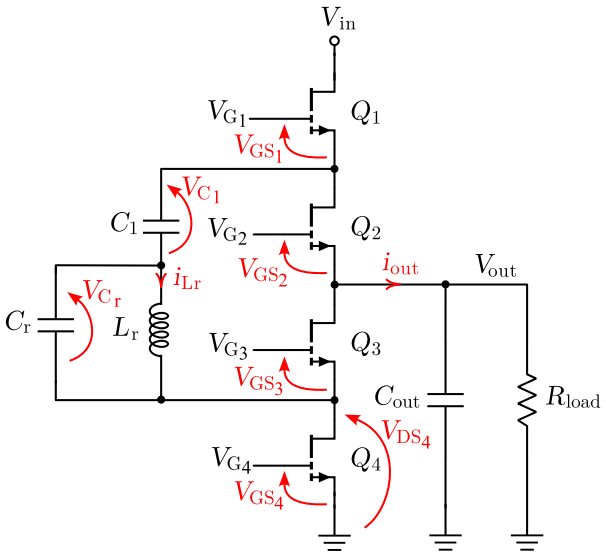

FIGURE 3. Schematic of a 2:1 Multi-Resonant Switched-Capacitor Converter (MuReSCC).

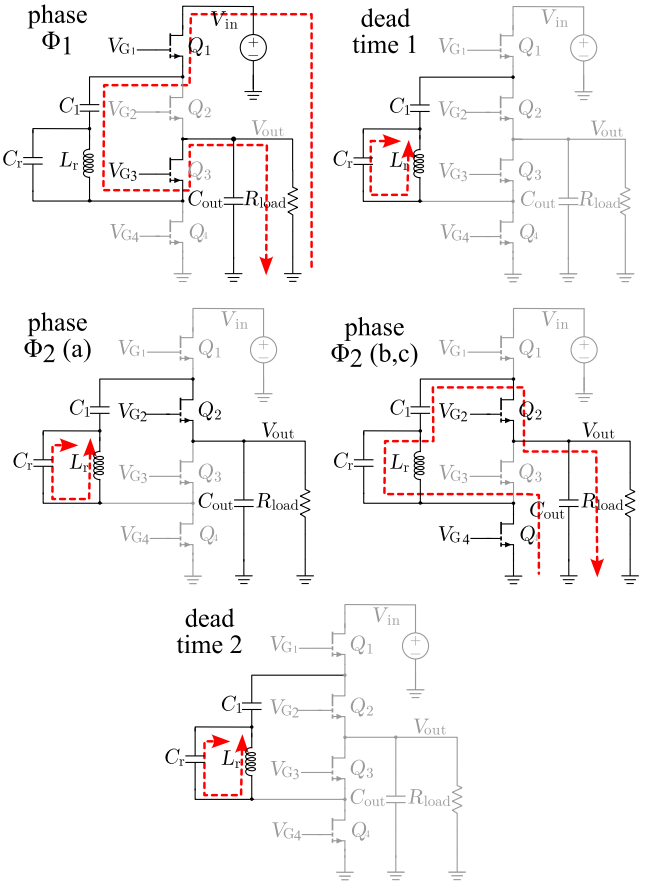

FIGURE 4. MuReSCC control scheme, with phases and current loops highlighted.

where $k > 1$ is the immunity factor, which ensures a margin in case the actual resonance frequency drifts above the expected value. The secondary resonance frequency f'_{res} of L_r and C_r is chosen such that $f'_{\text{res}} \gg f_{\text{res}}$ so that the two resonance loops operate independently.

The converter control scheme is depicted in Fig. 4, while Fig. 5 reports relevant circuit voltages and currents. The control sequence can be divided in two phases, separated by dead times. In the first phase (Phase Φ_1, $t_0 < t < t_1$), as in the single-resonant converter, Q_1 and Q_3 are activated, charging the L_rC_1 tank and the output capacitor C_{out}. Phase Φ_1 is followed by a first dead time t_{dt} ($t_1 < t < t_2$), during which all switches are turned off. However, since $f_{\text{sw}} > f_{\text{res}}$, a residual current remains in the inductor L_r at the beginning of t_{dt}. Due to the insertion of capacitance C_r, the residual current i_{Lr} in the inductor starts flowing into the capacitor, and the secondary loop L_r-C_r starts resonating. After the first dead time, the second phase (Phase Φ_2) starts, and transistor Q_2 is turned on at $t = t_2$. At this point, no new current path is created; however, the drain voltage of Q_2 is now equal to V_{out}. The secondary loop continues resonating (Phase Φ_{2a} in Fig. 5, $t_2 < t < t_3$), and at some point in time the drain voltage V_{DS_4} of Q_4 will become negative. At $t = t_3$, V_{DS_4} becomes sufficiently negative to trigger reverse conduction in Q_4, which occurs through the channel in enhancement GaN transistors. The energy stored in the L_r-C_r tank begins to discharge to the output during Phase Φ_{2b} ($t_3 < t < t_4$). After the additional dead-time t_{adt}, Q_4 is turned on to finally enable full conduction during Phase Φ_{2c} ($t_4 < t < t_5$), thereby completing the energy transfer to the output with lower losses. The time interval $[t_2, t_4]$ is called additional dead time (t_{adt}). At the end of Phase Φ_2, a second dead time t_{dt_2} occurs ($t_5 < t < t_6$), during which the secondary loop resonates again, preserving the residual energy for the next phase. After this, the cycle restarts with Phase Φ_1.

In the control waveforms shown in Fig. 5, the resonance frequency of the primary loop is lower than the switching frequency, and the residual energy in L_r is preserved in the secondary resonant loop, until the reverse conduction of Q_4 restores the primary resonant loop, and the control signals enable full conduction. This scenario is always guaranteed by design, as the switching frequency is incremented by the parameter k in relation to the targeted immunity margin (3). As a result, immunity is ensured by sacrificing ZCS; however, the expected quality factor of the secondary loop minimizes losses during dead-times. Moreover, due to reverse conduction, partial ZVS is still achieved. Depending on the duration of the additional dead time t_{adt}, conduction losses occur due to the voltage drop on Q_4 during its reverse conduction in Phase Φ_{2b}, until V_{GS_4} fully turns on Q_4 in Phase Φ_{2c}. Therefore, the power conversion efficiency, which is modeled and analyzed in the next paragraph, also depends on the parasitic capacitance of the power switches and the reverse voltage.

While this study primarily focuses on the 2:1 architecture, the fundamental operating principles of the MuReSCC can

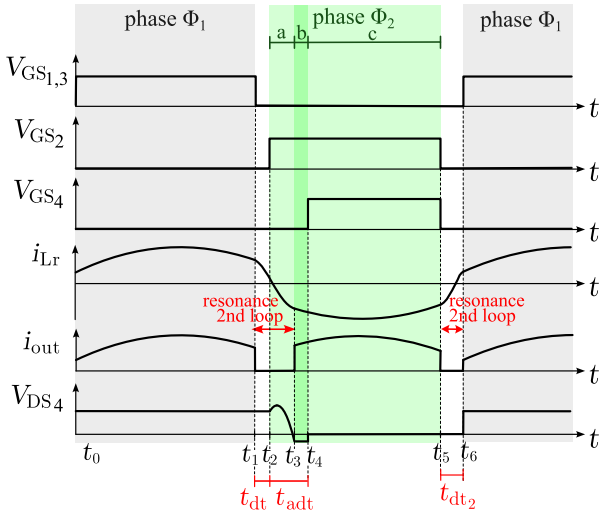

FIGURE 5. Waveforms of MuReSCC control scheme (not to scale).

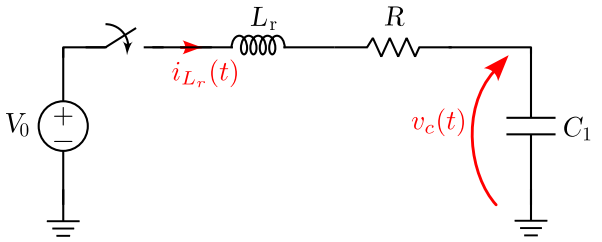

FIGURE 6. Simplified equivalent RLC circuit used for power conversion efficiency modeling of both ReSCC and MuReSCC circuits, in the on-off control case.

be extended to higher conversion ratios, such as a 4:1 Dickson MuReSCC. In a 4:1 implementation, multiple resonant branches are present, each with its own natural frequency designed around a common nominal value. Operating with a certain ratio k between the switching frequency and the nominal primary resonance preserves the topology's intrinsic tolerance to small component mismatches among the branches. This ensures that the qualitative operation remains unchanged and the RMS current is kept close to its theoretical minimum, despite slight differences in cell-to-cell resonant frequencies.

C. THEORETICAL POWER CONVERSION EFFICIENCY

The converter efficiency, denoted by η, can be estimated under the assumption that losses are solely due to the overall series resistance R in the current loops. By employing a hysteretic on-off control technique for voltage regulation, as in [24], the power conversion efficiency can be expressed as:

$$\eta \triangleq \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + R I_{L_r}^{RMS^2} \langle D \rangle}, \tag{4}$$

where $\langle D \rangle$ represents the average duty cycle of power conversion activation, and $I_{L_r}^{RMS}$ is the Root-Mean-Square (RMS) value of the current flowing through the inductor in the open-loop case in the considered conditions. The resistance R is assumed to be identical in both conduction phases. To accurately model η, the time-domain expression of the inductor current $i_{L_r}(t)$ is required. Moreover, the output voltage ripple is considered negligible, allowing the output capacitor to be modeled as an ideal voltage source for simplicity.

The equivalent circuit for the two phases can be modeled as a series RLC circuit, as depicted in Fig. 6. In this representation, the output current i_{out} coincides with the current $i_{L_r}(t)$ flowing through the inductor during the first half resonance period and with $-i_{L_r}(t)$ during the second half.

The circuit operation in both phases can be described by the equation of a conventional series RLC circuit:

$$V_0 = L_r \frac{d i_{L_r}(t)}{dt} + R i_{L_r}(t) + v_c(t), \tag{5}$$

where $v_c(t)$ is the voltage across the capacitor C_1, given by:

$$v_c(t) = \frac{1}{C_1} \int_0^t i_{L_r}(t) dt + v_{c_0}, \tag{6}$$

with $v_{c_0} = v_c(0)$ representing the initial voltage on C_1 at the beginning of each considered phase. The value of V_0 in (5) varies in relation to the considered phase:

$$\begin{cases} V_0 = V_{in} - V_{out}, & \text{for } \Phi_1 \\ V_0 = V_{out}. & \text{for } \Phi_2 \end{cases} \tag{7}$$

In both phases, due to ZCS, the initial condition $i_{L_r}(0) = 0$ must be considered. By solving (5) in underdamped regime, the inductor current $i_{L_r}(t)$ during each phase can be expressed as:

$$i_{L_r}(t) = \frac{V_0 - v_{c_0}}{\omega_0 L_r} e^{-\alpha t} \sin(\omega_0 t), \tag{8}$$

where $\omega_0 = \sqrt{\frac{1}{L_r C_1} - \alpha^2}$. Due to ZCS, the duration of each phase is:

$$t^* = \frac{\pi}{\omega_0}, \tag{9}$$

and the voltage $v_c(t^*)$ across capacitor C_1 at the end of each phase is given by:

$$v_c(t^*) = V_0 + e^{-\alpha t^*}(V_0 - v_{c_0}), \tag{10}$$

where V_0 assumes a different expression in relation to the control phase, as previously stated in (7).

The final value of v_c also serves as the initial condition for the subsequent phase. Since the final state of each phase matches the initial state of the next, the capacitor voltage evolution during the h-th switching period can be described as follows:

$$\begin{cases} v_{c_1}^{(h)} = (V_{in} - V_{out}) + e^{-\alpha t^*}\left(V_{in} - V_{out} - v_{c_0}^{(h)}\right) \\ v_{c_2}^{(h)} = V_{out} + e^{-\alpha t^*}\left(V_{out} - v_{c_1}^{(h)}\right) \\ v_{c_0}^{(h+1)} = v_{c_2}^{(h)}, \end{cases} \tag{11}$$

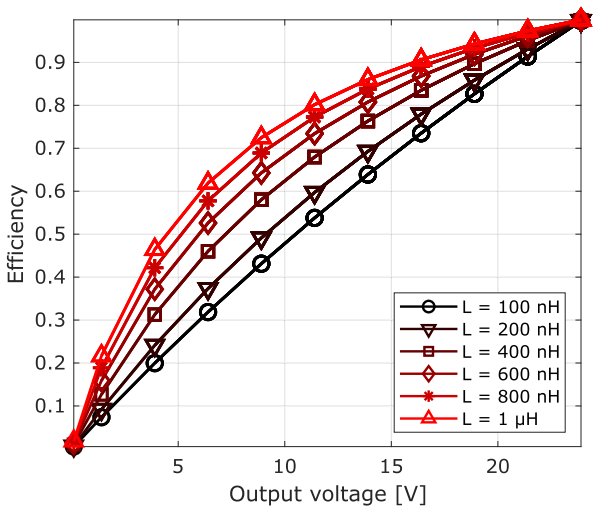

FIGURE 7. Power conversion efficiency of MuReSCC topology as a function of the target output voltage at different values of L_r for the same resonance frequency, at $V_{in} = 48$ V. The employed immunity factor k is 1.25.

where $v_{c_0}^{(h)}$, $v_{c_1}^{(h)}$, and $v_{c_2}^{(h)}$ are respectively the voltages across C_1 at the beginning of Φ_1, at the end of Φ_1 (or, equivalently, at the beginning of Φ_2), and at the end of Φ_2 of the h-th switching period. For the first cycle, it can be assumed that $v_{c_0}^{(0)} = 0$. It is then possible to use (11) to compute iteratively the values of v_c at the beginning and end of each phase, enabling an analysis of their evolution over time. These computed values allow to determine the waveform of current $i_{L_r}(t)$ during each phase of every switching cycle. At steady-state, for sufficiently large values of h, the waveforms become periodic, and it is possible to compute $I_{L_r}^{RMS}$, which in turn allows to evaluate efficiency using (4).

The above calculations can also be performed analytically under steady-state conditions (i.e., assuming $h \to \infty$). Since waveforms are periodic under this condition, it follows that $v_{c_2}^{(\infty)} = v_{c_0}^{(\infty)}$, meaning the voltage across C_1 at the beginning of Φ_1 necessarily equals that at the end of Φ_2, as illustrated in Fig. 2. By combining the above equation with the expressions reported in the first two equations in (11), it is possible to determine analytically that:

$$v_{c_0}^{(\infty)} = \frac{V_{out}(1+a) - aV_{in}}{1-a}, \tag{12}$$

where $a = e^{-\alpha t^*}$. Then, substituting this result in (8) yields the steady-state waveform of inductor current i_{L_r}, which takes, in first approximation, a sinusoidal form with amplitude:

$$i_0 \approx \frac{V_{in} - V_{out} - v_{c_0}^{(\infty)}}{\omega_0 L_r}. \tag{13}$$

From this expression, the RMS value $I_{L_r}^{RMS}$ can be computed, enabling to evaluate η via (4).

Fig. 7 shows the output efficiency, modeled with the previously described iterative analysis, as a function of the output voltage. The different curves correspond to various values of inductance L_r, yet at constant switching frequency f_{sw}, so that the value of C_1 is changed accordingly (see (2)).

Results show that, for a fixed resonance frequency, increasing L_r leads to higher efficiency when an on-off control is used for regulating the output voltage. This insight can be leveraged when selecting the value of L_r in relation to C_1, while maintaining the desired resonance frequency. The design trade-off lies between accepting losses of efficiency with on-off control and minimizing the inductor volume. This model is validated against experimental results for both ReSCC and MuReSCC topologies in Section V-F.

III. MURESCC DESIGN

A. SYSTEM ARCHITECTURE

As a specific contribution of this work, a complete architecture for the power converter was devised and implemented to demonstrate a fully independent operation of MuReSCC converters, along with ease of configuration, and support for automated measurement protocols (Fig. 8). The system implements a MuReSCC converter designed with GaN HEMTs operated at high frequencies above 1 MHz. The core of the system is a microcontroller unit (MCU), which generates precisely four independent phases by exploiting its internal high-resolution timers, and implements a closed-loop on-off control to regulate the output voltage. The local power supply block steps down an input voltage up to 60 V to an internal 5 V rail, which is then used to generate an additional 3.3 V rail for the MCU and the digital components, and four isolated 5 V supplies for each of the GaN HEMTs. Signal isolators separate the MCU from the gate drivers. This structure was necessary due to the unavailability of isolated drivers operating at the required frequencies.

B. DESIGN CONSIDERATIONS

Although different application constraints can lead to different design procedures, this work presents a practical design methodology, represented by the flowchart in Fig. 9, assuming that the main constraint is the achievable physical volume of the resonant inductor. The design process starts from the converter specifications, namely the input voltage (V_{in}), output voltage (V_{out}), maximum output power (P_{out}), and the maximum switching frequency allowed by device technology and control circuits. Firstly, these parameters define the required voltage and current ratings of the active devices. At startup, the maximum voltage stress across the switches is approximately equal to the input voltage (V_{in}). The current rating can be estimated through a first-harmonic approximation, under the assumption that it dominates the transferred power. Under this approximation, the RMS circulating current is approximately equal to the output current, and the peak current to withstand is approximately $I_{MAX} \approx \sqrt{2}P_{out}/V_{out}$.

Once the device ratings are established, the resonant inductor is selected according to the imposed volume constraints and the available magnetic technology. Among the feasible solutions, the preferred choice is the one that provides the

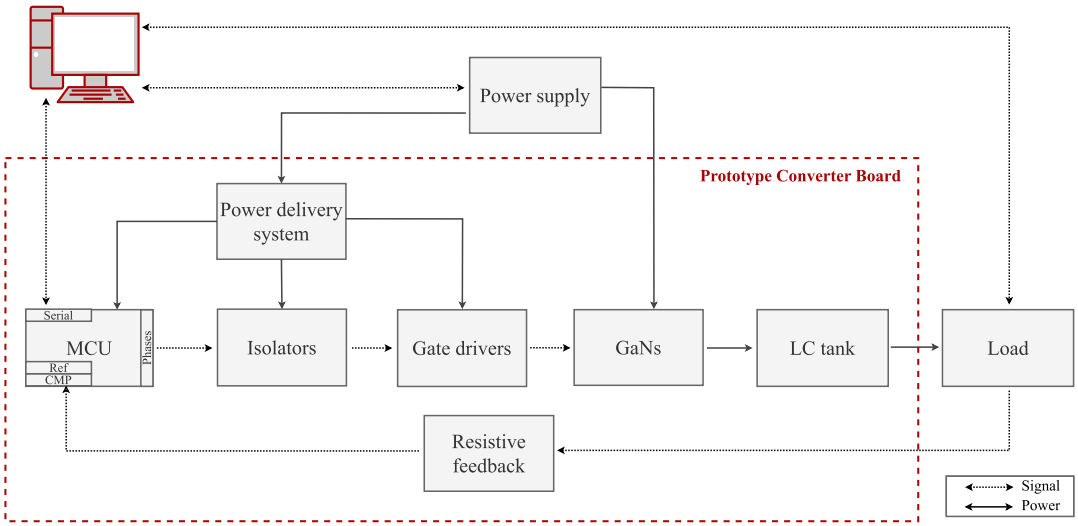

FIGURE 8. Block diagram of system architecture of the power converter, with the associated measurement system.

highest achievable inductance within the available volume while maintaining a low equivalent series resistance (ESR). This choice sets the achievable inductance (L_r) and its ESR. The total equivalent series resistance (R) of the resonant path can then be estimated as the sum of the switch on-resistances, inductor ESR, and capacitor ESRs. To guarantee under-damped operation, the critical resistance R_0 of the resonant loop, which is defined as

$$R_0 \triangleq 2\sqrt{\frac{L_r}{C_1}}, \tag{14}$$

must be greater than the actual loop resistance R, i.e. $R_0 > R$. Therefore, a target value of R_0 exceeding R by a sufficient margin must be selected. By combining (2) and (14), values for f_{res} and C_1 can be determined as:

$$f_{\text{res}} = \frac{R_0}{4\pi L_r}, \tag{15}$$

$$C_1 = \frac{4L_r}{R_0^2} = \frac{1}{\pi R_0 f_{\text{res}}}. \tag{16}$$

According to (3), i.e. $f_{sw} = k f_{res}$, the switching frequency can then be determined by selecting a suitable value of $k > 1$, thereby providing robustness against variations of the resonance frequency caused by tolerances, temperature drifts, and aging effects. Such variations are particularly significant when Class-2 ceramic capacitors are employed in ReSCC converters [25]. In practice, values between 1.2 and 1.3 generally provide a good trade-off between efficiency and robustness.

The auxiliary capacitor C_r is finally sized from the desired dead-time interval. Assuming that the current reversal of the secondary resonant loop approximately completes within the dead-time, the auxiliary capacitor can be estimated as

$$C_r = \frac{1}{L_r}\left(\frac{t_d}{\pi}\right)^2, \tag{17}$$

where t_d represents the total interval allocated for the secondary resonance. After the passive components are selected, the complete converter must be validated through circuit-level simulations. In particular, simulations should verify that the selected devices can sustain the actual peak and RMS currents when higher-order harmonics are considered, that the operating frequency remains compatible with the switching technology, and that the equivalent high-frequency resistances match the initial assumptions used during the design stage. It is worth emphasizing that this represents only one possible design methodology. Depending on the application, the designer may alternatively start from switching-frequency limitations, efficiency targets, or thermal constraints, and derive the passive components accordingly. This flexibility is one of the key advantages of the proposed topology.

The proper selection of the auxiliary capacitor C_r through (17) is critical for converter efficiency, as it directly dictates the shape of the current reversal during the dead-time. If C_r is selected too large, the auxiliary resonant frequency decreases and the capacitor acts nearly as a constant voltage source. This forces a constant current derivative, leading to a triangular current waveform that fails to fully reverse within a standard dead-time, thereby increasing RMS losses. Conversely, if C_r is too small, the high-frequency auxiliary loop completes multiple oscillation cycles within the dead-time interval, leading to unnecessary losses.

While the choice of t_{dt} and t_{adt} is mainly constrained by the properties of the switches, the values of C_1, C_r and L_r must be selected considering their effects on power conversion efficiency. In particular, t_{dt} is imposed by the selected device technology (and t_{adt} is derived from it), whereas C_r is chosen so that its associated resonant frequency is at least one decade higher than the main resonance. This design constraint prevents interaction between the two resonant tanks and makes the voltage gain essentially insensitive to C_r, so that C_r, t_{dt} and t_{adt} mainly act on device stress and soft-switching behavior,

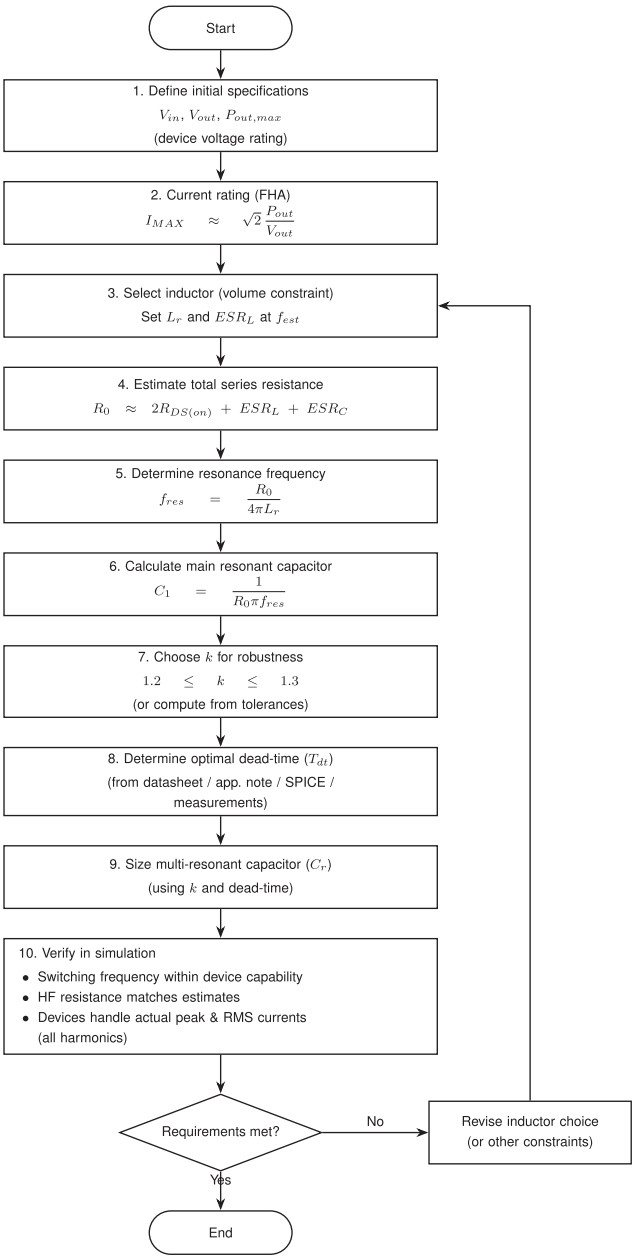

FIGURE 9. Flowchart of a possible design methodology.

trading off reverse-conduction robustness against additional conduction and switching losses.

The resonant capacitor C_r has a negligible direct influence on voltage gain and semiconductor stress, provided that the resonant frequency remains significantly higher than the switching frequency; however, its correct sizing is essential for energy recovery, reverse conduction, and quasi-zero-voltage switching, making it a key parameter for overall converter efficiency. The dead time (t_{dt}) has limited impact on voltage gain when the converter operates within its intended resonant regime, but excessive or insufficient values can increase current stress, compromise soft-switching conditions, and ultimately reduce efficiency. The additional dead time (t_{adt}) has a negligible effect on voltage gain, yet it strongly affects reverse-conduction operation: values that are too short may prevent the desired soft-switching mechanism, whereas excessively long values increase reverse-conduction losses and reduce efficiency.

From a theoretical perspective, increasing the resonant inductance L_r increases the critical resistance R_0 of the tank, effectively limiting the circulating charge and reducing both peak and RMS currents. However, in practical PCB inductor implementations, achieving higher inductance within the same physical footprint requires narrower tracks and more turns, such that its ESR scales with L_r.

When extending the design to multi-branch architectures (e.g., 4:1), the selection criteria for dead-time and passives do not fundamentally change. A common dead-time (t_{dt}) is selected such that, for nominal component values, the auxiliary resonance in each branch nearly completes the current reversal during this interval. The auxiliary capacitor C_r in each branch is sized according to this common dead-time requirement. If component mismatches cause slight variations in L_r or C_r across cells, some branches will reverse the current slightly faster or slower. However, the intrinsic tolerance of the multi-resonant structure successfully absorbs these minor frequency shifts, preventing incomplete current reversals and avoiding higher RMS currents without the need for independent dead-time controls.

IV. PROTOTYPE IMPLEMENTATION

A. RESONANT CIRCUIT DESIGN

The proposed design targets a 2:1 48 V-to-24 V open-loop conversion and is conceived to implement both ReSCC and MuReSCC schemes. A resonant frequency of $f_{\text{res}} = 1$ MHz was chosen, which is significantly higher than the one employed in [17], allowing the values of the passive components to be reduced. The coefficient k in (3) was set to 1.25, so that the switching frequency f_{sw} is equal to 1.25 MHz.

To minimize switching losses, enhancement-mode GaN HEMTs from Infineon (GS61004B) were selected, as they offer lower parasitic capacitances compared to silicon and silicon-carbide devices. The considerations expressed in the previous paragraph were followed by: *(i)* using the manufacturer-provided models in circuit simulators; *(ii)* using a linear series resistance model for the inductor (0.28 mΩ/nH); *(iii)* considering the parasitic series resistance of the capacitor provided by the manufacturer. As a result, the closest match to the required specifications (i.e., ESR, and RMS current supported) was found in the C1812 series of Kemet multi-layer ceramic capacitors (MLCCs). Performing a sweep of R_0 yielded an optimal value of 2.5 Ω, which maximizes the efficiency of the targeted open-loop conversion.

The sizing equations provides $L_r = 200$ nH, $C_1 = 127$ nF, and $f_{sw} = 1.25$ MHz. After rounding those values to commercially available devices and considering a dead time t_{dt} of 40 ns, the component values are summarized in the following Table 2.

TABLE 2. Component Values and Design Parameters

Component/Parameter	Value
$k = \frac{f_{sw}}{f_{res}}$	1.25
$C_1 = \frac{1}{R_0 \pi f_{res}}$	120 nF
$L_r = \frac{R_0}{4\pi f_{res}}$	220 nH
$C_r = \frac{1}{L_r}\left(\frac{t_d}{\pi}\right)^2$	820 pF
C_{out}	1 μF

B. PLANAR INDUCTOR

In order to explore viable alternatives to well-known suitable off-the-shelf air-core inductors, such as the Coilcraft 2222SQ-221, which meets the required size and performance specifications, this work investigates the effectiveness of custom air-core inductor designs directly implemented on printed circuit boards (PCBs). This approach is generally feasible due to the low inductance value required by the MuReSCC topology. This approach would not be applicable to buck converters, even when operated at significantly higher frequencies as in [4], which would require inductance values incompatible with this method.

While air-core inductors are particularly suitable for operation at frequencies above 1 MHz [26], PCB-based inductors offer several advantages. Firstly, an extremely low profile makes them suitable for space-constrained applications such as racks or LCD panels. Furthermore, as they leverage the existing PCB substrate, no additional solder joints and component assembly are required [27], [28]. PCB-based inductors simplify assembly and reduce overall manufacturing costs, compared to discrete inductors. However, there are some potential drawbacks to consider, including increased PCB area and potentially higher electromagnetic interferences (EMI) and inductive crosstalk.

To evaluate the feasibility of this approach, a PCB inductor was modeled and simulated by using electromagnetic analysis. The design aimed to balance overall size with series resistance. As shown in Fig. 10, the inductor consists of three parallel, mutually coupled, rectangular spiral traces, each with three turns. It is implemented on a 4-layer PCB with 2 oz (70 μm) copper thickness. The traces are 1 mm wide and spaced 0.25 mm apart. The mutual coupling among the spirals helps maintain the target inductance while reducing the overall series resistance. The resulting inductor achieves an inductance of 214 nH with an ESR of 63 mΩ at 1.25 MHz.

Although a detailed optimization of the PCB inductor is beyond the primary scope of this paper, its design followed a two-step procedure [27], [28]. Initially, the geometry of a single square planar spiral was analytically sized using Wheeler's empirical formulas [27] to target approximately 220 nH within a constrained 2 $\times$ 2 cm^2 footprint.

To reduce the ESR while maintaining the target inductance, the final design implements three identical planar windings distributed across different PCB layers, connected in parallel, and precisely aligned to ensure high mutual coupling. In the second step, the three-winding structure was imported into a planar electromagnetic simulator. Starting from the initial sizing based on Wheeler's equation, a parametric optimization was performed to extract the frequency-dependent parameters ($L(f)$, $R(f)$, $Q(f)$), ensuring that the target inductance was met at the operating frequency, the quality factor was maximized, and the self-resonant frequency remained safely above the operating range.

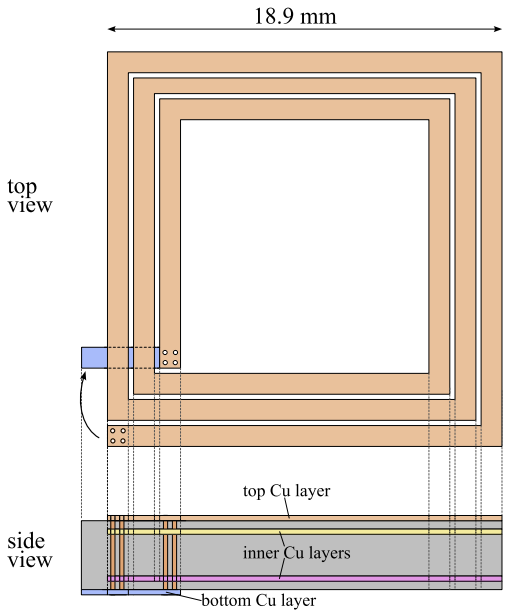

FIGURE 10. Sketch of the PCB inductor.

C. SYSTEM PROTOTYPE

The block diagram of the system prototype of the proposed hybrid ReSCC 2:1 and MuReSCC 2:1 is sketched in Fig. 8. The assembled circuit is shown in Fig. 11, and measures 96.7 $\times$ 40 mm, including the PCB inductor.

A first section handles control, phase generation, and feedback management, implemented using an STM32G474RE microcontroller from STMicroelectronics. The custom firmware is available at [29]. The second section is dedicated to driving operations. For proper functionality of this prototype, no suitable commercially available isolated drivers were identified. Therefore, four low-side high-frequency drivers (LMG1020 from Texas Instruments), operating at up to 60 MHz with 400 ps fall/rise times, were employed. Each driver was isolated at the signal level using a signal isolator (ISO7720 from Texas Instruments). On the back side of the board, four isolated power islands were implemented using UCC12040DVE also from Texas Instruments. This configuration compromises the overall compactness of the converter; however, we are confident that future developments in driver technology will help overcome these limitations. The ultimate goal is to minimize the total volume occupied by the components. Furthermore, since the driver does not provide a negative gate-source voltage (V_{GS}) during turn-off, a degradation in the dynamic on-resistance ($R_{DS,on}$) is observed

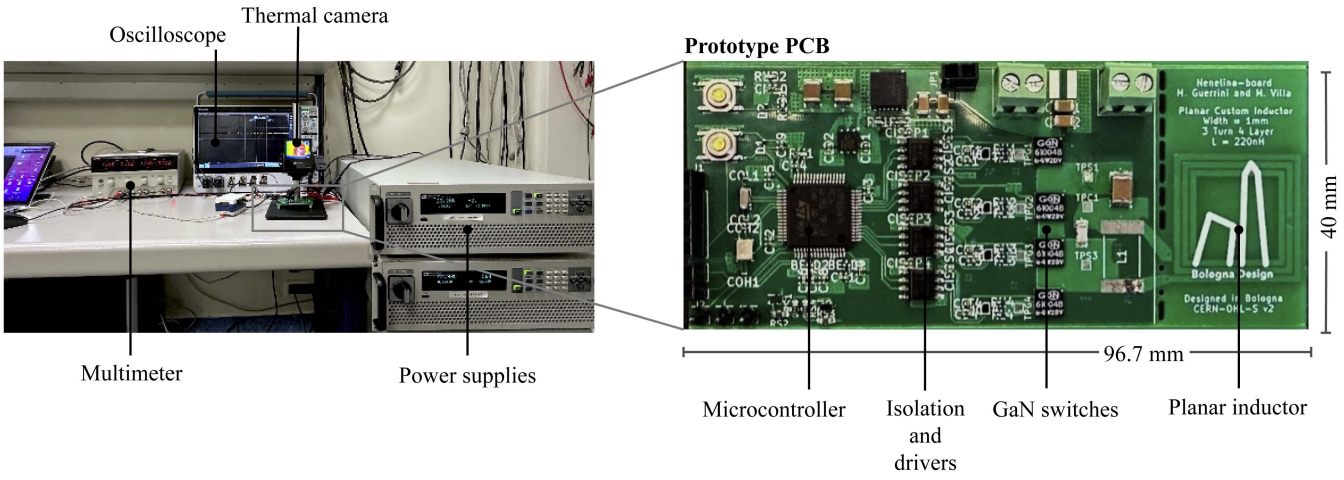

FIGURE 11. Picture of the experimental setup (left) and of the hybrid ReSCC-MuReSCC PCB prototype (right).

at these frequencies, due to the interaction between surface traps and buffer traps [30]. The last section implements power conversion and includes GS61004B enhancement-mode GaN HEMTs from Infineon, rated for 100 V and 38 A, a main resonance capacitor C_1 (Kemet C1812C124J1GACTU), and a multi-resonance capacitor C_r (Kemet C1206C821J1GACTU). The circuit topology can be switched between ReSCC and MuReSCC by simply connecting or disconnecting the secondary-resonance capacitor C_r.

The applied timing parameters were $t_{dt} = 40$ ns for the dead-time, and $t_{adt} = 20$ ns for the additional dead time (see Fig. 5). The above values were chosen in accordance with the switches characteristics provided by the manufacturers, and also to prevent shoot-through events due to potential phase misalignments caused by the gate control signal chain (microcontroller, signal isolator and drivers).

V. EXPERIMENTAL RESULTS

A. MEASUREMENT SETUP

The experimental setup consisted of the following:

- a personal computer (PC), used to automate the measurement setup.
- a Tektronix MSO56 oscilloscope, employed to monitor the input and output voltages.
- two Itech IT6000 C programmable bidirectional power supplies, one used as a power supply and the other as a load, also utilized for measuring input power P_{in} and output power P_{out}.
- a thermal camera, used to monitor temperature.

Measurements were performed on both MuReSCC and ReSCC topologies. Measurements for the single-resonant converter ReSCC were performed on the same board, by removing the multi-resonance capacitance C_r, and by adapting the control scheme to operate accordingly. Each measurement is carried out under the most appropriate conditions or at maximum power to properly isolate the phenomenon under observation, while carefully remaining within the thermal limits of the devices. Fig. 12 shows the four control phases and the inductor current, which can be compared with the theoretical waveforms reported in Fig. 5.

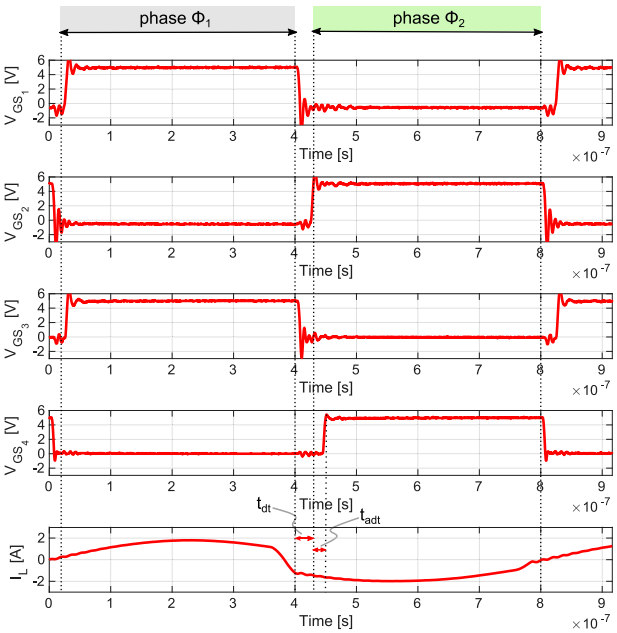

FIGURE 12. The four waveforms corresponding to the four phases (V_{GS_x}) are displayed, with the final figure representing the inductor current for a 35 W load and an open-loop conversion ratio of 48-24 V.

B. VALIDATION OF CONTROL TIMING PARAMETERS IN MURESCC

The first set of measurements was conducted on the MuReSCC to verify that the timing parameters discussed in the previous section resulted in an optimal operating point. To perform this validation, efficiency measurements were conducted in open-loop operation targeting 48 V to 24 V conversion with a 35 W load. This power level was chosen to

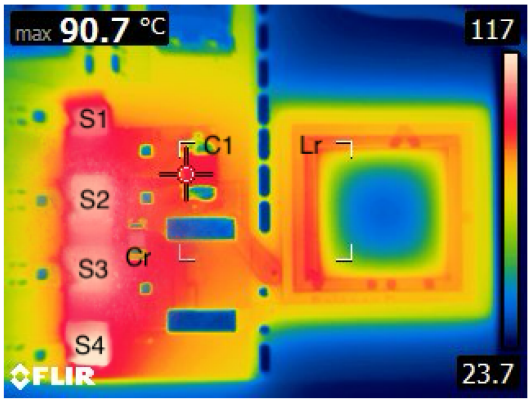

FIGURE 13. Thermal camera image in open-loop operation at maximum output power for MuReSCC mode, with an ambient temperature of 20 °C.

ensure safe operation even under significant deviations from optimal efficiency and to avoid overheating of active devices. During these measurements the dead time, additional dead time, and operating frequency were varied.

Fig. 14(a) shows a heatmap of the power conversion efficiency η at 35W load as a function of the dead time t_{dt} (y-axis) and additional dead time t_{adt} (x-axis), averaged across the target switching frequency (1.25 MHz), and two additional ones (1 MHz and 1.5 MHz). The region of optimum efficiency is clearly identifiable, with an efficiency peak of 98.5% occurring around a 40-ns dead time and a 20-ns additional dead time, confirming the design specifications experimentally. Additional measurements were performed at 5 W and 120 W (see Fig. 14(b) and (c)). The latter were conducted within a narrower variation range of dead-time and additional dead-time values to prevent excessive thermal stress on the converter. In all cases, the same trends were observed.

Unlike conventional hard-switched converters where the optimal dead-time varies with the load [31], the proposed MuReSCC exhibits an inherently load-independent timing behavior. Because the current and voltage waveforms are strongly shaped by the resonant network, the timing of the current zero-crossings is predominantly dictated by the passive LC tank parameters rather than the output power magnitude. Consequently, the quasi-ZVS and ZCS boundaries do not shift significantly, making load-dependent adaptive dead-time tracking unnecessary.

This intrinsic stability is validated by the extended power-sweep measurements. As demonstrated by the broad efficiency maximum in Fig. 14, small deviations from the optimal timing incur only marginal penalties. Therefore, the dead-times (t_{dt} and t_{adt}) optimized at the nominal 35 W load were kept fixed for all subsequent tests, successfully maintaining peak efficiency up to the maximum rated power. Finally, while applying a negative gate-source voltage during the off-state could theoretically allow for further dead-time reduction, standard gate drivers were utilized in this prototype due to commercial availability constraints at the time of development.

C. EVALUATION OF MURESCC IMMUNITY TO VARIATIONS OF CIRCUIT PARAMETERS

To assess the effectiveness of the MuReSCC converter in maintaining immunity to variations in circuit parameters, the power conversion efficiency η was measured at a fixed output power of 35W for both MuReSCC and ReSCC configurations. The normalized switching frequency was varied by applying different values of the immunity coefficient k, as defined in (3).

In particular, since the main resonance frequency is determined by the values of C_1 and L_r, the coefficient k was varied by changing the switching frequency of the GaN devices via the microcontroller. The efficiency measurements were conducted in the same configuration of Section V-B.

The results are reported in Fig. 15. The efficiency of MuReSCC decreases by less than 1% within a range of $\pm$300 kHz from the nominal 1.25MHz operating frequency (corresponding to $k = 1.25$). Conversely, if we consider the same frequency range for the ReSCC (whose nominal operating frequency corresponds to $k = 1$), the efficiency loss exceeds 15%. This demonstrates that the MuReSCC topology offers a significant improvement over ReSCC converters in terms of immunity to parameter variations affecting the resonance frequency.

It must be noted that all measurements in this parametric sweep were recorded under steady-state conditions, allowing the system to settle at each specific operating frequency. In a real-world application, dynamic deviations of the parameter k are primarily driven by thermal drifts or component aging—phenomena that occur on time scales drastically slower than the converter's electrical dynamics. Cycle-by-cycle frequency variations, such as the clock jitter of the digital controller, are typically well below 1% and are entirely absorbed by the intrinsic robustness of the MuReSCC without inducing measurable transient disturbances

D. OPEN-LOOP PERFORMANCE

The open-loop efficiency was also measured as a function of the output power with an input voltage $V_{in} = 48$V. Furthermore, measurements were performed with the nominal operating frequency configurations, i.e., $k = 1$ and $k = 1.25$ for the ReSCC and MuReSCC converters, respectively. To characterize the tolerance of the two schemes with respect to component variations, the same measurements were first repeated for values of k corresponding to $\pm$30% variations in C_1 or L_r. This results in an approximate variation of $\pm$15% in k with respect to its nominal value. Additionally, the same measurements were performed while varying the value of C_1 by approximately $\pm$25%.

The experimental results, reported in Fig. 16, show that the peak efficiency is nearly identical for both converters, with the MuReSCC achieving 98.9% and the ReSCC reaching 98.4%. Efficiency is measured as the ratio of output power to input power, evaluated across a sweep of output power levels. It can be observed that for output powers below 72 W,

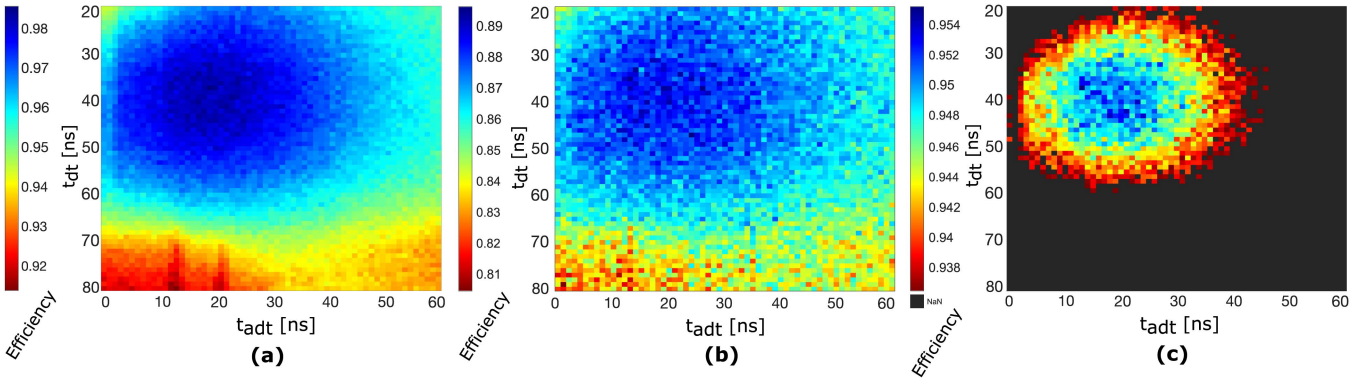

FIGURE 14. Heatmaps of measured power conversion efficiency η as a function of dead time t_{dt} and additional dead time t_{adt} during open-loop power conversion from 48 V to 24 V under the following conditions: (a) averaged over operating frequencies of 1, 1.25, and 1.5 MHz with 35 W load, (b) 5 W load at 1.25 MHz, (c) 120 W load at 1.25 MHz.

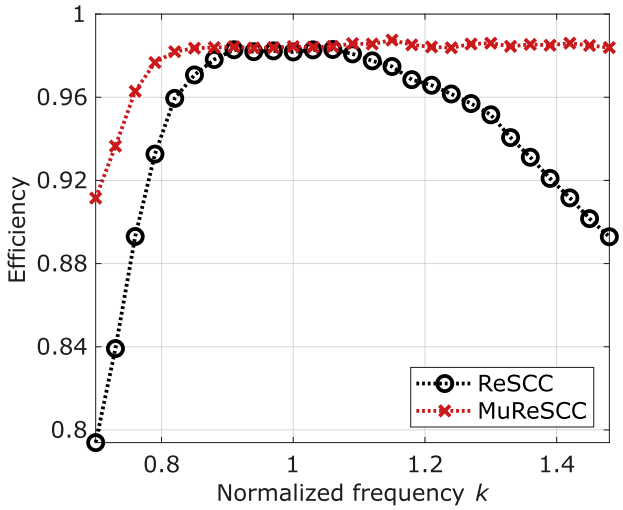

FIGURE 15. Experimentally measured open-loop efficiency of the MuReSCC and ReSCC converters, with $V_{in} = 48$ V and $V_{out} = 24$ V at $35W$, as a function of the normalized switching frequency coefficient k.

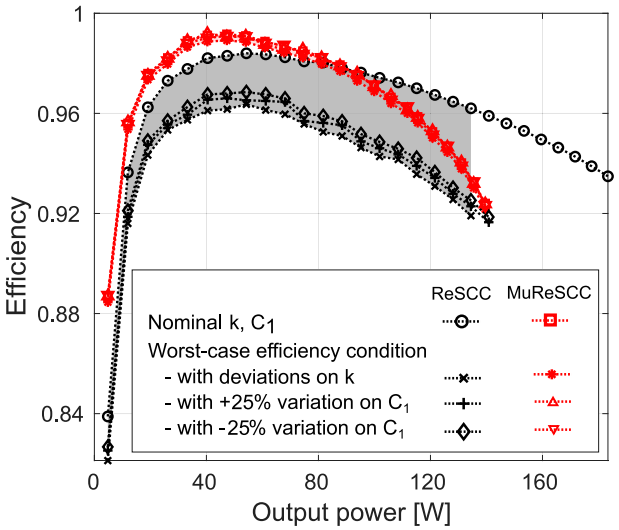

FIGURE 16. Experimentally measured open-loop power conversion efficiency of the MuReSCC and ReSCC converters as a function of P_{out}, with $V_{in} = 48$ V and a target $V_{out} = 24$ V. For each converter, the plot illustrates the curves for: the nominal values of k and C_1, deviations of k yielding the worst efficiency condition (equivalent to -30% component deviation) with the nominal C_1, variations of C_1 of respectively $\pm 25\%$ with the nominal k. All other curves fall within the shaded area.

the MuReSCC provides better performance than the ReSCC. For higher output power (corresponding to higher output currents), the ReSCC performs better and delivers higher power while maintaining slightly lower device temperatures (all measurements were halted upon reaching a case temperature of 120 °C to avoid device damage). This behavior is likely due to the smaller conduction angle of the fourth switch in the MuReSCC, which tends to increase its temperature more significantly than in the ReSCC due to less efficient reverse conduction. However, in the multi-resonant converter, the sensitivity of efficiency to parameter variations is practically negligible, whereas, depending on the parameter deviations, the single-resonant configuration exhibits a substantial spread in the reported efficiencies (gray area in Fig. 16).

E. ON-OFF CONTROL PERFORMANCE

For regulation purposes, an on-off control system was implemented, primarily managed by the internal comparator of the MCU. The converter output voltage is scaled down using a resistive ladder and fed into the comparator to enable feedback control.

The output ripple is set to 100 mV, determined by the minimum hysteresis of the internal comparator multiplied by the gain of the resistive feedback network. Due to the comparator's sensitivity to voltage levels, an additional output capacitor would not effectively reduce the ripple. Instead, ripple reduction may be achieved by selecting a more precise comparator or by decreasing the feedback gain.

The measured efficiency performance at various output voltages is shown in Fig. 17 as a function of the output current for both the ReSCC and MuReSCC. The output power sweep was performed for target output voltages set at 18 V, 15 V, and

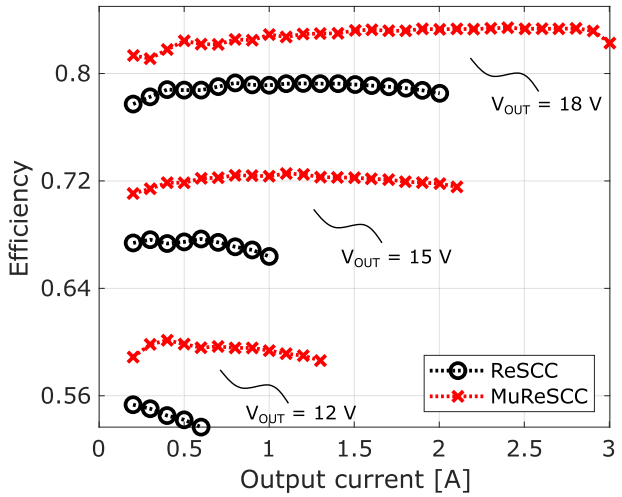

FIGURE 17. Measured open-loop efficiency of ReSCC and MuReSCC for V_{in} = 48 V, and output voltages V_{out} = 18 V, 15 V and 12 V, as a function of load current with an on-off control system regulating the target output voltage.

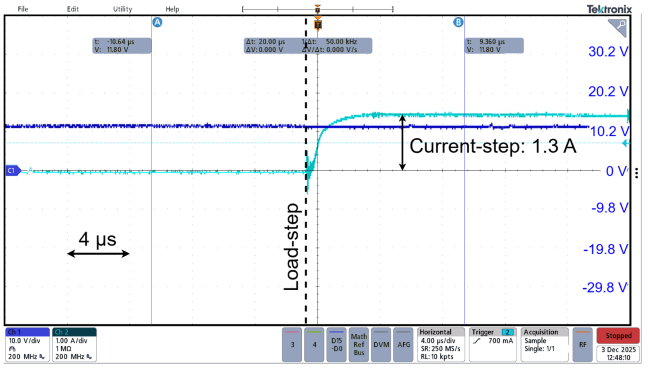

FIGURE 18. Output voltage (blue) and output current (light blue) waveforms measured with an oscilloscope. A current step from 0 A to 1.3 A is applied by connecting a load resistor through a switch. The output voltage is regulated at 12 V with a 48 V input.

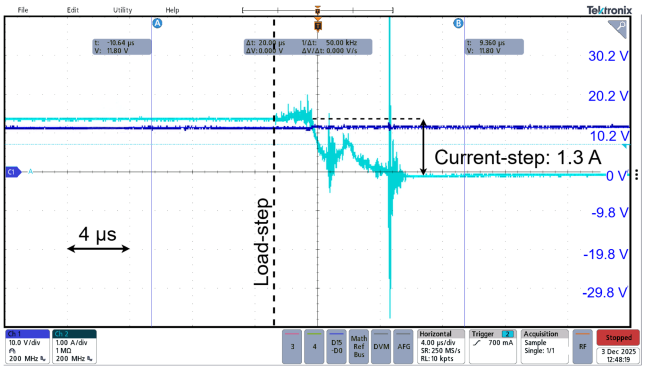

FIGURE 19. Output voltage (blue) and output current (light blue) waveforms measured with an oscilloscope. A current step from 1.3 A to 0 A is applied by disconnecting the load resistor through a switch. The output voltage is regulated at 12 V with a 48 V input.

12 V. Also in this case, all measurements were halted when any switch reached a case temperature of 120 °C.

Experimental results clearly show that the MuReSCC achieves slightly higher performance compared to the ReSCC for the same voltage conversion ratio. As the output voltage deviates from the open-loop value, i.e. half the input voltage as set by the 2:1 topology, the converter performance decreases, consistently with the theoretical analysis introduced in Section II-II-C. This decline is primarily due to the increase in RMS current through the inductor relative to the same average output current, as previously discussed.

This behavior is primarily due to the asynchronous on-off control method. Specifically, since the converter experiences a greater voltage difference across the LC tank compared to the open-loop condition, the peak current becomes higher. Additionally, operating with a smaller conduction angle (as the converter must be turned off at certain times with the on-off control) results in the converter handling higher instantaneous power for the same output power. The extent of this increase depends on both the load and the desired conversion ratio, with a shorter allowed on-time requiring the converter to manage proportionally higher instantaneous power. As shown in 7, increasing L_r is beneficial to power conversion efficiency. Nonetheless, further studies on alternative control methods could be of particular interest, especially by maintaining ZCS [32], [33], adopting multi-resonant compensation strategies [34], or cascading with other topologies [35]. However, this behavior is inherent to the considered resonant topologies, due to their fixed open-loop conversion ratio. As stated in the objectives of this work, the concept focuses on identifying circuit topologies alternative to conventional SICs, characterized by lower inductance and better performance than linear regulation or standard SCCs.

Furthermore, a dedicated set of measurements has been performed to characterize the converter's dynamic response to load transients. The transient was generated by connecting and disconnecting a resistive load through an externally controlled MOSFET switch placed at the converter output, producing a repeatable and abrupt load step between 0 A and 1.3 A. The converter operated from a 48 V input and regulated a 12 V output. The output voltage and output current were simultaneously acquired using a digital oscilloscope to capture the converter response before, during, and after the load transition. Figs. 18 and 19 show the corresponding oscilloscope waveforms. These results complement the previously presented steady-state data and confirm that the converter maintains correct regulation and exhibits appropriate transient behavior under sudden load variations.

F. THEORETICAL MODEL VALIDATION

The power conversion efficiency model presented in Section II-C is now assessed against previous experimental results. Fig. 20 reports the theoretical efficiencies of ReSCC and MuReSCC as a function of the target output voltage. Data

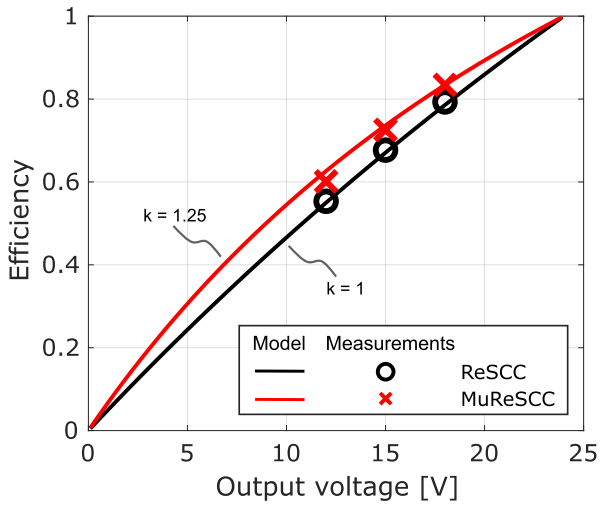

FIGURE 20. Theoretical and measured power conversion efficiency of ReSCC and MuReSCC topologies as a function of the target output voltage. A normalized switching frequency with k of 1 and 1.25 is used for ReSCC and MuReSCC, respectively.

were obtained by solving the theoretical model equations, previously presented in Section II-C, with the design parameters reported in Table 2.

Model validation is achieved with the results shown in Fig. 17 by reporting the measured peak efficiencies of ReSCC and MuReSCC. The results are consistent with the proposed efficiency model for both converters, so that it may be employed for further analyses in the design of such power converters.

VI. CONCLUSION

This paper presented the design of a hybrid MuReSCC. The current prototype was used to compare ReSCC and MuReSCC topologies. The developed system can operate completely standalone, without the support of any external signal generator or instrumentation, and implements output voltage regulation, which was characterized in terms of efficiency. The prototype operates at a switching frequency of 1.25 MHz, utilizes GaN HEMTs, and features a coreless PCB inductor. The prototype achieves a peak efficiency of 98.9% and a maximum output power of 200 W, ensuring a minimum efficiency of 98% under 30% variations in oscillation frequency, compared with the ReSCC's minimum efficiency of 88%.

The design choices are additionally supported by a numerical model developed to evaluate the power conversion efficiency of the resonant converter. For fixed voltage conversion ratios or operating points near them, the MuReSCC proves to be an efficient alternative to SICs even when using on-off control. Operation for conversion ratios different from the nominal open-loop value, despite the lower associated efficiency, still represents a reasonable compromise compared to SICs, SCCs and linear regulators, both in terms of efficiency and passive component size. This study may also find applications in the field of integrated DC/DC converters, where compact size, small inductances, and high efficiency are among the primary design drivers.

The experimental comparison between single-resonant and multi-resonant converters confirms the effectiveness of the multi-resonant approach in providing immunity to variations in component parameters. Additionally, the multi-resonant converter demonstrated higher efficiency when using the on-off control method than the mono-resonant case, and the results are consistent with the numerical model of power conversion efficiency.

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