A Novel Modular Multilevel Converter Based on Interleaved Half-Bridge Submodules

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***Abstract*—A new Modular Multilevel Converter with Interleaved half-bridge Sub-Modules (ISM-MMC) is proposed in this paper. The ISM-MMC exhibits a higher modularity and scalability in terms of current ratings with respect to a conventional MMC, while preserves the typical voltage level adaptiveness. The ISM-MMC brings the known advantages of classical MMC to low-voltage, high-current applications making it a novel candidate for the sector of ultra-fast chargers for all types of electrical vehicles (EV). This advanced topology makes it possible to easily reach charging power of the EV charging system up to 4.5 MW and beyond with low-voltage supply. To operate the new converter, a hybrid modulation scheme that helps to exploit advantages of the interleaving scheme, is implemented, and explained in this paper. It has been verified that the typical MMC control methods are still applicable for ISM-MMC. A comparative study between classical MMC and ISM-MMC configurations in terms of output characteristics and efficiency is also given. Furthermore, it has been demonstrated that the number of ac voltage levels is synthetically multiplied by the number of interleaved half-bridge legs in submodules. Simulations, Hardware-in-the-Loop and Experimental tests are carried out to demonstrate the feasibility of the proposed topology and implemented modulation scheme.**

***Index Terms*—modular multilevel converters, interleaved, pulse width modulation, charging stations, electric vehicles.**

I. Introduction

MODULAR multilevel converters (MMCs) have been winning over conventional solutions in many high- and medium-voltage applications owing to their capability in transformerless ac-dc and dc-ac conversion, while introducing lower harmonic pollution and having higher efficiency. While MMC has become the worldwide standard for high-voltage dc transmission [1], it has also been investigated in the power electronic transformer applications [2], medium-voltage motor drives, frequency change systems [3], etc. Depending on the application, the structure of submodules (SMs) is mainly half-bridge (HB) or full-bridge (FB), while many other types of SMs have been reported in the literature [3]. While voltage ratings of MMCs can vary in a great extent, current ratings instead are normally limited by the maximum current that components (mainly power switches) can handle, taking into account safety margins. In this context, the power capability of the classical MMC is limited once the voltage level was fixed. Some possibilities to boost current capacity of the classical MMC have been already discussed in [4], [5], exploiting current partitioning through parallel connection of converters' legs, arms (branches) or power modules in each MMC cell. However, the presented solutions do not exploit the interleaving scheme and hardly scalable when converter is already built/structured since it involves modifications on the converter level.

The interleaved concept has been thoroughly studied in the context of two-level dc-ac and dc-dc converters [6], providing opportunity not only to share the total current among interleaved units but also enhancing quality of input/output waveforms. For instance, authors in [6] demonstrated the possibility to obtain a ripple-free output current in interleaved dc-dc converters. On the other hand, this approach has been limited in MMC applications. In [7] authors proposed a dc-dc interleaved MMC for PV applications. Although, the proposed topology is named as "modular multilevel converter" it only partially resembles to a classical MMC structure, sharing floating capacitors between adjacent submodules. By bringing together the best practice of interleaving theory and current partitioning in a classical MMC structure, the ISM-MMC was initially introduced in [8].

There are several trending low-voltage, high-power applications that can benefit from ISM-MMC architecture, namely converters in ac or dc traction power supplies and ultrafast electric vehicle (EV) charging infrastructure. However, this list is not limited by low-voltage level. In fact, since the new converter topology is easily scalable in both voltage and current ratings, it can be used in a wide range of voltage and current levels. For instance, at this moment several charging systems are available on the market (e.g., GB/T, New GB/T, CHAdeMO, CCS1, CSS2, Tesla) having maximum charging power in between 237.5 - 900 kW range. Furthermore, a new High Power Commercial Vehicle Charging (HPCVC) standard is currently under development, which will level up the power delivery up to 4.5 MW. For this paper, a well-adopted commercial infrastructure for ultrafast EV charging with output power 180 kW has been selected as a reference application.

To the best of the authors' knowledge, all the previous publications regarding the MMC structure have focused on interleaving either at the leg or arm levels, and none, apart from [8], were considering the interleaving concept at the submodule level. The main contribution of the current work concerns some missing aspects and developments of [8], namely, performance

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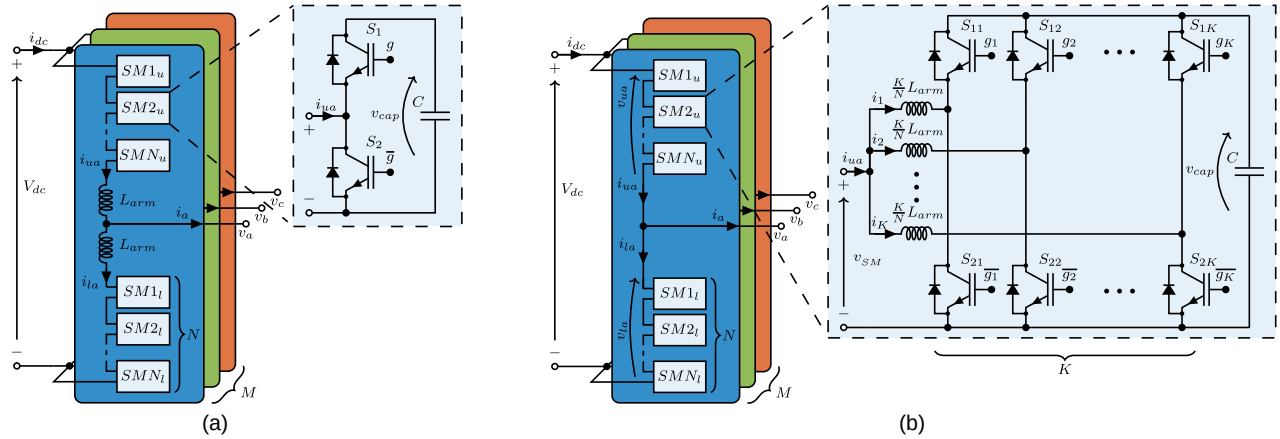

Fig. 1. Scheme of (a) the standard MMC with half-bridge submodule and (b) the proposed ISM-MMC with interleaved half-bridge submodule.

comparison between the classical MMC and ISM-MMC structures, as well as an implementation of the closed-loop strategy for ISM-MMC and analysis of its dynamic behavior.

The paper is structured as follows. Section II introduces the ISM-MMC topology, providing essential mathematical models. The closed-loop control methods and modulation schemes are discussed in Section III. Verification of ISM-MMC concept is supported by numerical simulations in Sections IV and by performed hardware-in-the-loop (HIL) and experimental test in Section VI. Comparison of ISM-MMC with the classical MMC configurations is given in Sections V. Finally, conclusions are drawn in Section VII.

II. Proposed Topology

A structural representation of an *M* phase (typically 3 phase) MMC using a half-bridge (HB) submodule configuration is shown in Fig. 1a. This MMC employs two-arm arrangement in each phase leg, commonly labeled as the upper (*u*) and lower (*l*) arms. Each MMC arm consists of *N* series connected power submodules and an arm inductor. Every SM is made up by a half-bridge leg joined in parallel with a capacitor. The output terminals of the submodule are the midpoint of the half-bridge leg and one of the sides of the capacitor (here low side is taken by default). The voltage level and power capacity of this type of MMC can be generally increased by the series connection of power submodules in each arm. As it was explained in [8] the arm inductor can be evenly distributed among the arm composing submodules without affecting the equivalent circuit of the whole converter. Having an inductor in each SM, it can be further split into *K* equally sized parallel inductors. Then, by connecting each one of these inductors to the midpoint of a dedicated half-bridge leg and linking their output and dc terminals the interleaved configuration of a submodule with *K* legs can be derived. The proposed MMC with interleaved half-bridge submodules, labeled as ISM-MMC, is illustrated in Fig. 1b. It should be noted that the interleaved half-bridge legs on the dc side share a common floating capacitor. This fact does not introduce extra complexity for the capacitor voltage balancing algorithms that are well established for the classical MMC. The current rating of 'inductor – HB-leg' units in the proposed submodule can be *K* times lower in comparison with switches and arm inductor in a classical MMC (cf. Fig. 1a). Alternatively, the total rated current of the new SM can be *K* times higher than the classical HB-based SM, preserving properties of individual HB-legs. Therefore, ISM-MMC introduces an additional way for increasing power capacity of the standard MMC structure by stepping up both voltage and current levels. In this context, the proposed ISM-MMC is well suited for all voltage levels high-current applications. The concepts of power scalability and/or power partitioning, discussed in [4], [5], with ISM-MMC gain an extra degree of freedom in comparison with classical MMCs, namely expanding on the submodule level. Since the degree of modularity in each of MMC levels: number of phases, number of series connected cells (SMs) and number of parallel (interleaved) HB legs in SMs are independent from each other, these three axes can be considered as orthogonal to one another, enabling a representation as shown in Fig. 2. Here, each cube represents a specific design with a certain degree of modularity in each of the axes.

For instance, an element close to origin would represent a design with low-level of modularity in all axes, i.e., a single-phase, single-cell MMC. On the other hand, an element distant from the origin would represent a highly expansive structure, i.e., a multi-phase, multi-cell ISM-MMC.

The proposed ISM-MMC has an additional feature that has not been discussed so far, namely the possibility not only sharing high-current among the parallel HB legs in each SM but also to further enhance the quality of output voltage waveforms by applying the interleaving concept. This ISM-MMC property leads to a very modest filtering requirements on the grid side.

Assuming a balanced and constant dc-link bus voltage equal to V_{dc}, the per phase relation among each output x^{th} phase (for three-phase system $x = a,b,c$) voltage, corresponding arm voltages and dc-link voltage in ISM-MMC can be expressed as:

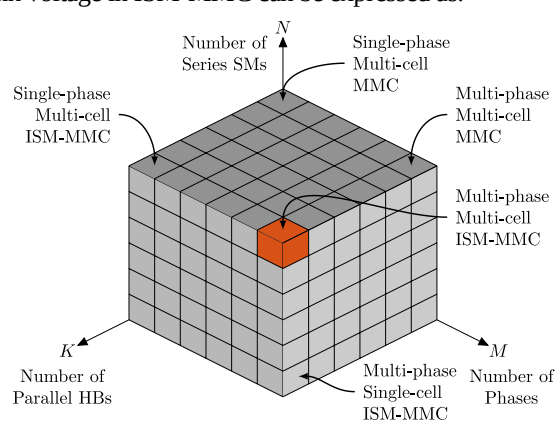

Fig. 2. Graphical representation of the three main degrees of modularity of ISM-MMC topologies.

$$\frac{V_{dc}}{2} - v_u = v\,, \qquad -\frac{V_{dc}}{2} + v_l = v \tag{1}$$

being v_u upper and v_l lower arm voltages, v the output phase voltage. Here and throughout the whole paper, for simplicity, the phase label (x) is generally omitted unless it is strictly necessary. The presented equations are derived per phase.

The arm voltages v_u and v_l, which are measured between the midpoint of the converter's arm and the corresponding dc rails, can be represented as a sum of composing submodule voltages:

$$v_{u,l} = \sum_{n=1}^{N} v_{SMn}|_{u,l} \tag{2}$$

where $v_{SMn}|_{u,l}$ is the nth submodule's voltage of the upper or lower arm. It can be derived as:

$$v_{SMn} = \frac{1}{K}\left[L\sum_{k=1}^{K}\frac{di_{n,k}}{dt} + R\sum_{k=1}^{K} i_{n,k} + \mathfrak{z}_n v_{cap,n}\right] \tag{3}$$

where K is the number of legs inside the submodule (K=1 in the case of the classical MMC Fig. 1a, K>1 in case of the interleaved configuration Fig. 1b) and n represents an ordinal number of the corresponding n^{th} SM of the upper or lower arm. Parameters L and R are the inductance and internal resistance of a leg inductor inside each SM, respectively. The term $i_{n,k}$ is the current of the kth leg inside the nth SM. It is worth to note that $i_{n,k}$ is equal to $i_{u,l}$ in case of classical MMC being the SM composed of only one HB-leg. Finally, v_{cap} and $\mathfrak{z}$ are the capacitor voltage and the corresponding number of HB legs in the SM where the top switch is "on". The latter is defined as the sum of logical gate signals $g_{n,k}$ (either 0 or 1) in n^{th} submodule:

$$\mathfrak{z}_n = \sum_{k=1}^{K} g_{n,k}\,. \tag{4}$$

As noticeable from (3), the enhancement of the ac voltage waveform is achieved thanks to the multilevel waveform of the open circuit voltage across ac terminals of each submodule. In fact, in total, there are K+1 open circuit voltage levels ranging between (and including) "0" and "v_{cap}". Having identical inductors (i.e., same R and L), and according with the interleaving concept, the open-circuit voltage across submodules' ac terminals is simply the average of pole voltages of the parallel branches. Depending on state of the legs' switches, the corresponding pole voltage can be either "0" or "v_{cap}". By applying the interleaving concept, the averaging of pole voltages will result in multilevel voltage structure with the following states 0, v_{cap}/K, $2v_{cap}/K$…$(K\text{-}1)v_{cap}/K$, v_{cap}.

The output (i) and circulating (i_{cir}) currents in the ISM-MMC are alike in classical MMCs and they can be defined as:

$$i = i_u - i_l\,, \qquad i_{cir} = \frac{i_u + i_l}{2} \tag{5}$$

where i_u and i_l are the upper and lower arm currents, respectively.

Bearing in mind that the sum of the individual leg currents in (3) is equal to the arm current $i_{u,l}$ and by combining (1)-(3) and (5) the two equations that govern the output and circulating currents are:

$$\begin{aligned} \frac{NL}{2K}\frac{di}{dt} &= \frac{1}{2K}\sum_{n=1}^{N}\left[\mathfrak{z}_{n,l}\, v_{cap|n,l} - \mathfrak{z}_{n,u}\, v_{cap|n,u}\right] - \frac{NR}{2K} i - v \\ \frac{NL}{K}\frac{di_{cir}}{dt} &= \frac{V_{dc}}{2} - \frac{1}{2K}\sum_{n=1}^{N}\left[\mathfrak{z}_{n,l}\, v_{cap|n,l} + \mathfrak{z}_{n,u}\, v_{cap|n,u}\right] - \frac{NR}{K} i_{cir} \end{aligned} \tag{6}$$

By matching inductances L and internal resistances R of the individual inductors in SMs to K/N times of the arm inductance L_{arm} and resistance R_{arm}, as depicted in Fig. 1b, the identical equivalent circuit characteristics of the classical MMC topology can be achieved.

$$L = \frac{K}{N} L_{arm}\,, \qquad R = \frac{K}{N} R_{arm}\,. \tag{7}$$

In this context, substituting (7) into (6) will lead to an identical averaged dynamic model of the proposed ISM-MMC with respect to a classical MMC [9]. In fact, as it will be shown later, only few modifications are required in the control method of ISM-MMC in comparison with standard MMC. This characteristic makes ISM-MMC solution very attractive for retrofitting already built MMCs when higher power capacity of the new converter is required. In addition to that by taking advantage of a proper modulation for driving interleaved HB-legs of each SM, the output characteristics of the converter can be significantly improved.

III. Control and Modulation

The proposed ISM-MMC has primary and secondary control objectives, in the same manner as the classical MMC. The submodule capacitor voltage balancing, and output current control are the primary objectives that directly relate to the operation of ISM-MMC. At the same time, the circulating current control is a secondary objective and associated with the size, reliability, and the efficiency of a converter. Unlike standard MMC, the ISM-MMC has an additional secondary control objective to deal with, namely equal current sharing among interleaved HB-legs in each SM. This problem becomes quite challenging with an increased number of both series connected submodules and interleaved HB-legs. It should be noted though that the current balancing of the interleaved legs is a decoupled control task that is associated with performance of a single submodule and with acceptable level of the currents imbalance it does not affect the operational behavior of the whole converter (the output characteristics remain unchanged). However, the obvious drawback of such unsupervised SM currents operation is a need in oversizing composed SM components. All these aspects are meticulously elaborated in [10], pointing out a need of modification of classical capacitor voltage balancing algorithms, which are widely used in MMC structures. Instead, this section deals with the implementation and performance of classical MMC control methods that reasonably fit for the proposed ISM-MMC with small modifications that are discussed below. In fact, having identical averaging model as a classical MMC, the ISM-MMC features the same dynamic behavior. Therefore, the high-level and internal control of ISM-MMC can be implemented in the same way as for classical MMCs.

A. Control method

Literature discusses the functionality of classical control methods for the MMC topology in great detail. For example, [9], [11] describe the operating and control principle very clearly, including detailed control design and stability analysis. Being thoroughly investigated in many available literature resources, the control design, including gains calculation and stability analysis are omitted in this paper. Therefore, and for the sake of conciseness, here a brief overview is given only.

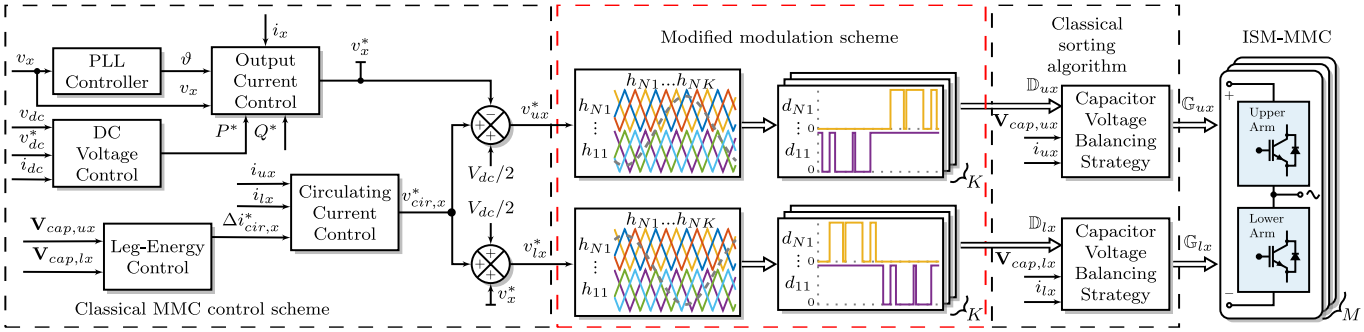

Fig. 3. Block diagram of implemented control method of the proposed ISM-MMC.

The general block diagram of implemented control methods for the proposed ISM-MMC is shown in Fig. 3. This control structure is designed for a front-end converter that interfaces ac grid and can be used in high-power applications, i.e., electric vehicles charging. It includes independent control approaches that are used to regulate dc-link voltage, the submodule capacitors voltage, output currents, and circulating currents. A simple proportional integral (PI) controller with feedforward path is adopted to regulate the dc-link voltage as the outer loop, and it provides the active power reference to the output current regulator that works as the inner loop. In addition to the active power, the reactive power reference can be added to control level or reactive power in the grid. Typically, unity power factor is desirable ($Q^* = 0$) in operation of grid-side converter. The output and circulating currents are adjusted using closed-loop controllers (cf. Fig. 3), which generate control commands v^*_x (reference of the output voltage) and $v^*_{cir,x}$ (compensating reference of the circulating current regulator), respectively. Both controllers are based on proportional resonant (PR) control strategy, capable to effectively track sinusoidal reference and reject disturbance with a low computation burden [9], [11]. The submodule capacitors voltage control aims to maintain the capacitor's voltage at an identical value within the arm. The voltage balancing can be attained either at control or modulation stage. At the control stage an additional closed-loop controller is required while implementing this regulation at modulation stage involves balancing logical functions [12], [13]. In the classical balancing method, associated with level-shifted PWM, the capacitor voltages (vectors $\mathbf{V}_{cap,ux}$, $\mathbf{V}_{cap,lx}$) within an arm are sorted either in ascending or descending order in accordance with the direction of the arm current. Then, the input gate signals are rearranged in agreement with the sorted capacitor voltages and the direction of the arm current. This algorithm operates directly on the generated set of PWM signals (2D arrays $\mathbb{D}_{ux}$, $\mathbb{D}_{lx}$), which are result of comparison between modulating signals and carriers. The output of this block is a set of logical gate signals (2D arrays $\mathbb{G}_{ux}$, $\mathbb{G}_{lx}$) that drive switches. The algorithm itself does not require a modification to meet the balancing requirements for an ISM-MMC since interleaving of HB-legs inside a submodule does not change its equivalent circuit. Nevertheless, the number of commutating switches is increased, and interleaving angles are applied. Likely, the interleaving concept is working entirely within a submodule, therefore, depending on the sorting algorithm action (bypass or insert the submodule), the group of gate signals can be swapped with similar group from another submodule that should be either inserted or bypassed. In this way the voltage balancing algorithm is irrespective of the number of interleaved HB-legs inside the submodule. Another type of control focuses to maintain the sum of capacitor voltages within each converters' arm, at their desired common value, V_{dc}. This closed-loop controller is implemented for multi-phase systems only and it generates a compensating signal $\Delta i^*_{cir,x}$, which is added to the reference of circulating current control. This signal is composed by action of the total (W_Σ) and imbalance (W_Δ) arm energies regulators [9].

B. Modulation

Many modulation schemes have been adopted to MMC based topologies. Among them the most widely employed modulation techniques can be categorized as multilevel carrier-based PWM techniques with either level-shifted (LS-PWM) or phase-shifted (PS-PWM) carriers [14], [15], staircase waveform modulations [16], [17], and space vector modulation (SVM) [18]–[20].

Staircase modulation methods feature fundamental switching frequency, reduced switching losses and simple realization, however it comes with the price of increased harmonic distortion of the output voltage and current waveforms. The quality of output waveforms can be improved by increasing the number of submodules, which is the case for an MMC-based high voltage applications. These staircase methods mainly include selective harmonic elimination (SHE) scheme and nearest level modulation (NLM). The NLM approach is computationally less complex, however its performance is significantly affected by the sorting algorithm and sampling frequency, especially when the number of submodules is low [17]. The SHE scheme requires off-line computation of a large number of switching angles, which increase the computational complexity with the growth of the number of voltage levels.

The SVM directly controls the line-to-line voltages of a modular multilevel converter and allows generating the phase voltages implicitly. In this way SVM eliminates the influence of common-mode voltages and provides more flexibility (i.e., redundant switching sequences) to optimize switching pattern [19]. Nevertheless, the SVM method is difficult to implement for a converter from the MMC family with many voltage levels due to high computational burden.

On the other hand, carrier-based modulation schemes are widely applied to control multilevel power converters due to their simple implementation and ease of extension to higher number of voltage levels. In PS-PWM, the triangular carriers with an identical magnitude are horizontally biased, while in LS-PWM they are disposed vertically. The LS-PWM can be further classified based on the phase relationship between the adjacent carriers into phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD) and other hybrid schemes. The carrier-based modulations usually fall into the high switching frequency category, therefore, have higher switching losses in

comparison with staircase modulation schemes. Moreover, an accurate synchronization between the carriers is essential to generate high-quality voltage and current waveforms [15].

Similarly, the interleaving modulation methods have been well-reported in literature as well. Most of the attention in this regard has been drawn to a phase-shift in the operation of the parallel branches, generally achieved through PS-PWM [21] or SVM [22]. Another trending modulation strategy to handle interleaving in VSCs is the LS-PWM [23], [24].

To drive the proposed ISM-MMC, a hybrid modulation scheme is implemented. It is composed of LS-PWM for synthesizing voltage levels given by series connected SMs whether PS-PWM scheme handles interleaving of parallel HB-legs within each SM. A classical MMC with N SMs per arm (cf. Fig. 1a) can provide either N+1 or 2N+1 levels in the output voltage, depending on whether adjacent level-shifted carriers are synchronized or they are in anti-phase. In relation to LS-PWM N+1 levels correspond to APOD scheme, while 2N+1 levels can be generated with PD approach. In the current work PD LS-PWM has been selected to maximize the number of output levels. Other dispositions will be studied in the future. In addition to that only sinusoidal modulation was applied for this study case for simplicity, while other modulating strategies with common-mode injections, typical for classical MMC, are possible as well.

As it was pointed out in Section II, each interleaved submodule can produce additional K+1 voltage levels. Therefore, in total, the implemented hybrid modulation scheme (cf. Fig. 3) can synthesize 2KN+1 levels [8]. The arm modulation signals, generated by the control scheme described in Section III.A, are compared with corresponding arm carrier signals. For instance, the upper arm ISM-MMC modulation signal is compared with the upper arm carrier signals ($h_{11},\ldots h_{NK}$). The output of the comparator block is a set $\mathbb{D}_{ux}$ of logical PWM signals ($d_{11},\ldots d_{NK}$). Similarly, the lower arm PWM set $\mathbb{D}_{lx}$ is generated. Later, these two sets are applied to the voltage balancing strategy as discussed in Section III.A.

Another characteristic that should be discussed for the implemented hybrid modulation scheme is the switching frequency of ISM-MMC. It is well-known that depending on whether phase displacement between adjacent level-shifted carriers is applied or not the switching frequency of classical MMC can be defined either $Nf_{sw|SM}$ or $2Nf_{sw|SM}$, respectively. The term $f_{sw|SM}$ represents the switching frequency of a submodule. For PS-PWM it is equal to the carrier frequency (f_c), while for LS-PWM it can be calculated as f_c/N. At the same time, the submodule interleaving action (PS-PWM) increases equivalent switching frequency by a factor K. In this context, the hybrid modulation scheme (PD LS-PWM + PS-PWM) will result in the converter's switching frequency $2Kf_c$.

IV. Simulation Results

In this section, numerical simulation results are presented to demonstrate the operation behavior of the proposed ISM-MMC. The comparison of working characteristics between standard MMC and newly introduced topology are made basing on the converter structures given in Fig. 1. As a base architecture, an ISM-MMC with 2 SMs per arm (N = 2) and 3 interleaved HB-legs in each SM (K = 3) was selected. Depending on which carrier frequency was applied 1 or 0.333 kHz, it is labeled as "**N2K3f1k**" or "**N2K3f333**", respectively. A classical MMC, having 2 SMs per arm (N = 2) with 3 parallel switches, which commutate simultaneously at f_c = 1kHz, is labeled as "**N2Kp3f1k**". Another MMC with 6 SMs per arm (N = 6) and f_c = 1kHz is labeled as "**N6K1f1k**". These labels are used throughout the whole paper for short notation of the compared configurations. These configurations have been chosen to demonstrate main differences between the classical MMC and ISM-MMC having similar design parameters (i.e., individual SM capacitance, total number of switches, etc.) or output characteristics (i.e., number of ac voltage levels, etc.). The system example was selected in relation to a real design of the front-end converter in ultra-fast electric vehicle (EV) chargers (i.e., "Terra 184" ABB Ltd.). The main system parameters of compared configurations are listed in Table I. It should be noted that ISM-MMC is easily scalable to any voltage and current levels, therefore, other EV charger designs with few MW power and more can be realized (i.e., "NBSK1000" Power Electronics Corp., "1.5MW Charger" Proterra Corp.). Proper selection of ISM-MMC design parameters (i.e., number of series connected SMs, number of interleaved HB-legs in each SM, etc.) is an optimization problem that includes many variables, for example, cost and power capability of the power electronic switches. This topic is beyond article scope and will be reported in detail in future works.

Performance of the compared configurations was firstly verified under open-loop control operation mainly to demonstrate differences of ac voltage characteristics (cf. Fig. 4) and to introduce behavioral relation between sorting frequency, which is used in the capacitor voltage balancing algorithm, and proper current sharing among interleaved HB-legs in each SM (cf. Fig. 5). It must be noted that although this section refers to "open-loop control" operation, nevertheless, the internal control methods (cf. Fig. 3), such as arm-energy control, circulating current control and capacitor voltage sorting algorithm, are enabled.

TABLE I. Main System Parameters for Compared Configurations

Description	Symbol	N2K3f1k	N2K3f333	N2Kp3f1k	N6K1f1k
number of SM in each arm	N	2	2	2	6
number of HB-legs in each SM	K	3	3	1 (3 paral. sw.)	1
dc output power and dc-link voltage	P_{dc}, V_{dc}	180 kW, 1000 V			
rated ac input power, current (rms)	S_{ac}, i_x	214 kVA, 310 A			
ac line-to-line voltage (rms) and fundamental frequency	v_{xy}, f	400 V, 50 Hz			
sorting frequency	f_{sort}	333 Hz			
carrier frequency	f_c	1 kHz	333 Hz	1 kHz	1 kHz
equivalent arm inductor / individual interleaved inductor (if applicable)	R_{arm}, L_{arm} / R, L	4 mΩ, 1.7 mH / 6 mΩ, 2.5 mH (@ 103.3 A rms)		4 mΩ, 1.7 mH (@ 310 A rms) / -	
equivalent arm capacitance / individual SM capacitance	C_{arm} / C, ESR	3.2 mF / 6.4 mF, 0.2 mΩ			3.2 mF / 19.2 mF, 0.2 mΩ
IGBT module (Infineon Technologies AG)	-	FF150R12RT4			FF450R07ME4

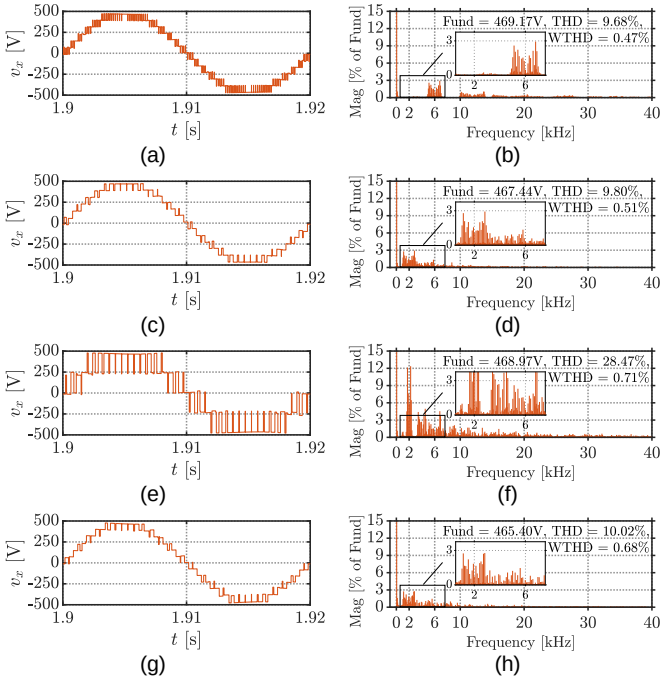

Fig. 4. Phase voltage and its corresponding harmonic content in ISM-MMC (a-d) and classical MMC (e-h) for the following subcases: (a,b) **N2K3f1k**; (c,d) **N2K3f333**; (e,f) **N2Kp3f1k**; (g,h) **N6K1f1k**.

For this test, the compared topologies were working in inverter mode delivering power from dc to ac side. The reference output power was selected similar to the system design example (cf. Table I), namely 180 kW operating with unity power factor. To depict the maximum of available ac phase voltage levels, the highest modulation index from linear modulation range of the sinusoidal PWM (without overmodulation) was selected. To speed up convergence of output characteristics to steady state values after the start-up, a higher value of internal resistance of interleaved inductors was set (R_{arm} = 156.4 mΩ / R = 234.7 mΩ where it is applicable). Considering internal resistances of the other components (i.e., IGBT modules, capacitors) they remain unchanged. The increase results in a higher equivalent arm resistance and consequently larger voltage drop. This effect is well noticeable in Fig. 4. However, it does not introduce tremendous effect on the performed comparative analysis. As expected, configurations "**N2K3f1k**", "**N2K3f333**" and "**N6K1f1k**" can generate 13 voltage levels operating under PD LS-PWM scheme. It is interesting to notice here that "**N2K3f333**" and "**N6K1f1k**" have quite similar harmonic spectrum with dominant switching harmonic components appearing as a first sideband at 2 kHz. This effect was explained in Section III.B. On the other hand, "**N2K3f1k**" with similar THD exhibits superior performance since the first sideband harmonics are located around 6 kHz, consequently reducing requirements for the ac interface filter. In this context, weighted THD (WTHD) [25] can quantitatively justify greater performance of "**N2K3f1k**" in comparison with other converter arrangements. At the same time "**N2Kp3f1k**" having the same number of SMs (capacitors) and power switches that work without interleaving scheme can synthesize only 5 voltage levels with remarkably high harmonic pollution.

Another noteworthy characteristic of ISM-MMC is the relation

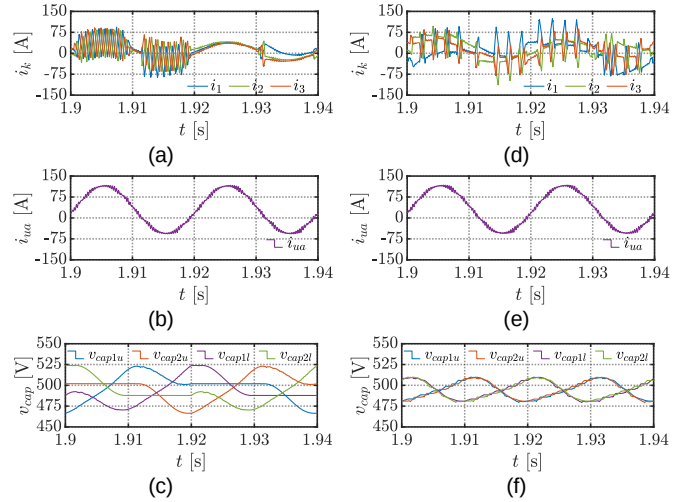

Fig. 5. Interleaved leg currents in one submodule of ISM-MMC (a,d), the corresponding arm current (b,e) and capacitor voltages in phase *'a'* of ISM-MMC (c,f) at sorting frequency 50 Hz (a,b,c) and at 1 kHz (d,e,f).

between sorting frequency of capacitor voltage balancing algorithm, and equal current sharing among interleaved HB-legs in each SM. It is well visible from Fig. 5 that operating with low sorting frequency of voltage balancing function, better current distribution among interleaved legs can be achieved. Conversely, higher sorting frequency results in higher imbalance of the currents in interleaved legs. This fact can be explained by significant time constants of interleaved inductors and large number of commutations within one fundamental period provoked by capacitor voltage balancing algorithm. This aspect must be taken into account while selecting sorting frequency. The summation of interleaved currents cancels out part of the ripple, that in this way, does not affected output SM's current (i.e., the arm current), output phase current, and circulating current that is part of the arm current (cf. dc offset in Fig. 5b,e).

V. Comparison

This section gives a comparative analysis of major features of the converter configurations listed in Table I. The first aspect to be compared is the number of main components (i.e., IGBT modules, inductors, capacitors, etc.) and their characteristics (current and voltage ratings, etc.). All configurations have the same number of power switches, while arrangement and operation modes are different. The two chosen reference IGBT modules are from the same generation, device family and manufactured by the same company. The "FF150R12RT4" module is designed with the following maximum rated values: collector-emitter voltage 1200V and continuous dc current 150A. Similarly, the "FF450R07ME4" has the following maximum ratings: 650V and 450A, respectively. Configurations "**N2K3f1k**" and "**N2K3f333**" feature distributed inductor arrangement, having 6 inductors in total per arm. In contrast, "**N2Kp3f1k**" and "**N6K1f1k**" have only one inductor per arm. Although structural characteristics of these inductors are different (internal resistance and inductances), one should note that distributed (interleaved) inductors carry only a portion of arm current, thus, can be designed with a significantly smaller cross-section of composed wires. This fact directly reflects on cost, weight and volume of the converter. To form either ISM-MMC

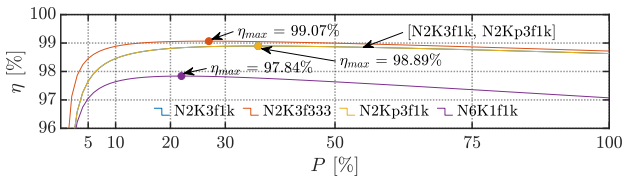

Fig. 6. Converter efficiency for compared cases.

("**N2K3f1k**" and "**N2K3f333**") or classical MMC ("**N2Kp3f1k**") configurations with 2 SMs per arm only 2 capacitors per arm are needed. In fact, for high current applications those SM capacitors are composed of a set of parallel connected capacitors. However, for simplicity it will be assumed that the SM capacitors are single components. For the "**N6K1f1k**" configuration 6 capacitors per arm are required. Yet, to keep voltage ripple across the capacitors within ±10% tolerance band of its average value, the size of capacitors must be increased drastically. As a matter of fact, the classical MMC configuration is not well suitable for low-voltage, high-power applications, since an increase of ac voltage levels results in a corresponding increment of series connected SMs in each arm, while low dc-link voltage significantly reduces allowed fluctuating voltage range of SM capacitors, therefore, a bigger capacitor is required in each SM.

Analytical developments for the converter efficiency have been discussed in literature in great detail (e.g., [26]–[28]). Therefore, for sake of conciseness, the efficiency formulation is omitted in this paper. Instead, the focus has been given to the comparison between studied configurations. Nevertheless, some assumptions must be taken into consideration in the analytical derivations of the converter efficiency, namely constant capacitor voltage in each SM, circulating current purely composed by a dc component, which can be computed as the dc current equally shared among converters' phases, unity power factor, and almost sinusoidal (ripple magnitude is negligible) balanced currents in the interleaved HB-legs. System parameters from Table I, 125 °C junction temperature, and 100 W driving losses (gate-driving losses: 50 W @ 1 kHz) have been used in the efficiency analysis.

Fig. 6 depicts efficiencies for the compared converter configurations. Firstly, "**N2K3f1k**" and "**N2Kp3f1k**" have almost identical efficiency curve since they have similar circuital structure and operating switching frequencies, leading to indistinguishable conduction and switching losses. The main difference among them is the interleaving effect, which does not notably affect efficiency. Instead, "**N2K3f333**" operates with one third switching frequency, reducing by 66% switching and gate-driving losses in comparison to "**N2K3f1k**" or "**N2Kp3f1k**". A significantly lower efficiency can be observed in the "**N6K1f1k**" case due to higher conduction losses caused by the large number of series submodules. Capacitor and inductor (copper only) losses do not play relevant roles. Overall, it is evident from the analysis that the ISM-MMC can offer higher or equal efficiency in comparison with classical MMC, while having the same or enhanced harmonic spectrum features of the converter, depending on operating switching frequency.

TABLE II. SUMMARY OF THE COMPARISON (THREE-PHASE SYSTEM)

Characteristic	N2K3f1k	N2K3f333	N2Kp3f1k	N6K1f1k
number of active switches (rated blocking voltage, rated rms current)	72 (1200 V, 150 A)	72 (1200 V, 150 A)	72 (1200 V, 150 A)	72 (650 V, 450 A)
number of SM capacitors (capacitance, rated voltage)	12 (6.4 mF, 1200 V)	12 (6.4 mF, 1200 V)	12 (6.4 mF, 1200 V)	36 (19.2mF, 400 V)
number of arm/interleaved inductors (rated rms current)	- / 36 (2.5 mH, 103.3 A)	- / 36 (2.5 mH, 103.3 A)	6 / - (1.7 mH, 310 A)	6 / - (1.7 mH, 310 A)
maximum number of phase voltage level @ PD LS-PWM	13	13	5	13
equivalent switching freq. @ PD LS-PWM (carrier freq.)	6 kHz (1 kHz)	2 kHz (333 Hz)	2 kHz (1 kHz)	2 kHz (1 kHz)
weighted efficiency "eu"/"cal"	98.68% / 98.81%	98.95% / 99.01%	98.68% / 98.81%	97.66% / 97.72%

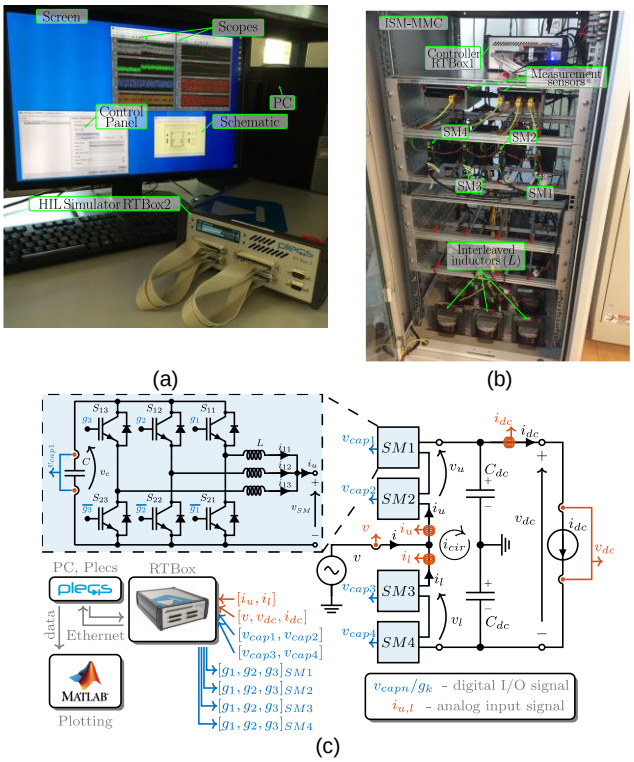

Fig. 7. View of the HIL simulator (a), experimental setup (b) and circuit scheme of the test single-phase ISM-MMC (c).

Table II provides a summary of the performed comparison including some structural and performance characteristics. To demonstrate unique performance characteristic of the conversion system the weighted efficiencies with labels "eu" and "cal" are included in Table II. They represent equivalent conversion efficiencies, which has been calculated similarly to the so called "European" ("eu") and "Californian" ("cal") efficiencies in [29] for grid connected photovoltaic systems.

VI. PRACTICAL IMPLEMENTATION

Fig. 7 depicts a view of the HIL setup, experimental test bench and circuit scheme of the single-phase ISM-MMC converter. The single-phase structure of ISM-MMC was used for both HIL implementations and experimental tests. The following subsections contain necessary description of main parameters have been used for performed tests. The HIL and experimental tests are designed to demonstrate dynamic behavior of the new ISM-MMC topology and verify applicability of the classical MMC control techniques.

A. Hardware-in-the-loop implementation and tests

Recently, HIL simulators have been widely adopted for commissioning and testing of multilevel converters [30]. In current work, HIL tests have been performed using RT Box2 (Plexim) in

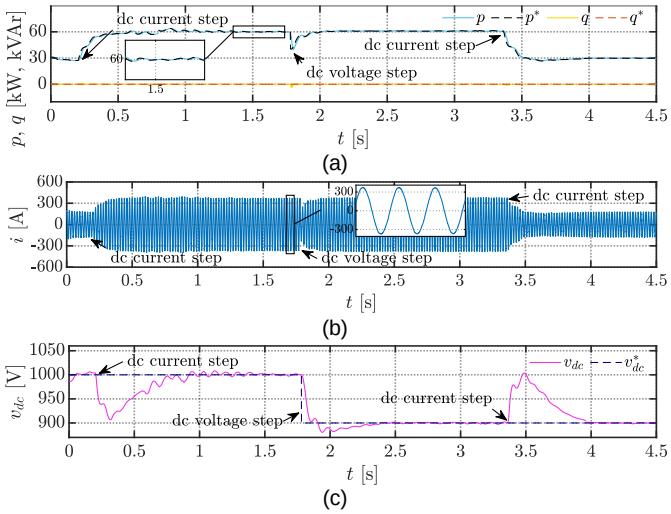

Fig. 8. Active and reactive powers (a) supplied by the grid (solid lines) along with their reference values (dashed lines), ac phase current (b) and dc-link voltage (c) – measured value (solid line) and its reference (dashed line).

the PLECS environment with sampling period 12.5µs. The HIL simulation results are presented for "**N2K3f1k**" case only. To reduce the computation burden of the HIL setup, for these tests a single-phase ISM-MMC with 2 SMs per arm (N=2) and 3 interleaved legs in each SM (K=3) was used. The real-time simulation was performed in a multitasking mode, such that power circuit was emulated on CPU1 and CPU2, while the entire control has been deployed on CPU3.

The single-phase, grid-connected (230 Vrms) ISM-MMC supplies a dc load (60 kW) with unity power factor via the dc-link. A split dc-link capacitor (C_{dc} = 15 mF) provides the reference neutral wire connection. The dc load was realized as a controlled current source (i_{dc}) with known demand profile. The profile includes a step-like change of dc current by 50% from half to full demand and back. The second dc current step is applied when the system has already experienced a step-like drop of dc-link voltage by 10%. The interleaved inductors internal resistance was set to a higher value in comparison with Table I (R_{arm} = 30.3 mΩ / R = 45.5 mΩ) to smooth divergence of interleaved currents from one another since they are not actively controlled. The resistance values were selected smaller in comparison to those in Section IV to have a well noticeable current imbalance within SMs and consequently demonstrate that this imbalance does not affect the I/O converter's characteristics. These resistances include also IGBT on-state resistance.

The rest parameters of passive components (L, C, cf. Table I) were assigned with reference to real commercial components having standard tolerances. For R, L the tolerance is 15%, while for C it is 10%. Accounting of these tolerances in simulations was made by generating random values following a Gaussian distribution and having a confidence interval of ±4σ.

Fig. 8 depicts measured ac powers (active and reactive) supplied by the grid, the corresponding ac phase current, and dc-link voltage along with its reference. Fig. 8a confirms that the HIL simulated ISM-MMC operates with unity power factor.

Fig. 9a presents measured capacitor voltages from each submodule of the single-phase ISM-MMC. The dashed lines in this plot represent ±10% voltage ripple tolerance band and mean value of capacitor voltage. Dynamic behavior of circulating current in

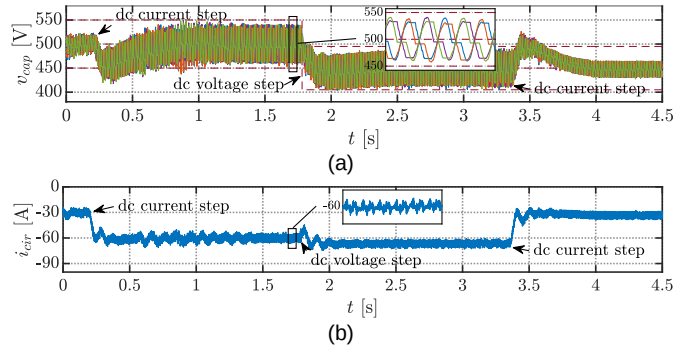

Fig. 9. Capacitor voltages (a) from each submodule of the ISM-MMC (solid traces) along with its ±10% tolerance band and mean value (dashed lines) and corresponding circulating current (b) in phase leg of ISM-MMC.

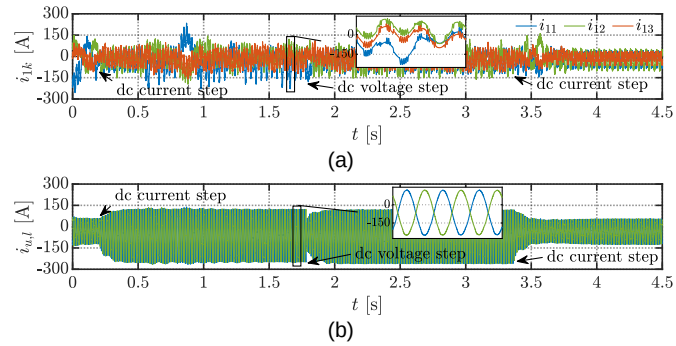

Fig. 10. Currents in interleaved legs of the submodule SM1 (a) and arm currents of ISM-MMC (b).

response of the imposed system changes can be seen from Fig. 9b. Circulating current after some transients reaches steady state values depending on the operating point. The circulating current is composed of dc current and high frequency ripple component. Overall, the system behavior under classical MMC close-loop control demonstrates expected, stable performance in all tested operational modes having passive components unequal parameters.

Fig. 10 confirms the fact that the balancing of interleaved currents is a decoupled control task and should be implemented individually in each SM. Interleaved currents balancing as previously mentioned is outside the scope of this paper. Nevertheless, it worth to notice that even though the currents inside of a SM are unbalanced (cf. currents fundamental components) and feature high-magnitude ripple, the sum of them (arm current) remains balanced and sinusoidal-like.

B. Experimental implementation and tests

The laboratory ISM-MMC has a single-phase configuration with two SMs per arm. Each submodule consists of a custom-made three-leg converter formed by an intelligent power module (DIPIPM PS219B4-AS, Mitsubishi Electric) and connected to a capacitor (C) at its dc side, while ac terminals are linked with uncoupled iron-core inductors (L). The converter operates in a rectification mode, feeding an electronic load (i_{dc}). To control the power stage RTBox1 (Plexim) has been used. Sensed voltages and currents enter RTBox1 either as analog (red symbols cf. Fig. 7c) or digital (blue symbols cf. Fig. 7c) signals. The digital outputs of RTBox1 are the firing PWM signals for the power switches. Optical fiber links have been used to isolate digital inputs and outputs from the power boards. RTBox1 is equipped with a high-speed Ethernet connection, creating a channel with a PC for data

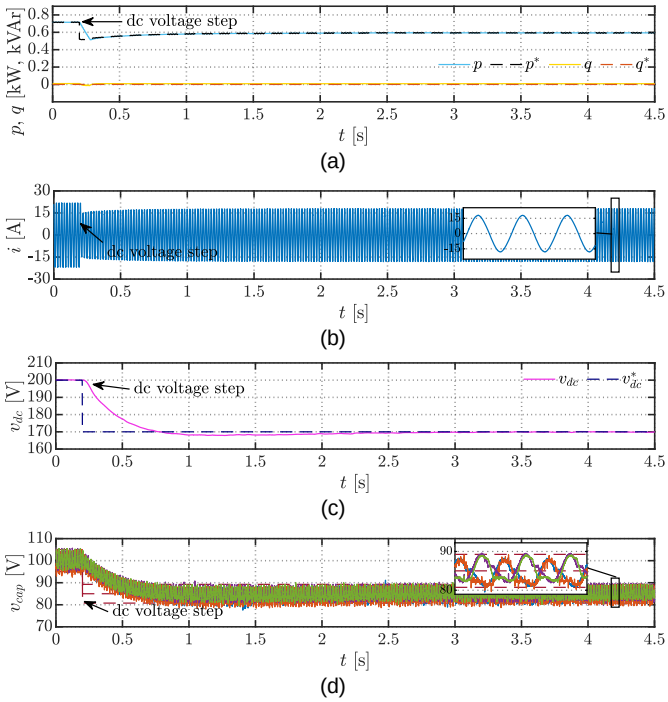

Fig. 11. Dc voltage step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines), ac phase current (b), dc-link voltage (c) – measured value (solid trace) and its reference (dashed trace) and capacitor voltages (d) from each submodule of the ISM-MMC (solid traces) along with its ±10% tolerance band and mean value (dashed lines).

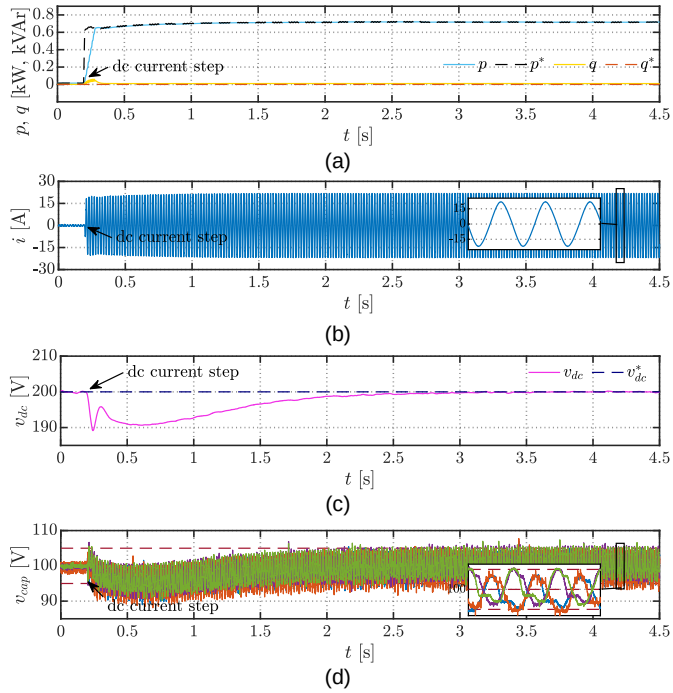

Fig. 12. Dc current step. Active and reactive powers (a) supplied by the grid (solid traces) along with their reference values (dashed lines), ac phase current (b), dc-link voltage (c) – measured value (solid trace) and its reference (dashed trace) and capacitor voltages (d) from each submodule of the ISM-MMC (solid traces) along with its ±10% tolerance band and mean value (dashed lines).

acquisition and real-time target control through a PLECS (Plexim) model. The maximum sampling period of the controller is 20 µs. The measured signals sampled with the same sampling period and stored on the PC for the subsequent post-processing (figures plotting) in MATLAB (MathWorks). The main parameters of the laboratory prototype are given in Table III.

Various experiments were performed to validate applicability of the classical MMC control methods on the new topology. The first test verifies the converter response on a dc current step rise from 0 to 3 A. Fig. 11 depicts the instantaneous ac active and reactive powers along with their references, ac phase current, dc-link voltage, and SM capacity or voltages. It can be observed that the transient of dc-link voltage caused by the dc current step is cleared around 3s. Similarly, SM capacitor voltages feature double fundamental frequency oscillations with the expected maximum ripple magnitude (remain bounded by tolerance band, dashed traces). All measures have a clean and well-balanced profile.

TABLE III. MAIN PARAMETERS OF THE LABORATORY PROTOTYPE

Description	Labels	Parameters
number of SMs per arm	N	2
number of interleaved HB legs in each SM	K	3
individual interleaved leg inductor parameters	R, L	244 mΩ, 12.6 mH
capacitance in each SM	C	3.54 mF
dc-link split capacitance (2x)	C_{dc}	5.2 mF
rated line-to-neutral voltage (rms)	v	50 V
power factor	-	1
fundamental frequency	f	50 Hz
rated dc power and dc-link voltage	P_{dc} ,v_{dc}	600 W, 200 V
carrier frequency	f_c	2 kHz
sorting frequency	f_{sort}	400 Hz

The second experiment demonstrates that the system produces stable, balanced response for a dc voltage drop from 200 to 170V. Fig. 12 illustrates the same quantities of Fig. 11 for the dc voltage step test. It can be seen that the new steady-state value is reached after roughly 2.2s from the step change occur.

All in all, based on the implemented HIL simulations and experimental test with different power levels, it is possible to claim that the classical MMC control methods are equally suitable for the new ISM-MMC converter. This fact works in favor to the ISM-MMC as an alternative topology to the classical MMC.

The study of experimental setup efficiency is not part of this paper since the laboratory setup operates at reduced power levels (~600 W), while the converter design is not optimal (based on the available components in the laboratory) leading to substantial power losses. For example, at rated dc power and dc-link voltage (cf. Table III) the overall converter's efficiency is about 85%, calculated basing on the input power ~710 W (as visible in Fig. 11a) and the output power ~600 W (given by 200 V and 3 A). However, one should not take this number as a reference since, the primary goal of the setup is to verify feasibility of the new topology, check performance of the suggested modulation and control, while the comparative efficiency analysis is implemented analytically in Section V.

VII. CONCLUSION

A new interleaved submodule structure has been proposed for modular multilevel converters, forming a novel topology named ISM-MMC. Among strong points of the new converter structure are easily scalable voltage and current ratings, suitable for all voltage levels high power applications, enhanced output

waveforms, improved efficiency and fault tolerance capability. The latter concept justified by highly modular structure of SMs in ISM-MMC exploiting benefits of parallel systems (term in readability studies), where failure of a single component (HB-leg) does not mean failure of whole system (SM). On the contrary some drawbacks are increased complexity of the converter architecture with many switching devices to be controlled, proper current sharing between interleaved legs within SM, larger number of required inductors. Nevertheless, it should be pointed out that inductors distributed arrangement is not necessarily a weak point since the inductors current ratings is proportionally less than a classical arm inductor. Therefore, an optimal design, can reach equal or superior qualitive characteristics (cost, weight, etc.).

A proper modulation scheme has been presented consisting of level shifted PWM for controlling the submodules and phase shifted PWM for driving the different legs inside each submodule. In addition to that the applicability of classical MMC control techniques for ISM-MMC has been proven.

Numerical simulations, HIL and experimental tests were carried out to validate key features of ISM-MMC and the implemented modulation technique, eventually proving feasibility of the proposed MMC-based structure with reference to ultrafast EV charging infrastructure. Efficiency comparison between several classical MMC and ISM-MMC configurations is presented by showing a relative efficiency gain up to 1.56% (with total power losses reduction up to 53.24%) depending on the compared configurations and operating power level.

A future development could refer to an optimal design of ISM-MMC, considering cost and characteristics of the composing components (i.e., less SMs/interleaved legs with higher ratings or more SMs/interleaved legs with reduced ratings). In addition, a proper design of interleaved inductors must be studied, considering maximum allowed peak-to-peak current ripple in interleaved assemblies and output characteristics of the converter.

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